

DATA SHEET

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74LVC827A

10-bit buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

Product specification

1998 Sep 04

10-bit buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC827A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when $V_{CC} = 0V$

DESCRIPTION

The 74LVC827A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-state operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC827A is a 10-bit buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs \overline{OE}_1 and \overline{OE}_2 .

A HIGH on \overline{OE}_n causes the outputs to assume a high impedance OFF-state.

QUICK REFERENCE DATA

$GND = 0V$; $T_{amb} = 25^\circ C$; $t_r = t_f \leq 2.5 ns$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay A_n to Y_n	$C_L = 50 pF$; $V_{CC} = 3.3 V$	4	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1 and 2	24	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_I = GND$ to V_{CC} .

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	-40°C to +85°C	74LVC827A D	74LVC827A D	SOT137-1
24-Pin Plastic SSOP Type II	-40°C to +85°C	74LVC827A DB	74LVC827A DB	SOT340-1
24-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVC827A PW	7LVC827APW DH	SOT355-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{OE}_1, \overline{OE}_2$	Output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_9	Data inputs
12	GND	Ground (0 V)
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Y_0 to Y_9	Bus outputs
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

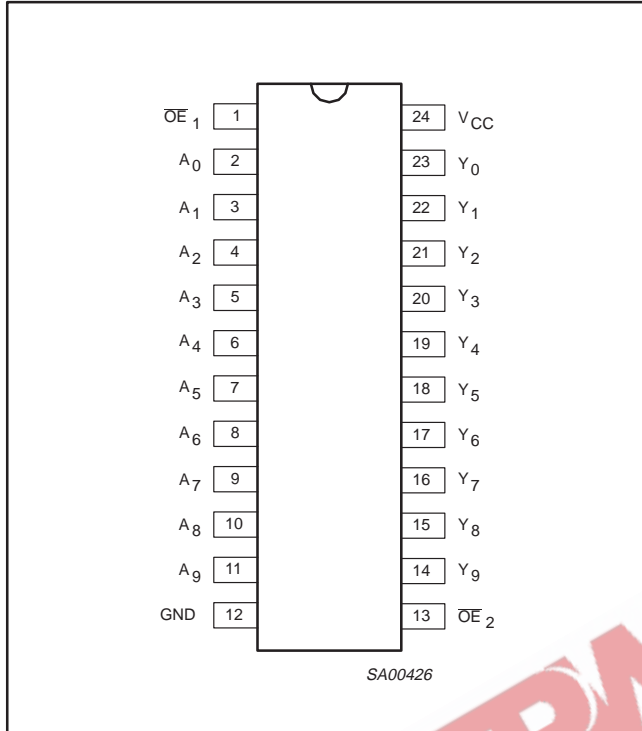
INPUTS			OUTPUTS
\overline{OE}_1	\overline{OE}_2	A_n	Y_n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 Z = high impedance OFF-state

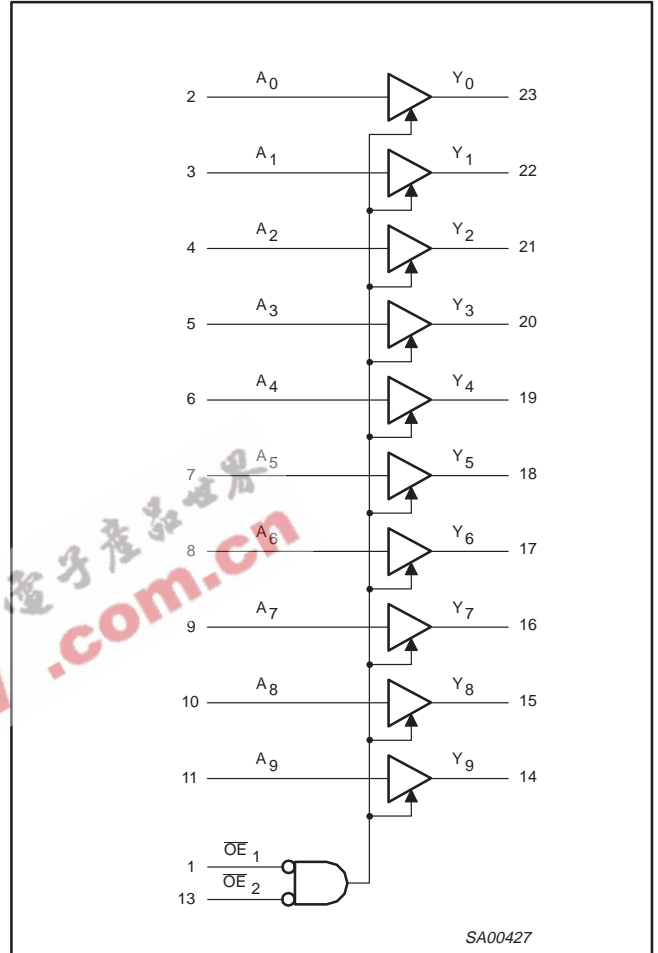
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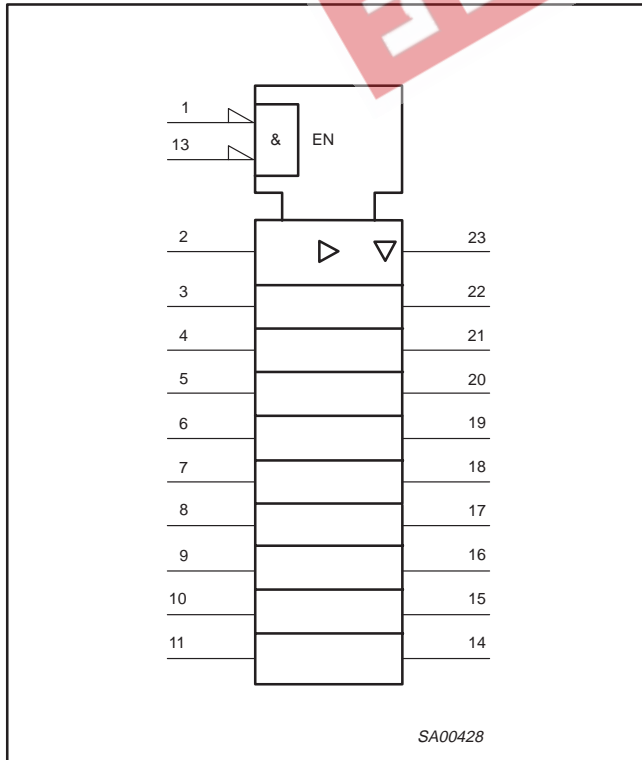
PIN CONFIGURATION



LOGIC SYMBOL



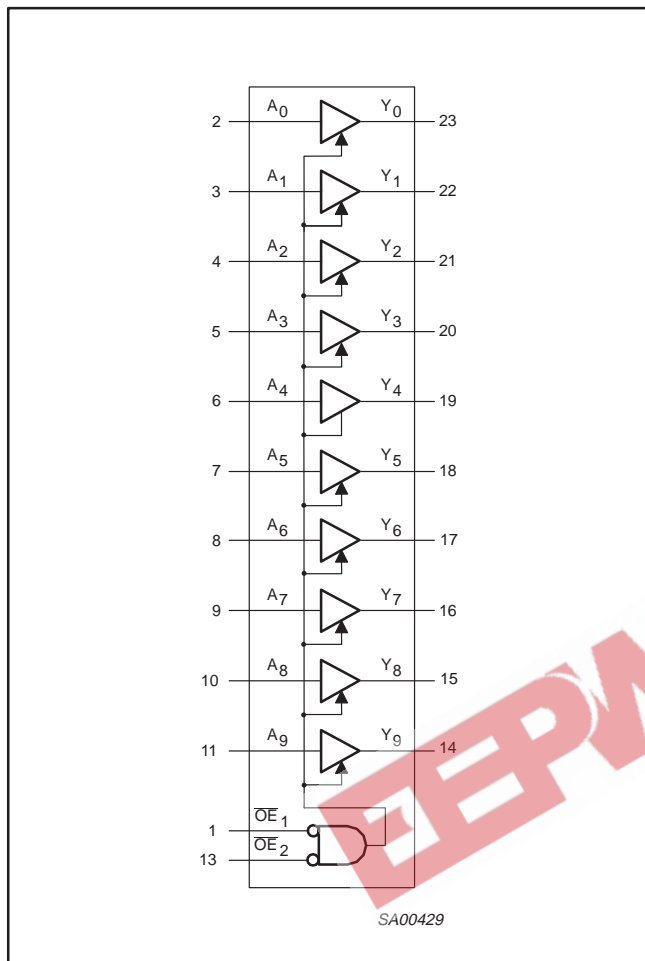
LOGIC SYMBOL (IEEE/IEC)



10-bit buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

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FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V _{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V _I	DC Input voltage range		0	5.5	V
V _O	DC output voltage range; output HIGH or LOW state		0	V _{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T _{amb}	Operating ambient temperature range in free-air		-40	+85	°C
t _r , t _f	Input rise and fall times	V _{CC} = 1.2 to 2.7V	0	20	ns/V
		V _{CC} = 2.7 to 3.6V	0	10	

10-bit buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

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ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	Note 2	-0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	-0.5 to $V_{CC} + 0.5$	V
	DC output voltage; output 3-State	Note 2	-0.5 to 6.5	
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K	500	mW
		above +60°C derate linearly with 5.5 mW/K	500	

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V_{IH}	HIGH level Input voltage	$V_{CC} = 1.2V$	V_{CC}			V
		$V_{CC} = 2.7$ to $3.6V$	2.0			
V_{IL}	LOW level Input voltage	$V_{CC} = 1.2V$			GND	V
		$V_{CC} = 2.7$ to $3.6V$			0.8	
V_{OH}	HIGH level output voltage	$V_{CC} = 2.7V; V_I = V_{IH}$ or $V_{IL}; I_O = -12mA$	$V_{CC} - 0.5$			V
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = -100\mu A$	$V_{CC} - 0.2$	V_{CC}		
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = -18mA$	$V_{CC} - 0.6$			
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = -24mA$	$V_{CC} - 0.8$			
V_{OL}	LOW level output voltage	$V_{CC} = 2.7V; V_I = V_{IH}$ or $V_{IL}; I_O = 12mA$			0.40	V
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$			0.20	
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 24mA$			0.55	

NOTES:

- All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
- The specified overdrive current at the data input forces the data input to the opposite logic input state.

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DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			Temp = -40°C to +85°C				
			MIN	TYP ¹	MAX		
I_I	Input leakage current	$V_{CC} = 3.6V$; $V_I = 5.5V$ or GND	Not for I/O pins		± 0.1	± 5	μA
I_{OZ}	3-State output OFF-state current	$V_{CC} = 3.6V$; $V_I = V_{IH}$ or V_{IL} ; $V_O = 5.5V$ or GND			0.1	± 5	μA
I_{off}	Power off leakage supply	$V_{CC} = 0.0V$; V_I or $V_O = 5.5V$			0.1	± 10	μA
I_{CC}	Quiescent supply current	$V_{CC} = 3.6V$; $V_I = V_{CC}$ or GND; $I_O = 0$			0.1	10	μA
ΔI_{CC}	Additional quiescent supply current per input pin	$V_{CC} = 2.7V$ to $3.6V$; $V_I = V_{CC} - 0.6V$; $I_O = 0$			5	500	μA

NOTES:

- All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
- The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$; $T_{amb} = -40^\circ C$ to $+85^\circ C$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		$V_{CC} = 1.2V$	
			MIN	TYP ¹	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	Figures 1, 3	1.5	4.0	6.7	1.5	7.1	15	ns
t_{PZH} t_{PZL}	3-State output enable time \overline{OE}_1 to $1Y_n$; \overline{OE}_2 to $2Y_n$	Figures 2, 3	1.5	5.4	8.5	1.5	9.5	25	ns
t_{PHZ} t_{PLZ}	3-State output disable time \overline{OE}_1 to $1Y_n$; \overline{OE}_2 to $2Y_n$	Figures 2, 3	1.5	4.0	6.7	1.5	7.3	11	ns

NOTE:

- Unless otherwise stated, all typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.

AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7V$.

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7V$

$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7V$

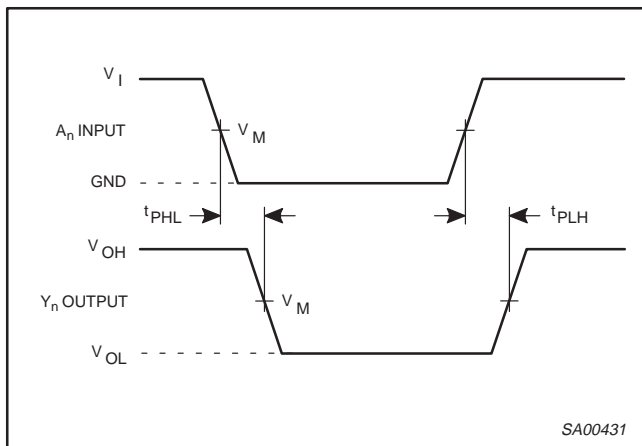


Figure 1. The input (A_n) to output (Y_n) propagation delays.

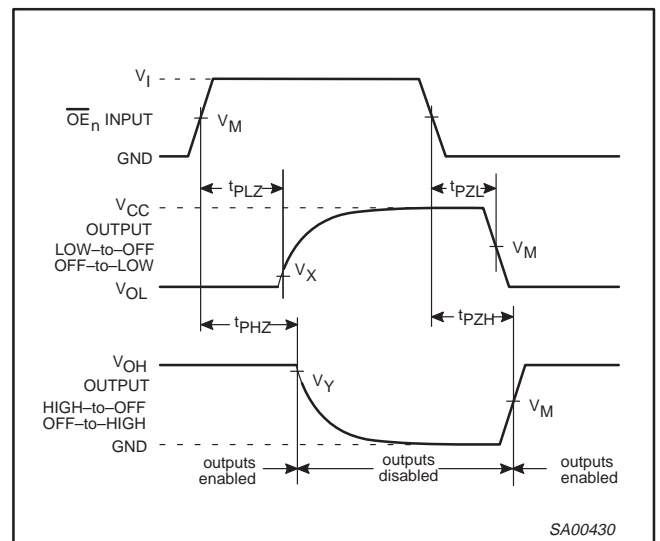


Figure 2. 3-State enable and disable times.

10-bit buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

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TEST CIRCUIT

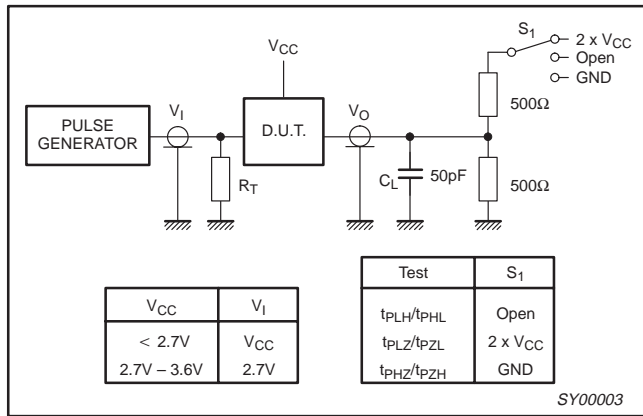


Figure 3. Load circuitry for switching times.

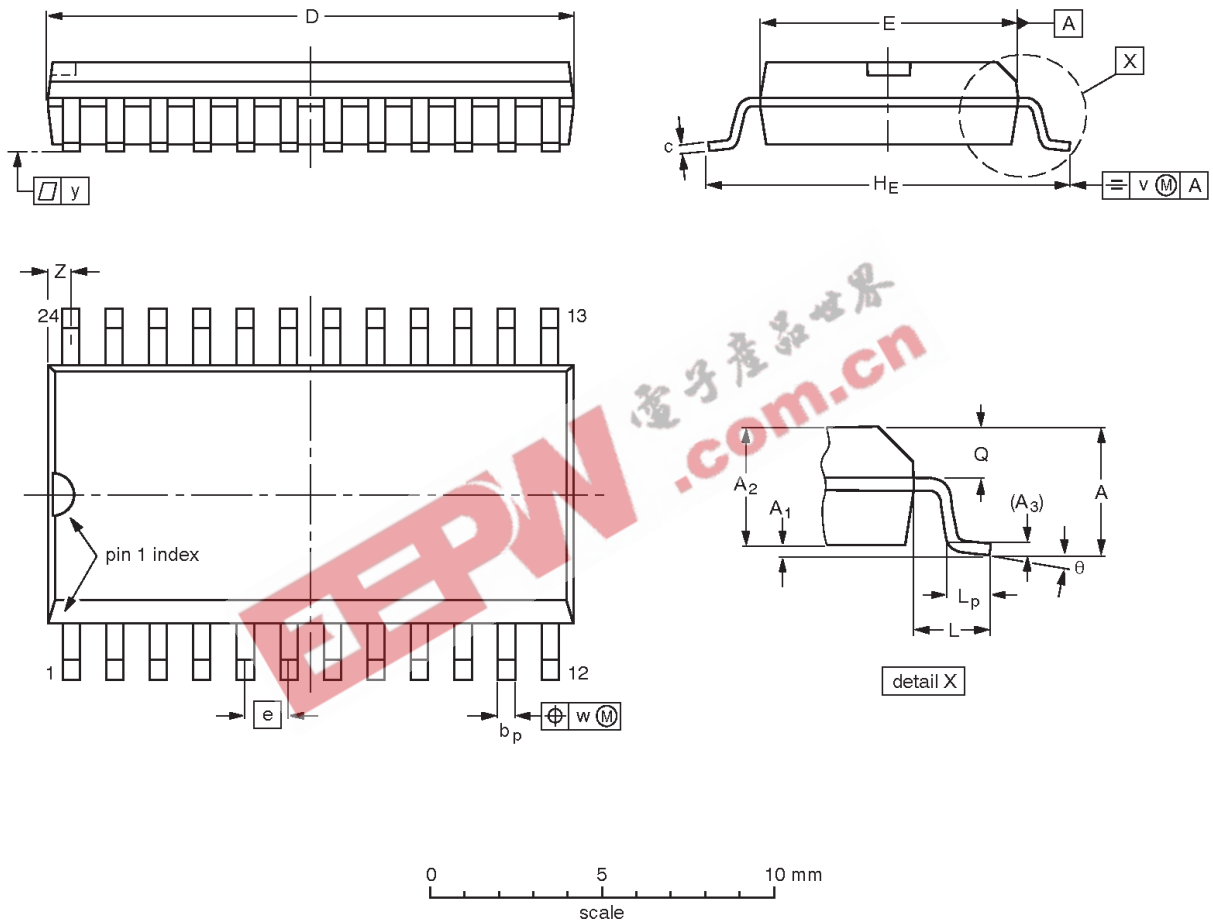


10-bit buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

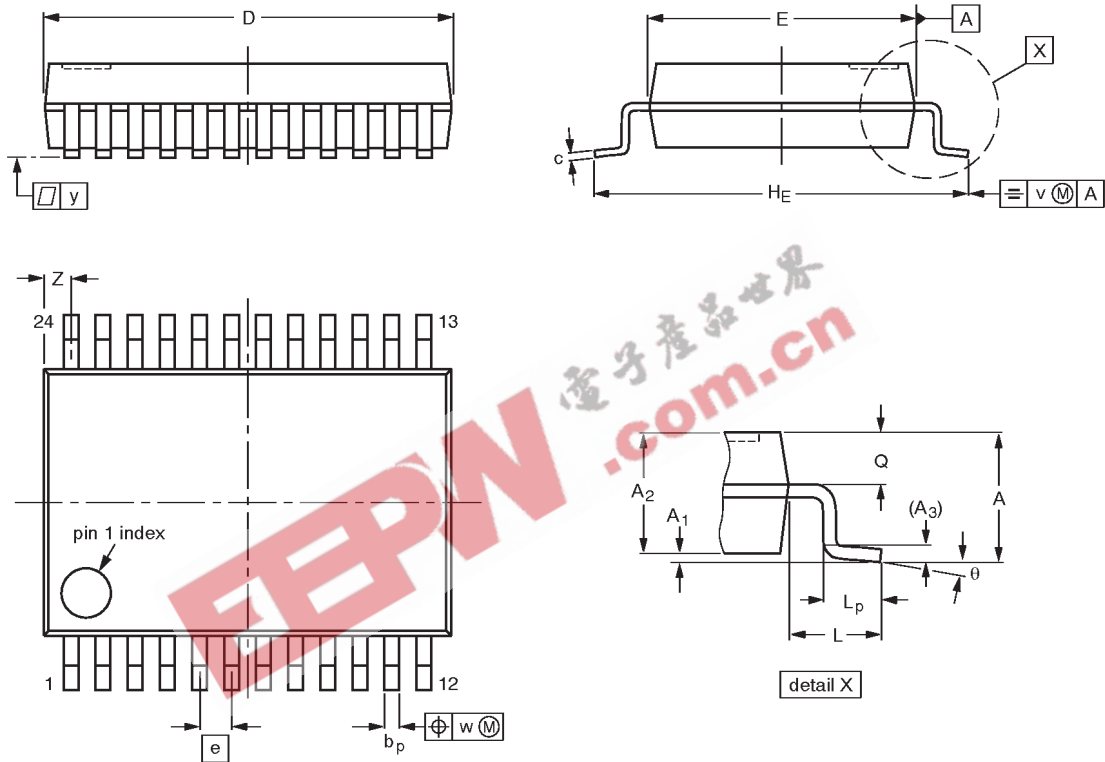
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

10-bit buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

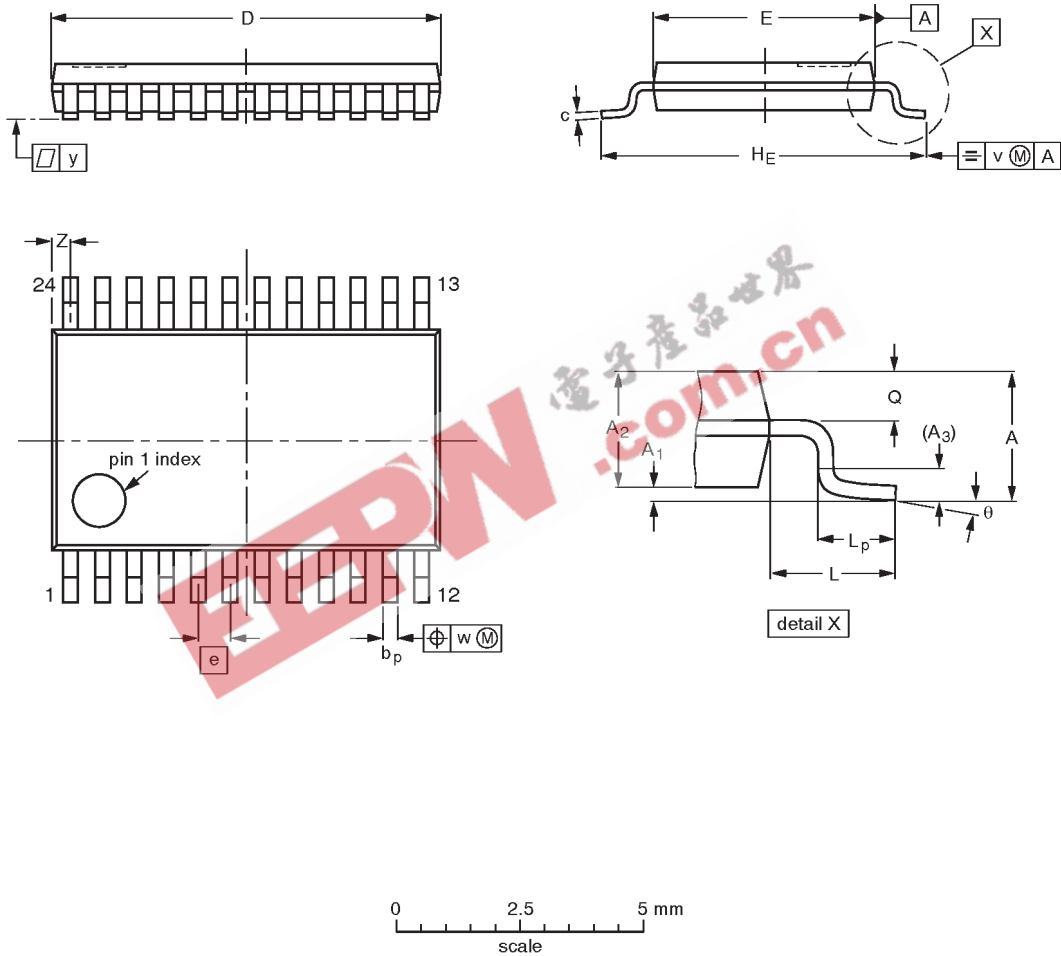
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08 95-02-04

10-bit buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC827A

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				93-06-16 95-02-04

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NOTES



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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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print code

Date of release: 08-98

Document order number:

9397-750-04521

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