

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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74HC/HCT7245 Octal bus Schmitt-trigger transceiver; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

Octal bus Schmitt-trigger transceiver; 3-state

74HC/HCT7245

FEATURES

- Octal bidirectional bus interface
- Non-inverting 3-state outputs
- Output capability: bus driver
- I_{CC} category: MSI
- Schmitt-trigger action on all data inputs

GENERAL DESCRIPTION

The 74HC/HCT7245 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in

compliance with JEDEC standard no. 7A.

The 74HC/HCT7245 are octal transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The "7245" features an output enable (\overline{OE}) input for easy cascading and a send/receive input (DIR) for direction control. \overline{OE} controls the outputs so that the buses are effectively isolated. The 74HC/HCT7245 have Schmitt-trigger inputs. These inputs are capable of transforming slowly changing input signals into sharply defined jitter-free output signals.

The "7245" is identical to the "245" but has hysteresis on the data inputs.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
\overline{OE}	DIR	A _n	B _n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

Notes

1. H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay A _n to B _n	C _L = 15 pF; V _{CC} = 5 V	8	12	ns
C _I	input capacitance		3.5	3.5	pF
C _{I/O}	input/output capacitance		10	10	pF
C _{PD}	power dissipation capacitance per transceiver	notes 1 and 2	40	40	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

ORDERING INFORMATION

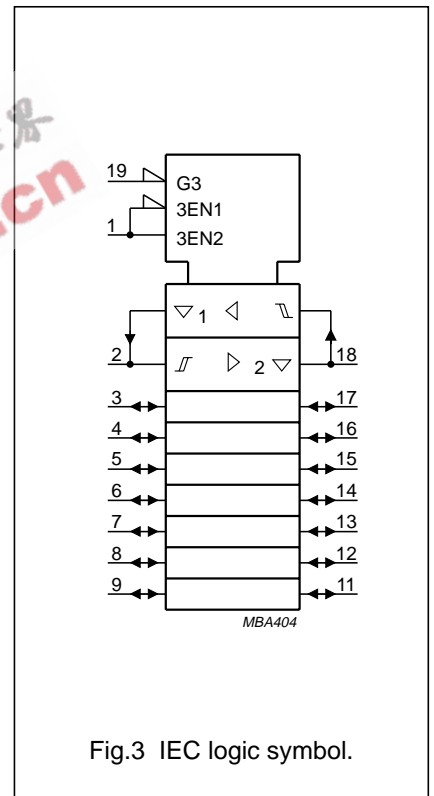
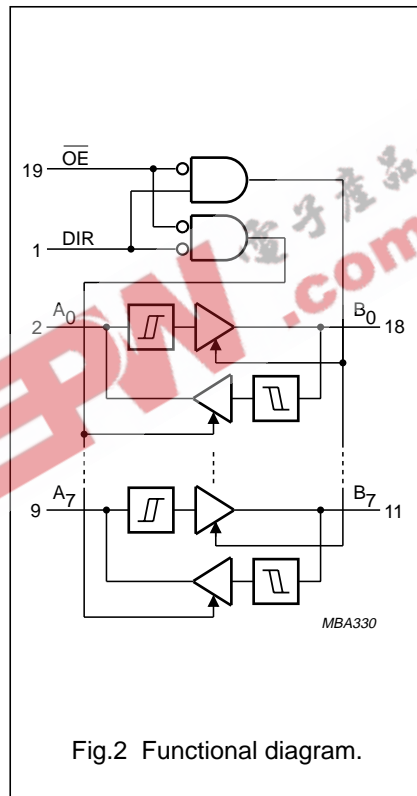
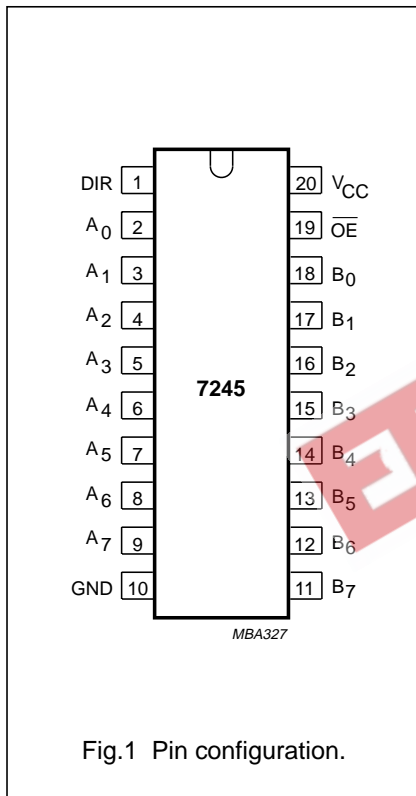
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Octal bus Schmitt-trigger transceiver;
3-state

74HC/HCT7245

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₇	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B ₀ to B ₇	data inputs/outputs
19	\overline{OE}	output enable input (active LOW)
20	V _{CC}	positive supply voltage



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74HC/HCT7245

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are referred to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
V _{T+}	positive-going threshold			1.50 3.15 4.20		1.50 3.15 4.20		1.50 3.15 4.20	V	2.0 4.5 6.0	Figs. 4 and 5
V _{T-}	negative-going threshold	0.30 1.35 1.80			0.30 1.35 1.80		0.30 1.35 1.80		V	2.0 4.5 6.0	Figs. 4 and 5
V _H	hysteresis (V _{T+} - V _{T-})	0.1 0.25 0.3	0.2 0.4 0.5		0.1 0.25 0.3		0.1 0.25 0.3		V	2.0 4.5 6.0	Figs. 4 and 5

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay A _n to B _n ; B _n to A _n		33 12 10	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.7
t _{PZH} / t _{PZL}	3-state output enable time \overline{OE} to A _n ; \overline{OE} to B _n		47 17 14	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.7
t _{PHZ} / t _{PLZ}	3-state output disable time \overline{OE} to A _n ; \overline{OE} to B _n		52 19 16	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.7
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.7

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74HC/HCT7245

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A _n	0.33
B _n	0.33
\overline{OE}	1.50
DIR	1.00

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are referred to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} (V)	WAVEFORMS	
		+25		-40 to +85		-40 to +125					
min.	typ.	max.	min.	max.	min.	max.					
V _{T+}	positive-going threshold			2.0 2.1		2.0 2.1		2.0 2.1	V	4.5 5.5	Figs. 4 and 5
V _{T-}	negative-going threshold	0.7 0.8			0.64 0.74		0.6 0.7		V	4.5 5.5	Figs. 4 and 5
V _H	hysteresis (V _{T+} - V _{T-})	0.17 0.17	0.23 0.23						V	4.5 5.5	Figs. 4 and 5

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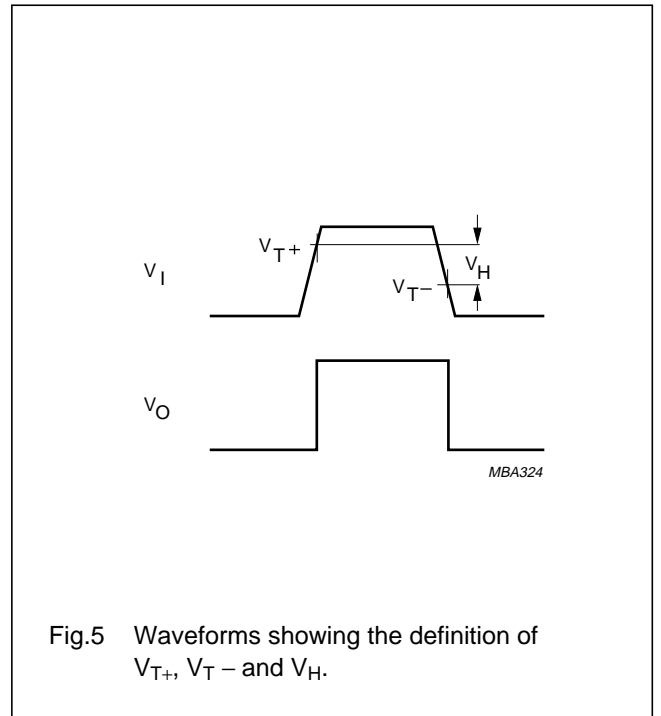
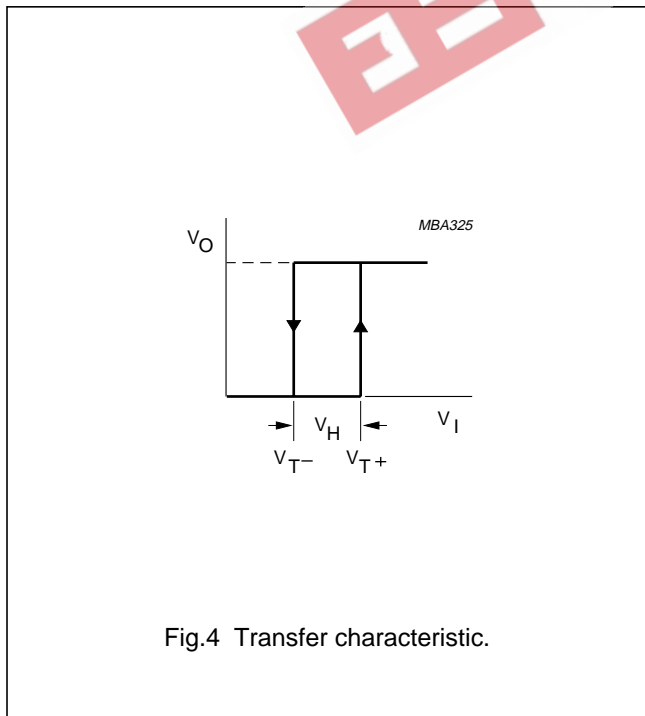
74HC/HCT7245

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n ; B_n to A_n		17	30		37		45	ns	4.5	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time \overline{OE} to A_n ; \overline{OE} to B_n		19	32		40		48	ns	4.5	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time \overline{OE} to A_n ; \overline{OE} to B_n		19	32		40		48	ns	4.5	Fig.7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.7

TRANSFER CHARACTERISTIC WAVEFORMS



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74HC/HCT7245

AC WAVEFORMS

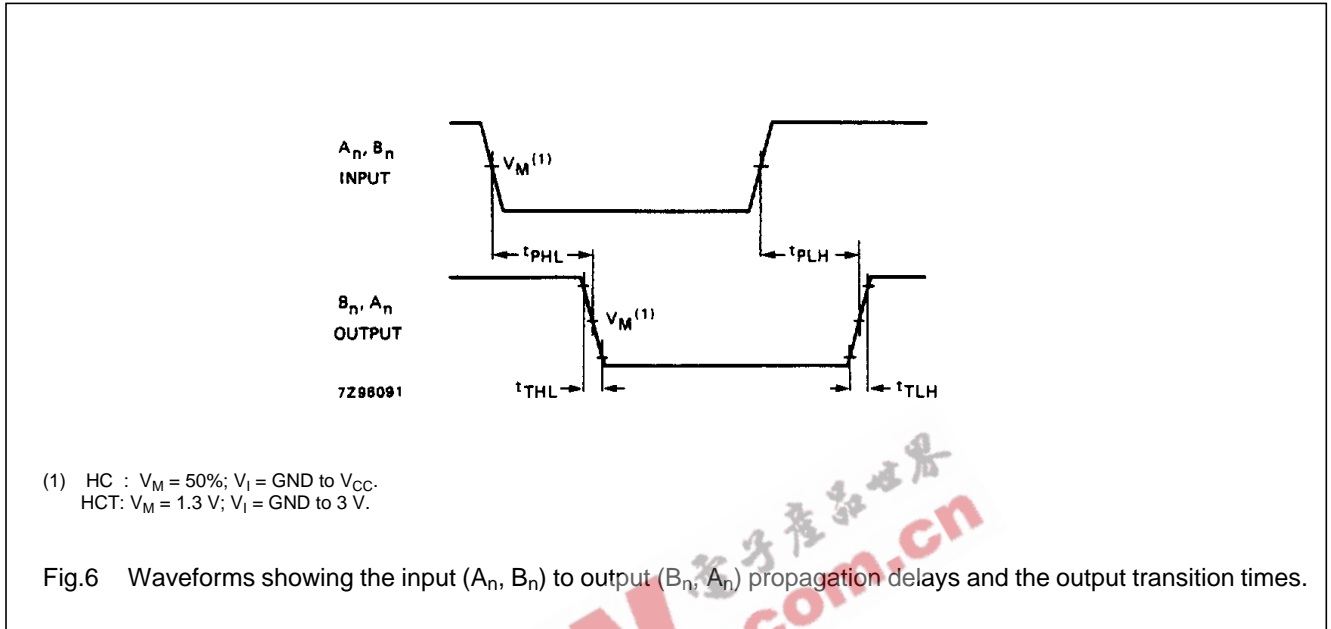


Fig.6 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

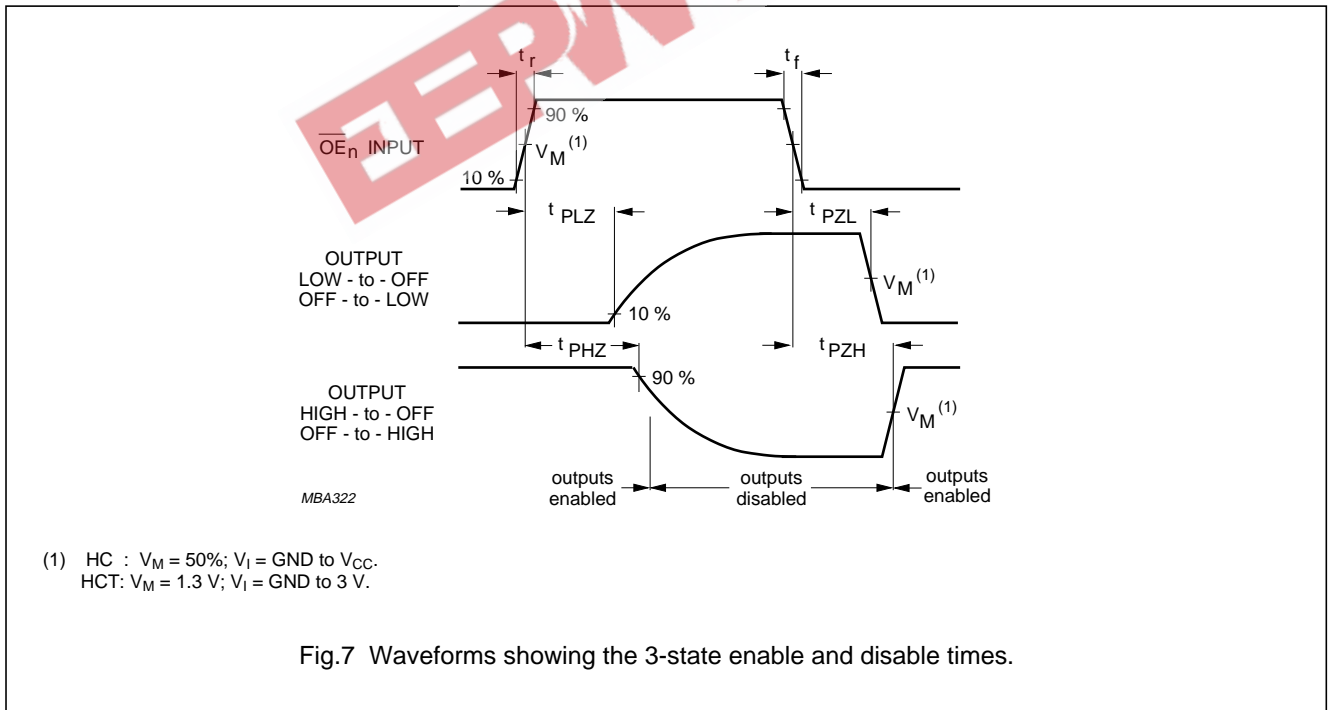


Fig.7 Waveforms showing the 3-state enable and disable times.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".