

# DATA SHEET

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## 74LVT543

3.3V Octal latched transceiver with  
dual enable (3-State)

Product specification  
Supersedes data of 1994 May 20  
IC23 Data Handbook

1998 Feb 19

# 3.3V Octal latched transceiver with dual enable (3-State)

74LVT543

## FEATURES

- Combines 74LVT245 and 74LVT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

## DESCRIPTION

The 74LVT543 is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3V.

This device contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable (LEAB, LEBA) and Output Enable (OEAB, OEBA) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

## FUNCTIONAL DESCRIPTION

The 74LVT543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable (EAB) input and the A-to-B Latch Enable (LEAB) input are Low the A-to-B path is transparent. A subsequent Low-to-High transition of the LEAB signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With EAB and OEAB both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the EBA, LEBA, and OEBA inputs.

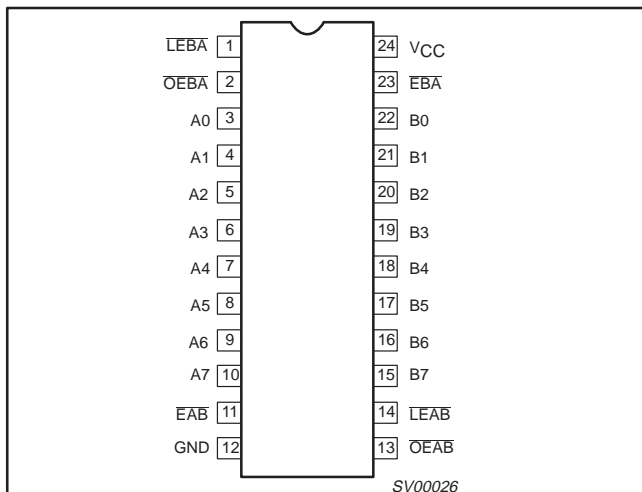
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C; GND = 0V$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Bn or Bn to An	$C_L = 50pF;$ $V_{CC} = 3.3V$	2.3 3.0	ns
$C_{IN}$	Input capacitance	$V_I = 0V$ or $3.0V$	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_{I/O} = 0V$ or $3.0V$	10	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 3.6V$	0.13	mA

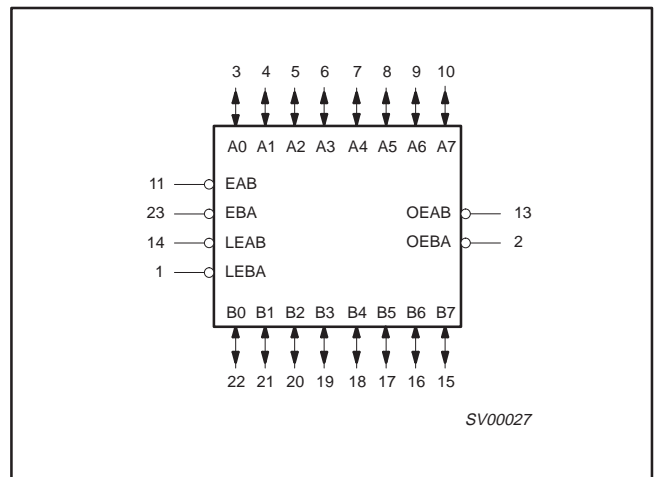
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic SOL	-40°C to +85°C	74LVT543 D	74LVT543 D	SOT137-1
24-Pin Plastic SSOP Type II	-40°C to +85°C	74LVT543 DB	74LVT543 DB	SOT340-1
24-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVT543 PW	74LVT543PW DH	SOT355-1

## PIN CONFIGURATION



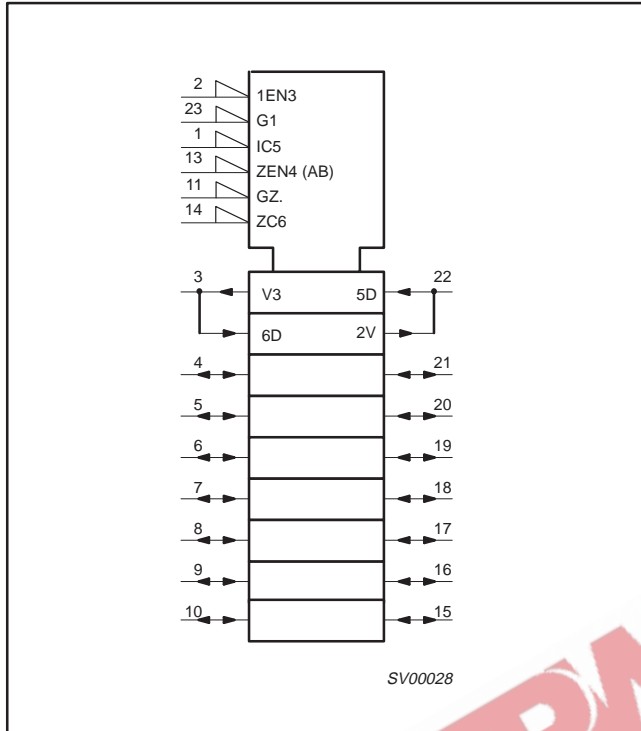
## LOGIC SYMBOL



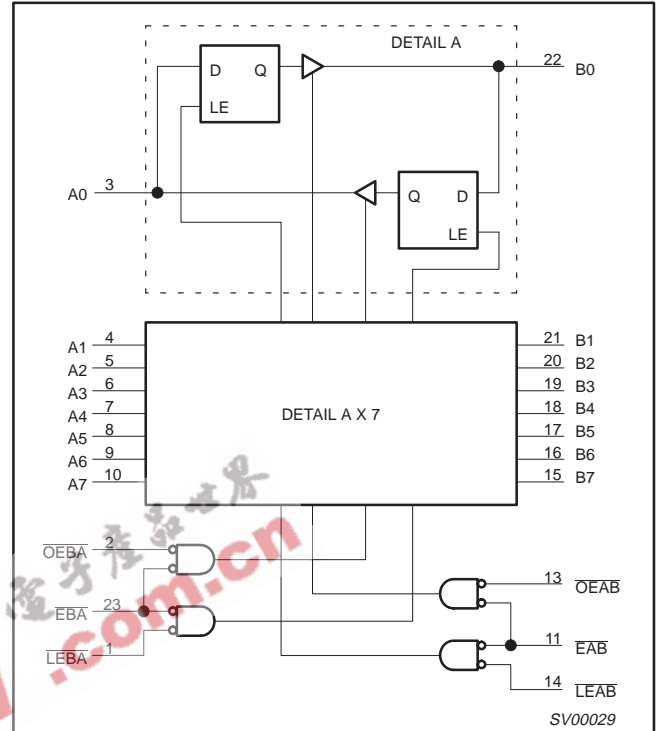
# 3.3V Octal latched transceiver with dual enable (3-State)

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## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
14, 1	$\overline{LEAB} / \overline{LEBA}$	A to B / B to A Latch Enable input (active-Low)
11, 23	$\overline{EAB} / \overline{EBA}$	A to B / B to A Enable input (active-Low)
13, 2	$\overline{OEAB} / \overline{OEBA}$	A to B / B to A Output Enable input (active-Low)
3, 4, 5, 6, 7, 8, 9, 10	A0 – A7	Port A, 3-State outputs
22, 21, 20, 19, 18, 17, 16, 15	B0 – B7	Port B, 3-State outputs
12	GND	Ground (0V)
24	V <sub>CC</sub>	Positive supply voltage

## FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
OEXX	EXX	LEXX	An or Bn	Bn or An	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L	↑	L	h	Z	Disabled + Latch
L	↑	L	l	Z	
L	L	↑	h	H	Latch + Display
L	L	↑	l	L	
L	L	L	H	H	Transparent
L	L	L	L	L	
L	L	H	X	NC	Hold

H = High voltage level  
 h = High voltage level one set-up time prior to the Low-to-High transition of LEXX or EXX (XX = AB or BA)  
 L = Low voltage level  
 l = Low voltage level one set-up time prior to the Low-to-High transition of LEXX or EXX (XX = AB or BA)

X = Don't care  
 ↑ = Low-to-High transition of LEXX or EXX (XX = AB or BA)  
 NC = No change  
 Z = High impedance or "off" state

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### ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +4.6	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$	-50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +7.0	V
$I_{OUT}$	DC output current	Output in Low state	128	mA
		Output in High state	-64	
$T_{stg}$	Storage temperature range		-65 to 150	°C

#### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	2.7	3.6	V
$V_I$	Input voltage	0	5.5	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Low-level input voltage		0.8	V
$I_{OH}$	High-level output current		-32	mA
$I_{OL}$	Low-level output current		32	mA
	Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1$ kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

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### DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 2.7V; I <sub>IK</sub> = -18mA		-0.9	-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 2.7 to 3.6V; I <sub>OH</sub> = -100μA	V <sub>CC</sub> -0.2	V <sub>CC</sub> -0.1		V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -8mA	2.4	2.5		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -32mA	2.0	2.2		
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 100μA		0.1	0.2	V
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 24mA		0.3	0.5	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 16mA		0.25	0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 32mA		0.3	0.5	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 64mA		0.4	0.55	
V <sub>RST</sub>	Power-up output low voltage <sup>5</sup>	V <sub>CC</sub> = 3.6V; I <sub>O</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>		0.13	0.55	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins	±0.1	±1	μA
		V <sub>CC</sub> = 0 or 3.6V; V <sub>I</sub> = 5.5V		1	10	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V	I/O Data pins <sup>4</sup>	1	20	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub>		0.1	1	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 0		-1	-5	
I <sub>OFF</sub>	Output off current	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5V		1	±100	μA
I <sub>HOLD</sub>	Bus Hold current A inputs <sup>6</sup>	V <sub>CC</sub> = 3V; V <sub>I</sub> = 0.8V	75	150		μA
		V <sub>CC</sub> = 3V; V <sub>I</sub> = 2.0V	-75	-150		
		V <sub>CC</sub> = 0V to 3.6V; V <sub>CC</sub> = 3.6V	±500			
I <sub>EX</sub>	Current into an output in the High state when V <sub>O</sub> > V <sub>CC</sub>	V <sub>O</sub> = 5.5V; V <sub>CC</sub> = 3.0V		60	125	μA
I <sub>PU/PD</sub>	Power up/down 3-State output current <sup>3</sup>	V <sub>CC</sub> ≤ 1.2V; V <sub>O</sub> = 0.5V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; OE/OE = Don't care		15	±100	μA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		0.13	0.19	mA
I <sub>CCL</sub>		V <sub>CC</sub> = 3.6V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		3	12	
I <sub>CCZ</sub>		V <sub>CC</sub> = 3.6V; Outputs Disabled; V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		0.13	0.19	
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 3V to 3.6V; One input at V <sub>CC</sub> - 0.6V, Other inputs at V <sub>CC</sub> or GND		0.1	0.2	mA

#### NOTES:

- All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND
- This parameter is valid for any V<sub>CC</sub> between 0V and 1.2V with a transition time of up to 10msec. From V<sub>CC</sub> = 1.2V to V<sub>CC</sub> = 3.3V ± 0.3V a transition time of 100μsec is permitted. This parameter is valid for T<sub>amb</sub> = 25°C only.
- Unused pins at V<sub>CC</sub> or GND.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

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## AC CHARACTERISTICS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP <sup>1</sup>	MAX	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Bn, Bn to An	2	1.0 1.0	2.3 3.0	4.7 4.6	5.5 5.8	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	1 2	1.0 1.0	3.6 4.2	5.9 5.7	7.3 7.3	ns
$t_{PZH}$ $t_{PZL}$	Output enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	4 5	1.0 1.1	3.8 3.8	5.8 6.4	7.6 8.2	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	4 5	2.4 2.0	3.7 3.5	6.5 5.8	7.1 5.9	ns
$t_{PZH}$ $t_{PZL}$	Output enable time EBA to An, $\overline{EAB}$ to Bn	4 5	1.0 1.4	4.0 4.1	6.0 6.7	7.6 8.3	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time EBA to An, $\overline{EAB}$ to Bn	4 5	2.3 2.0	3.7 3.5	6.4 5.4	7.1 5.6	ns

**NOTE:**

1. All typical values are at  $V_{CC} = 3.3V$  and  $T_{\text{amb}} = 25^\circ\text{C}$ .

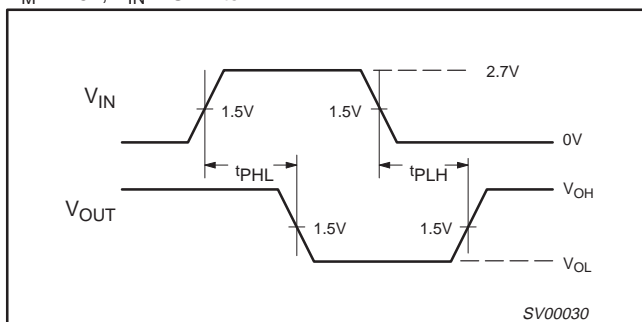
## AC SETUP REQUIREMENTS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

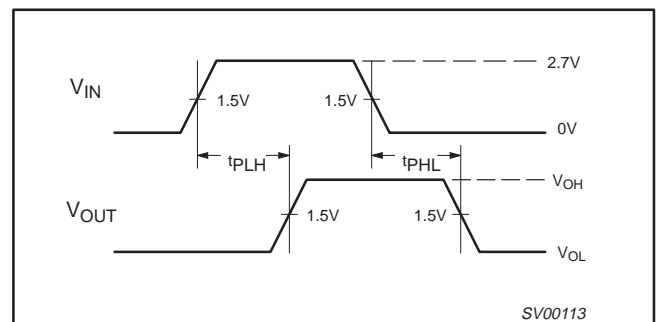
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$	
			MIN	MAX	MIN	
$t_s(H)$ $t_s(L)$	Setup time An to $\overline{LEAB}$ , Bn to $\overline{LEBA}$	3	0 0.8		0 1.1	ns
$t_h(H)$ $t_h(L)$	Hold time An to $\overline{LEAB}$ , Bn to $\overline{LEBA}$	3	1.7 1.7		1.7 1.7	ns
$t_s(H)$ $t_s(L)$	Setup time An to $\overline{EAB}$ , Bn to $\overline{EBA}$	3	0 0.9		0 1.2	ns
$t_h(H)$ $t_h(L)$	Hold time An to $\overline{EAB}$ , Bn to $\overline{EBA}$	3	1.8 1.8		1.8 1.8	ns
$t_w(L)$	Latch enable pulse width, Low	3	3.3		3.3	ns

## AC WAVEFORMS

$V_M = 1.5V$ ,  $V_{IN} = \text{GND to } 2.7V$



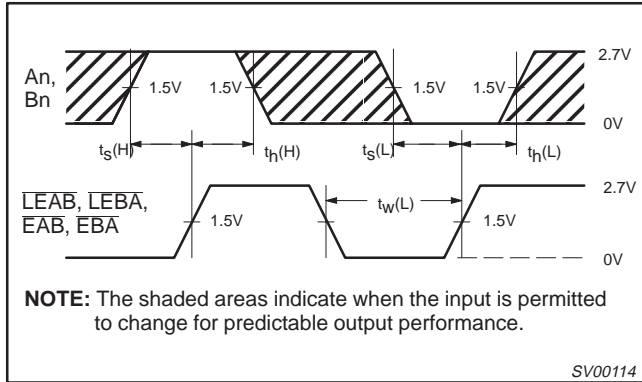
Waveform 1. Propagation Delay For Inverting Output



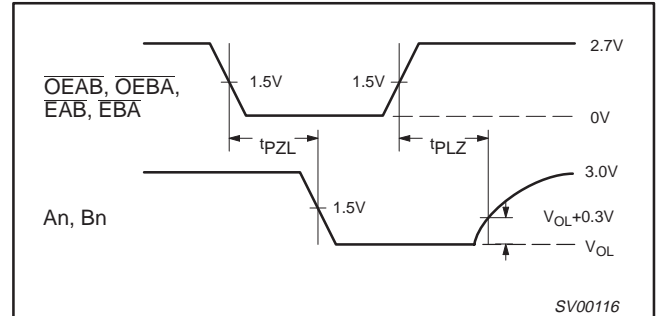
Waveform 2. Propagation Delay For Non-Inverting Output

# 3.3V Octal latched transceiver with dual enable (3-State)

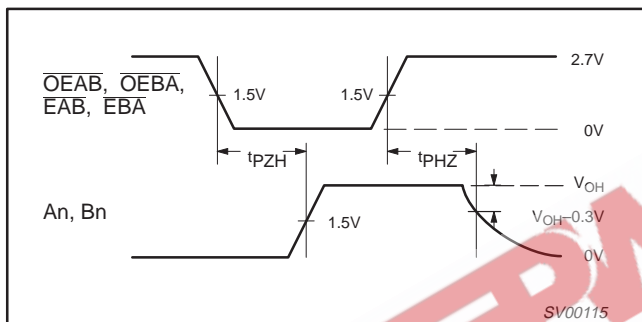
74LVT543



**Waveform 3. Data Setup and Hold Times And Latch Enable Pulse Width**



**Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**



**Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level**

## TEST CIRCUIT AND WAVEFORM

Test Circuit for 3-State Outputs

$V_M = 1.5V$   
Input Pulse Definition

**SWITCH POSITION**

TEST	SWITCH
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6V
$t_{PHZ}/t_{PZH}$	GND

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_w$	$t_R$	$t_F$
74LVT	2.7V	$\leq 10\text{MHz}$	500ns	$\leq 2.5\text{ns}$	$\leq 2.5\text{ns}$

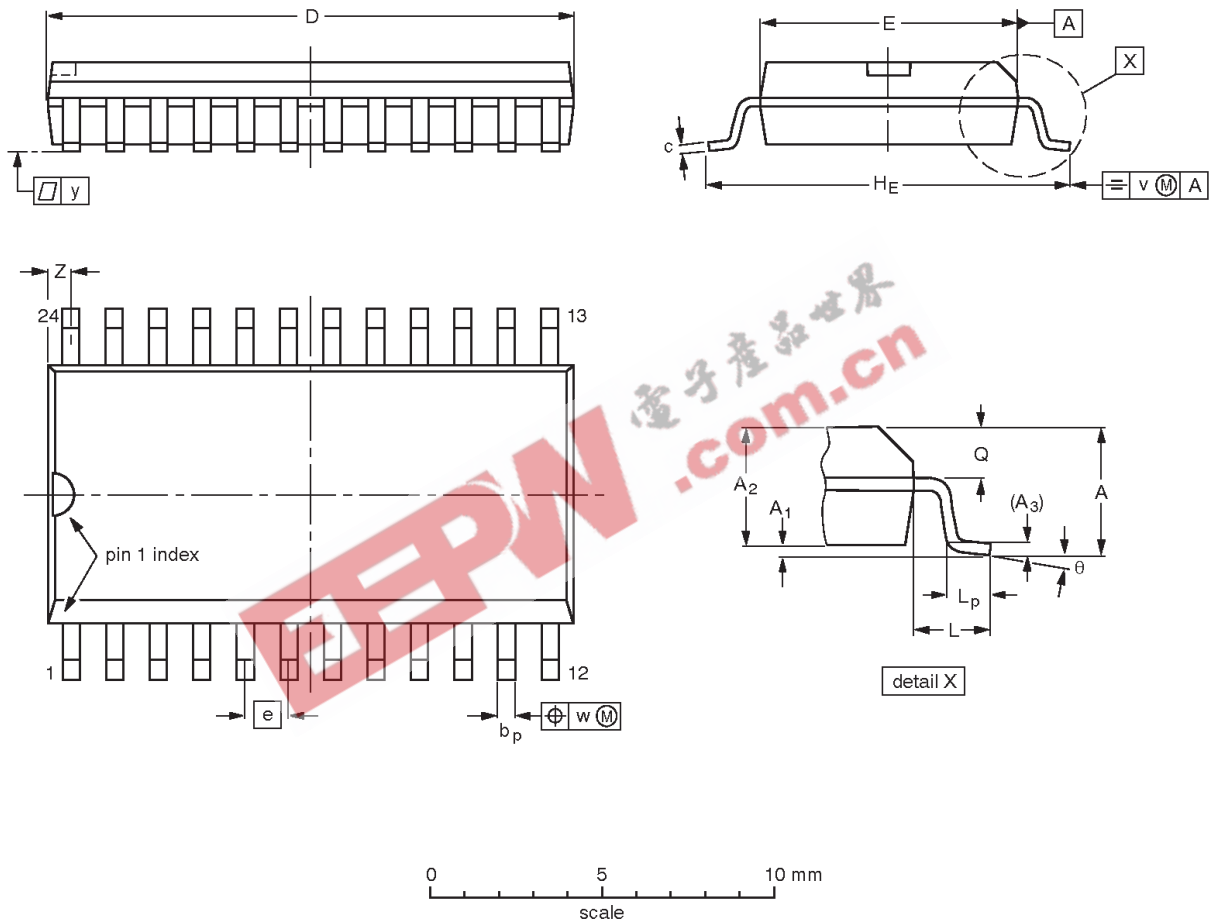
SV00092

3.3V Octal latched transceiver with dual enable  
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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

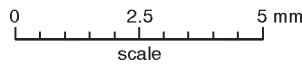
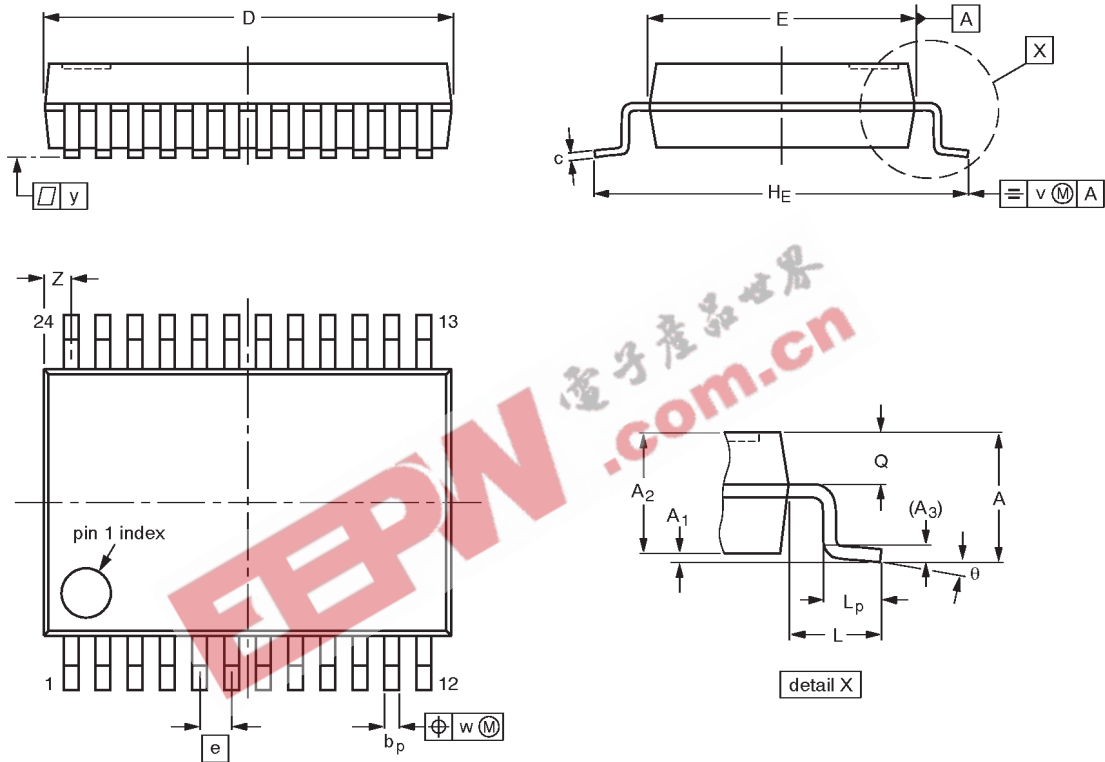


3.3V Octal latched transceiver with dual enable  
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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

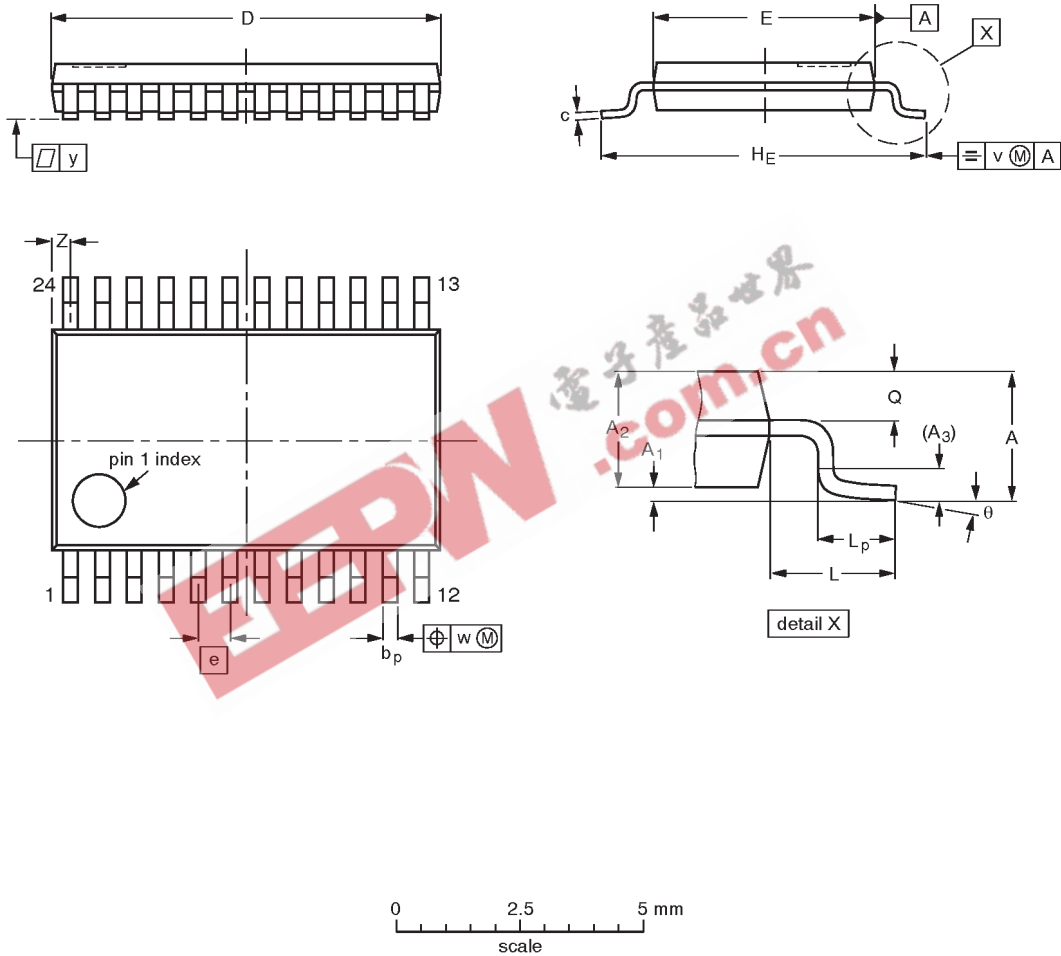
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08 95-02-04

3.3V Octal latched transceiver with dual enable  
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TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



**DIMENSIONS** (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				93-06-16 95-02-04

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3.3V Octal latched transceiver with dual enable  
(3-State)

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NOTES



# 3.3V Octal latched transceiver with dual enable (3-State)

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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