FAIRCHILD SEMICONDUCTOR™

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# 74LVXC4245
# 8-Bit Dual Supply Configurable Voltage Interface Transceiver with 3-STATE Outputs

## General Description

The LVXC4245 is a 24-pin dual-supply, 8-bit configurable voltage interface transceiver suited for PCMCIA and other real time configurable I/O applications. The $V_{CCA}$ pin accepts a 5V supply level. The "A" Port is a dedicated 5V port. The $V_{CCB}$ pin accepts a 3V-to-5V supply level. The "B" Port is configured to track the $V_{CCB}$ supply level respectively. A 5V level on the $V_{CC}$ pin will configure the I/O pins at a 5V level and a 3V $V_{CC}$ will configure the I/O pins at a 3V level. This device will allow the $V_{CCB}$ voltage source pin and I/O pins on the "B" Port to float when $\overline{OE}$ is HIGH. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation.

## Features

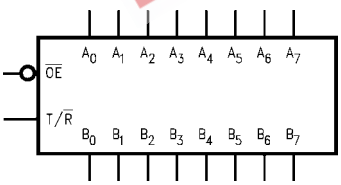
- Bidirectional interface between 5V and 3V-to-5V buses
- Control inputs compatible with TTL level
- Outputs source/sink up to 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Implements patented EMI reduction circuitry
- Flexible $V_{CCB}$ operating range
- Allows B Port and $V_{CCB}$ to float simultaneously when $\overline{OE}$ is HIGH
- Functionally compatible with the 74 series 245

## Ordering Code:

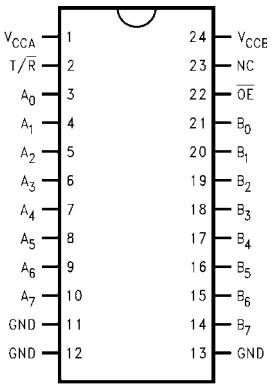
| Order Number | Package Number | Package Description |
|---|---|---|
| 74LVXC4245WM | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74LVXC4245QSC | MQA24 | 24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide |
| 74LVXC4245MTC | MTC24 | 24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Logic Symbol




## Connection Diagram




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OE}$ | Output Enable Input |
| T/$\overline{R}$ | Transmit/Receive Input |
| $A_0$–$A_7$ | Side A Inputs or 3-STATE Outputs |
| $B_0$–$B_7$ | Side B Inputs or 3-STATE Outputs |

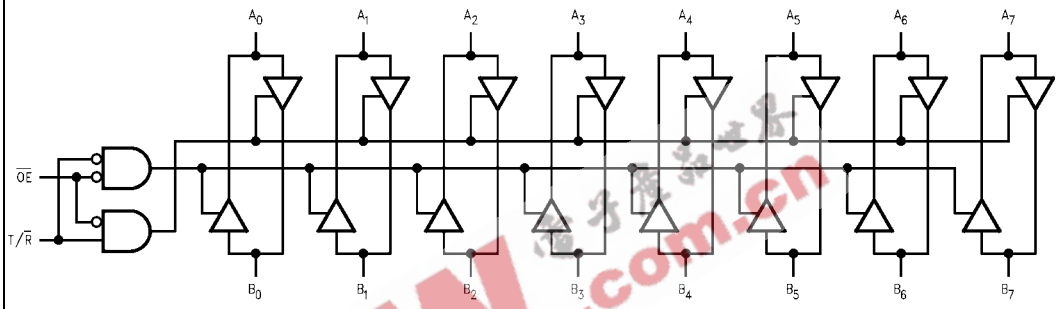
 

## Truth Table

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}$ | T/$\overline{R}$ | |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | HIGH-Z State |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

## Logic Diagram



## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CCA}$,$V_{CCB}$) | −0.5V to +7.0V |
| DC Input Voltage ($V_I$) @ $\overline{OE}$, T/$\overline{R}$ | −0.5V to $V_{CCA}$ +0.5V |
| DC Input/Output Voltage ($V_{I/O}$) | |
| @ $A_n$ | −0.5V to $V_{CCA}$ +0.5V |
| @ $B_n$ | −0.5V to $V_{CCB}$ +0.5V |
| DC Input Diode Current ($I_{IK}$) | |
| @ $\overline{OE}$, T/$\overline{R}$ | ±20 mA |
| DC Output Diode Current ($I_{OK}$) | ±50 mA |
| DC Output Source or | |
| Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current | |
| Per Output Pin ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| and Max Current | ±200 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| DC Latch-Up Source or | |
| Sink Current | ±300 mA |

## Recommended Operating Conditions (Note 2)

| | |
|---|---|
| Supply Voltage $V_{CCA}$ | 4.5V to 5.5V |
| $V_{CCB}$ | 2.7V to 5.5V |
| Input Voltage ($V_I$) @ $\overline{OE}$, T/$\overline{R}$ | 0V to $V_{CCA}$ |
| Input/Output Voltage ($V_{I/O}$) | |
| @$A_n$ | 0V to $V_{CCA}$ |
| @$B_n$ | 0V to $V_{CCB}$ |
| Free Air Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate (ΔV/Δt) | 8 ns/V |
| $V_{IN}$ from 30% to 70% of $V_{CC}$ | |
| $V_{CC}$ @ 3V, 4.5V, 5.5V | |

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** The A Port unused pins (inputs and I/O's) must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | | $V_{CCA}$ (V) | $V_{CCB}$ (V) | $T_A$ = +25°C Typ | $T_A$ = −40°C to +85°C Guaranteed Limits | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IHA}$ | Minimum HIGH Level Input Voltage | $A_n$ | 4.5 | 2.7 | | 2.0 | 2.0 | V | $V_{OUT} \le 0.1V$ or $\ge V_{CC} - 0.1V$ |
| | | $\overline{OE}$ | 4.5 | 3.6 | | 2.0 | 2.0 | | |
| | | T/$\overline{R}$ | 5.5 | 5.5 | | 2.0 | 2.0 | | |
| $V_{IHB}$ | | $B_n$ | 4.5 | 2.7 | | 2.0 | 2.0 | | |
| | | | 4.5 | 3.6 | | 2.0 | 2.0 | | |
| | | | 4.5 | 5.5 | | 3.85 | 3.85 | | |
| $V_{ILA}$ | Maximum LOW Level Input Voltage | $A_n$ | 4.5 | 2.7 | | 0.8 | 0.8 | V | $V_{OUT} \le 0.1V$ or $\ge V_{CC} - 0.1V$ |
| | | $\overline{OE}$ | 4.5 | 3.6 | | 0.8 | 0.8 | | |
| | | T/$\overline{R}$ | 5.5 | 5.5 | | 0.8 | 0.8 | | |
| $V_{ILB}$ | | $B_n$ | 4.5 | 2.7 | | 0.8 | 0.8 | | |
| | | | 4.5 | 3.6 | | 0.8 | 0.8 | | |
| | | | 4.5 | 5.5 | | 1.65 | 1.65 | | |
| $V_{OHA}$ | Minimum HIGH Level Output Voltage | | 4.5 | 3.0 | 4.49 | 4.4 | 4.4 | V | $I_{OUT}$ = −100 µA |
| | | | 4.5 | 3.0 | 4.25 | 3.86 | 3.76 | | $I_{OH}$ = −24 mA |
| $V_{OHB}$ | | | 4.5 | 3.0 | 2.99 | 2.9 | 2.9 | V | $I_{OUT}$ = −100 µA |
| | | | 4.5 | 3.0 | 2.85 | 2.56 | 2.46 | | $I_{OH}$ = −12 mA |
| | | | 4.5 | 3.0 | 2.65 | 2.35 | 2.25 | | $I_{OH}$ = −24 mA |
| | | | 4.5 | 2.7 | 2.5 | 2.3 | 2.2 | | $I_{OH}$ = −12 mA |
| | | | 4.5 | 2.7 | 2.3 | 2.1 | 2.0 | | $I_{OH}$ = −24 mA |
| | | | 4.5 | 4.5 | 4.25 | 3.86 | 3.76 | | $I_{OH}$ = −24 mA |
| $V_{OLA}$ | Maximum LOW Level Output Voltage | | 4.5 | 3.0 | 0.002 | 0.1 | 0.1 | V | $I_{OUT}$ = 100 µA |
| | | | 4.5 | 3.0 | 0.21 | 0.36 | 0.44 | | $I_{OL}$ = 24 mA |
| $V_{OLB}$ | | | 4.5 | 3.0 | 0.002 | 0.1 | 0.1 | V | $I_{OUT}$ = 100 µA |
| | | | 4.5 | 3.0 | 0.21 | 0.36 | 0.44 | | $I_{OL}$ = 24 mA |
| | | | 4.5 | 2.7 | 0.11 | 0.36 | 0.44 | | $I_{OL}$ = 12 mA |
| | | | 4.5 | 2.7 | 0.22 | 0.42 | 0.5 | | $I_{OL}$ = 24 mA |
| | | | 4.5 | 4.5 | 0.18 | 0.36 | 0.44 | | $I_{OL}$ = 24 mA |
| $I_{IN}$ | Maximum Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$ | | 5.5 | 3.6 | | ±0.1 | ±1.0 | µA | $V_I = V_{CCA}$, GND |
| | | | 5.5 | 5.5 | | ±0.1 | ±1.0 | | |

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | | $V_{CCA}$ (V) | $V_{CCB}$ (V) | $T_A = +25°C$ Typ | $T_A = +25°C$ Guaranteed Limits | $T_A = -40°C$ to $+85°C$ Guaranteed Limits | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $I_{OZA}$ | Maximum 3-STATE Output Leakage @ $A_n$ | | 5.5<br>5.5 | 3.6<br>5.5 | | ±0.5<br>±0.5 | ±5.0<br>±5.0 | µA | $V_I = V_{IL}$, $V_{IH}$, $\overline{OE} = V_{CCA}$<br>$V_O = V_{CCA}$, GND |
| $I_{OZB}$ | Maximum 3-STATE Output Leakage @ $B_n$ | | 5.5<br>5.5 | 3.6<br>5.5 | | ±0.5<br>±0.5 | ±5.0<br>±5.0 | µA | $V_I = V_{IL}$, $V_{IH}$, $\overline{OE} = V_{CCA}$<br>$V_O = V_{CCB}$, GND |
| $\Delta I_{CC}$ | Maximum | All Inputs | 5.5 | 5.5 | 1.0 | 1.35 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ |
| | $I_{CC}$/Input | $B_n$ | 5.5 | 3.6 | | 0.35 | 0.5 | mA | $V_I = V_{CCB} - 0.6V$ |
| $I_{CCA1}$ | Quiescent $V_{CCA}$ Supply Current as B Port Floats | | 5.5 | Open | | 8 | 80 | µA | $A_n = V_{CCA}$ or GND<br>$B_n$ = Open, $\overline{OE} = V_{CCA}$<br>$T/\overline{R} = V_{CCA}$, $V_{CCB}$ = Open |
| $I_{CCA2}$ | Quiescent $V_{CCA}$ Supply Current | | 5.5<br>5.5 | 3.6<br>5.5 | | 8<br>8 | 80<br>80 | µA | $A_n = V_{CCA}$ or GND<br>$B_n = V_{CCB}$ or GND<br>$\overline{OE}$ = GND, $T/\overline{R}$ = GND |
| $I_{CCB}$ | Quiescent $V_{CCB}$ Supply Current | | 5.5<br>5.5 | 3.6<br>5.5 | | 5<br>8 | 50<br>80 | µA | $A_n = V_{CCA}$ or GND<br>$B_n = V_{CCB}$ or GND<br>$\overline{OE}$ = GND, $T/\overline{R} = V_{CCA}$ |
| $V_{OLPA}$ | Quiet Output Maximum Dynamic | | 5.0<br>5.0 | 3.3<br>5.0 | | 1.5<br>1.5 | | V | (Note 3) (Note 4) |
| $V_{OLPB}$ | $V_{OL}$ | | 5.0<br>5.0 | 3.3<br>5.0 | | 0.8<br>1.5 | | V | (Note 3) (Note 4) |
| $V_{OLVA}$ | Quiet Output Minimum Dynamic $V_{OL}$ | | 5.0<br>5.0 | 3.3<br>5.0 | | –1.2<br>–1.2 | | V | (Note 3) (Note 4) |
| $V_{OLVB}$ | | | 5.0<br>5.0 | 3.3<br>5.0 | | –0.8<br>–1.2 | | V | (Note 3) (Note 4) |
| $V_{IHDA}$ | Minimum HIGH Level Dynamic Input | | 5.0<br>5.0 | 3.3<br>5.0 | | 2.0<br>2.0 | | V | (Note 3) (Note 5) |
| $V_{IHDB}$ | Voltage | | 5.0<br>5.0 | 3.3<br>5.0 | | 2.0<br>3.5 | | V | (Note 3) (Note 5) |
| $V_{ILDA}$ | Maximum LOW Level Dynamic Input | | 5.0<br>5.0 | 3.3<br>5.0 | | 0.8<br>0.8 | | V | (Note 3) (Note 5) |
| $V_{ILDB}$ | Voltage | | 5.0<br>5.0 | 3.3<br>5.0 | | 0.8<br>1.5 | | V | (Note 3) (Note 5) |

**Note 3:** Worst case package.

**Note 4:** Max number of outputs defined as (n). Data inputs are driven 0V to $V_{CC}$ level; one output at GND.

**Note 5:** Max number of Data Inputs (n) switching. (n–1) inputs switching 0V to $V_{CC}$ level. Input-under-test switching: $V_{CC}$ level to threshold ($V_{IHD}$), 0V to threshold ($V_{ILD}$), f = 1 MHz.

## AC Electrical Characteristics

| Symbol | Parameter | $C_L$ = 50 pF, $V_{CCA}$ = 4.5V to 5.5V, $V_{CCB}$ = 4.5V to 5.5V | | | | | $C_L$ = 50 pF, $V_{CCA}$ = 4.5V to 5.5V, $V_{CCB}$ = 2.7V to 3.6V | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $T_A$ = +25°C | | | $T_A$ = −40°C to +85°C | | $T_A$ = +25°C | | | $T_A$ = −40°C to +85°C | | |
| | | Min | Typ (Note 6) | Max | Min | Max | Min | Typ (Note 7) | Max | Min | Max | |
| $t_{PHL}$ | Propagation | 1.0 | 4.9 | 6.5 | 1.0 | 7.0 | 1.0 | 5.5 | 7.5 | 1.0 | 8.0 | ns |
| $t_{PLH}$ | Delay A to B | 1.0 | 4.0 | 5.5 | 1.0 | 6.0 | 1.0 | 5.0 | 7.0 | 1.0 | 7.5 | |
| $t_{PHL}$ | Propagation | 1.0 | 4.7 | 6.5 | 1.0 | 7.0 | 1.0 | 5.6 | 7.5 | 1.0 | 8.0 | ns |
| $t_{PLH}$ | Delay B to A | 1.0 | 3.9 | 5.0 | 1.0 | 5.5 | 1.0 | 4.3 | 6.0 | 1.0 | 6.5 | |
| $t_{PZL}$ | Output Enable | 1.0 | 5.6 | 7.5 | 1.0 | 8.0 | 1.0 | 6.7 | 9.0 | 1.0 | 10.0 | ns |
| $t_{PZH}$ | Time $\overline{OE}$ to B | 1.0 | 5.7 | 7.5 | 1.0 | 8.0 | 1.0 | 6.9 | 9.5 | 1.0 | 10.0 | |
| $t_{PZL}$ | Output Enable | 1.0 | 7.4 | 9.0 | 1.0 | 10.0 | 1.0 | 8.0 | 10.0 | 1.0 | 11.0 | ns |
| $t_{PZH}$ | Time $\overline{OE}$ to A | 1.0 | 6.1 | 7.5 | 1.0 | 8.5 | 1.0 | 6.3 | 8.0 | 1.0 | 8.5 | |
| $t_{PHZ}$ | Output Disable | 1.0 | 4.8 | 7.0 | 1.0 | 7.5 | 1.0 | 6.0 | 9.0 | 1.0 | 9.5 | ns |
| $t_{PLZ}$ | Time $\overline{OE}$ to B | 1.0 | 3.8 | 5.5 | 1.0 | 6.0 | 1.0 | 4.2 | 6.5 | 1.0 | 7.0 | |
| $t_{PHZ}$ | Output Disable | 1.0 | 3.4 | 5.5 | 1.0 | 6.0 | 1.0 | 3.4 | 5.5 | 1.0 | 6.0 | ns |
| $t_{PLZ}$ | Time $\overline{OE}$ to A | 1.0 | 2.9 | 4.5 | 1.0 | 5.0 | 1.0 | 2.9 | 5.0 | 1.0 | 5.5 | |
| $t_{OSHL}$ | Output to Output | | | | | | | | | | | ns |
| $t_{OSLH}$ | Skew (Note 8) | | 1.0 | 1.5 | | 1.5 | | 1.0 | 1.5 | | 1.5 | |
| | Data to Output | | | | | | | | | | | |

**Note 6:** Typical values at $V_{CCA}$ = 5V, $V_{CCB}$ = 5V @25°C.

**Note 7:** Typical values at $V_{CCA}$ = 5V, $V_{CCB}$ = 3.3V @25°C.

**Note 8:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$). Parameter guaranteed by design.

## Capacitance

| Symbol | Parameter | | Typ | Units | Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 4.5 | pF | $V_{CC}$ = Open |
| $C_{I/O}$ | Input/Output Capacitance | | 10 | pF | $V_{CCA}$ = 5V, $V_{CCB}$ = 3.3V |
| $C_{PD}$ | Power Dissipation Capacitance | A→B | 45 | pF | $V_{CCA}$ = 5V |
| | (Note 9) | B→A | 50 | pF | $V_{CCB}$ = 3.3V |

**Note 9:** $C_{PD}$ is measured at 10 MHz.

## Power Up Considerations

To insure the system does not experience unnecessary $I_{CC}$ current draw, bus contention, or oscillations during power up, the following guidelines should be adhered to (refer to Table 1):

- Power up the control side of the device first. This is the $V_{CCA}$.
- $\overline{OE}$ should ramp with or ahead of $V_{CCA}$. This will help guard against bus contention.
- The Transmit/Receive control pin (T/$\overline{R}$) should ramp with $V_{CCA}$, this will ensure that the A Port data pins are configured as inputs. With $V_{CCA}$ receiving power first, the A I/O Port should be configured as inputs to help guard against bus contention and oscillations.
- A side data inputs should be driven to a valid logic level. This will prevent excessive current draw.

The above steps will ensure that no bus contention or oscillations, and therefore no excessive current draw occurs during the power up cycling of these devices. These steps will help prevent possible damage to the translator devices and potential damage to other system components.

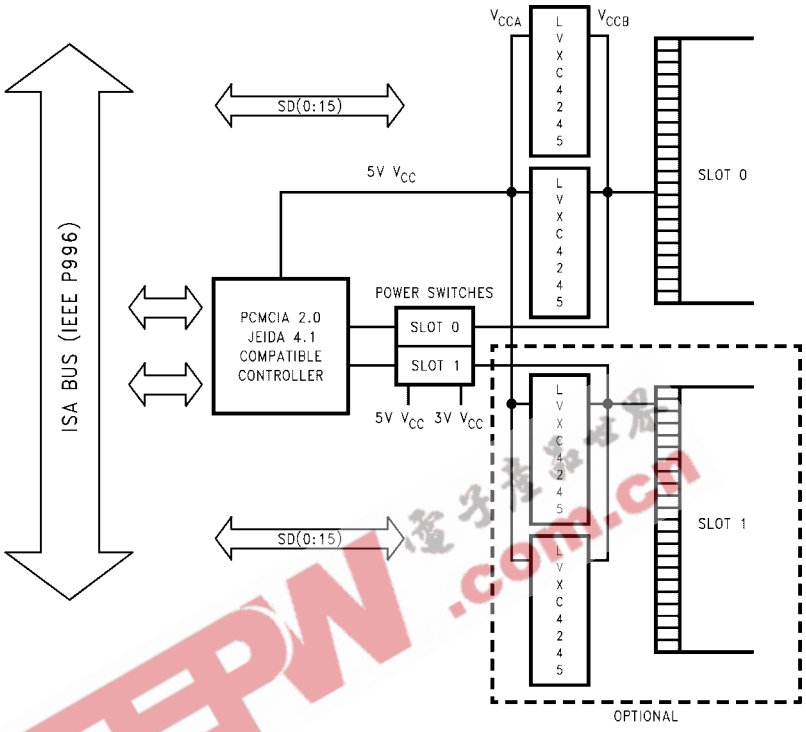
**TABLE 1. Low Voltage Translator Power Up Sequencing Table**

| Device Type | $V_{CCA}$ | $V_{CCB}$ | T/$\overline{R}$ | $\overline{OE}$ | A Side I/O | B Side I/O | Floatable Pin Allowed |
|---|---|---|---|---|---|---|---|
| 74LVXC4245 | 5V (power up 1st) | 2.7V to 5.5V configurable | ramp with $V_{CCA}$ | ramp with $V_{CCA}$ | logic 0V or $V_{CCA}$ | outputs | yes, $V_{CCB}$ and B I/O's w/ $\overline{OE}$ HIGH |

Please reference Application Note AN-5001 for more detailed information on using Fairchild's LVX Low Voltage Dual Supply CMOS Translating Transceivers.

## Configurable I/O Application for PCMCIA Cards

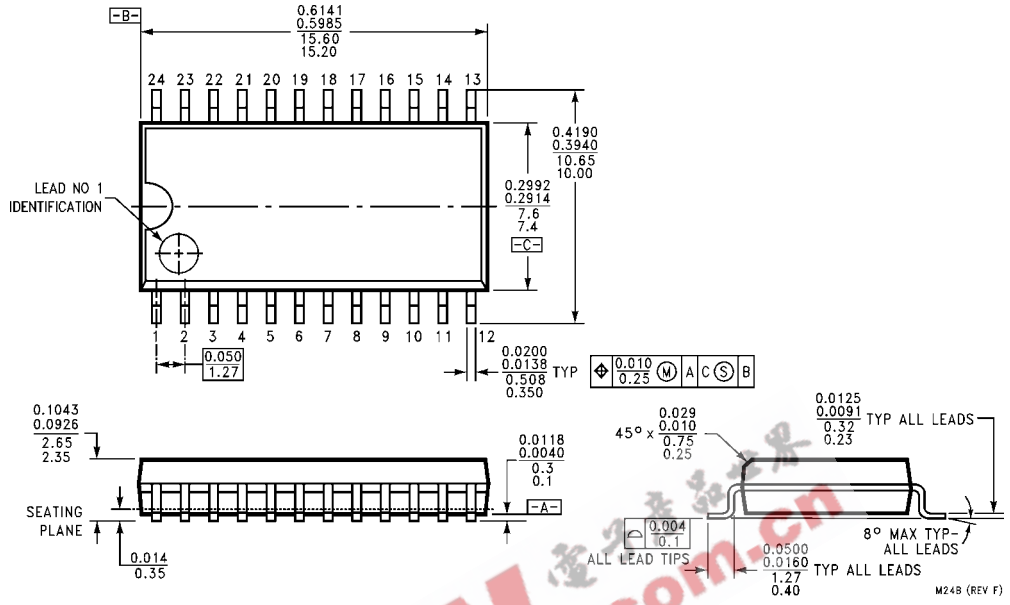
**Block Diagram**



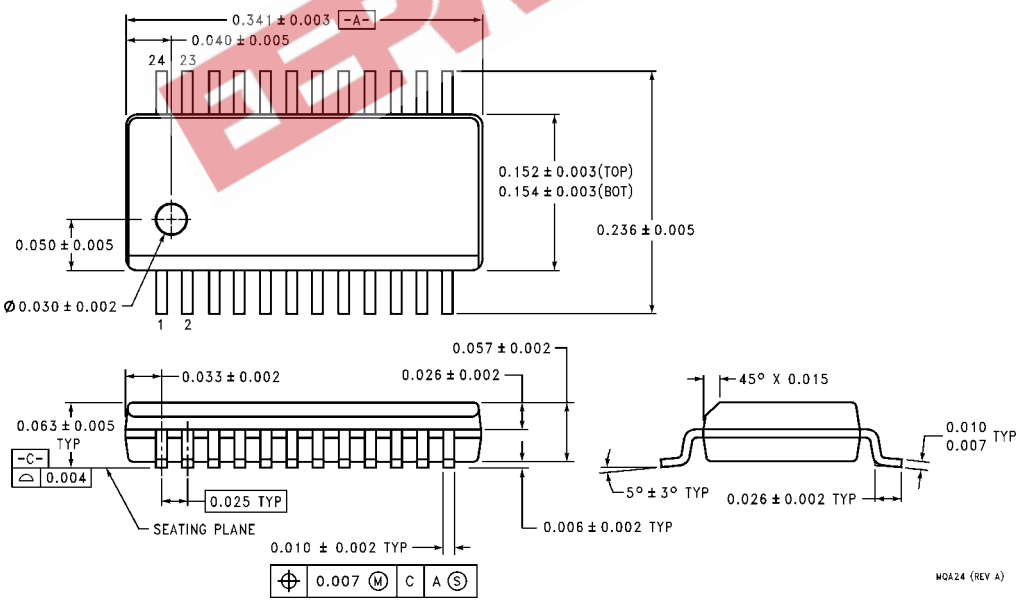

The LVXC4245 is a 24-pin dual supply device well suited for PCMCIA configurable I/O applications. Ideal for low power notebook designs, the LVXC4245 consumes less than 1 mW of quiescent power in all modes of operation. The LVXC4245 meets all PCMCIA I/O voltage requirements at 5V and 3.3V operation. By tying $V_{CCB}$ of the LVXC4245 to the card voltage supply, the PCMCIA card will always experience rail to rail output swings, maximizing the reliability of the interface.

The $V_{CCA}$ pin on the LVXC4245 must always be tied to a 5V power supply. This voltage connection provides internal references needed to account for variations in $V_{CCB}$. When connected as in the block diagram above, the LVXC4245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).

## Physical Dimensions inches (millimeters) unless otherwise noted

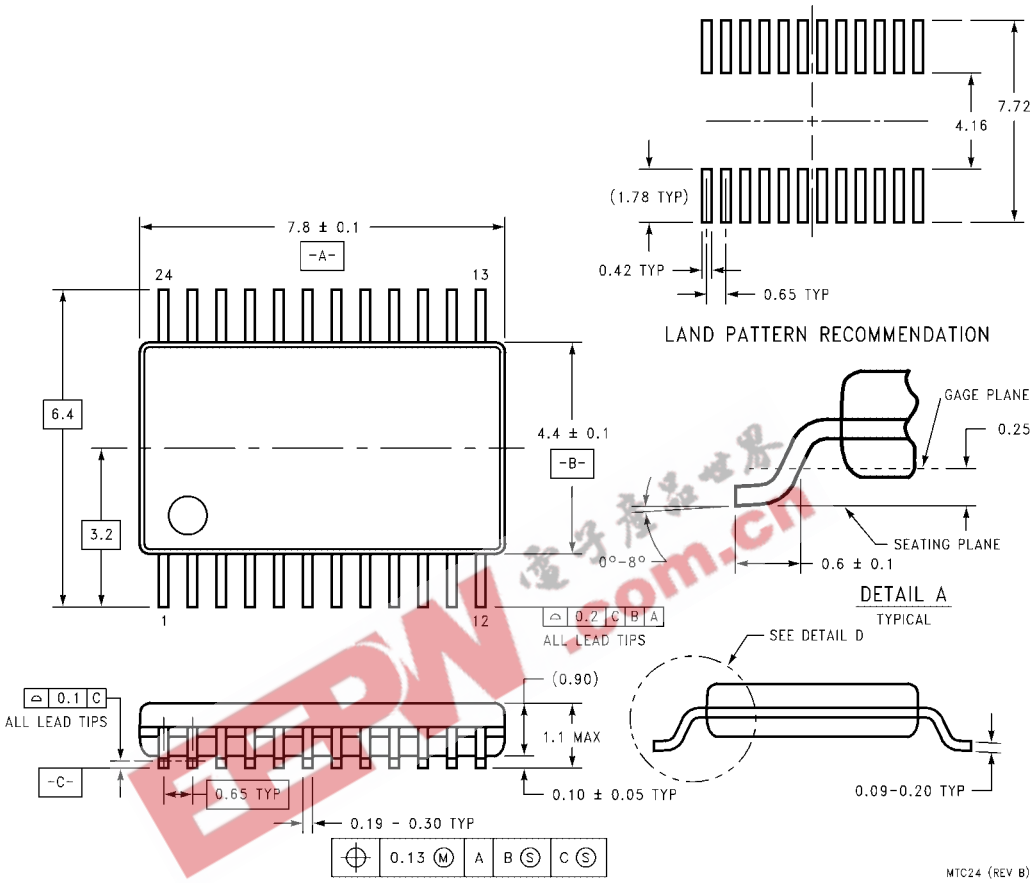



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**
**Package Number M24B**




**24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide**
**Package Number MQA24**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC24**



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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