

## 74VHC574

### Octal D-Type Flip-Flop with 3-STATE Outputs

#### General Description

The VHC574 is an advanced high speed CMOS octal flip-flop with 3-STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8-bit D-type flip-flop is controlled by a clock input (CP) and an output enable input ( $\overline{OE}$ ). When the  $\overline{OE}$  input is HIGH, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

cuit prevents device destruction due to mismatched supply and input voltages.

#### Features

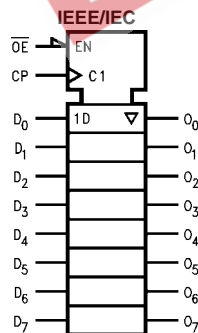
- High Speed:  $t_{PD} = 5.6$  ns (typ) at  $V_{CC} = 5$ V
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min)
- Power Down Protection is provided on all inputs
- Low Noise:  $V_{OLP} = 0.6$ V (typ)
- Low Power Dissipation:  $I_{CC} = 4$   $\mu$ A (Max) @  $T_A = 25^\circ$ C
- Pin and Function Compatible with 74HC574

#### Ordering Code:

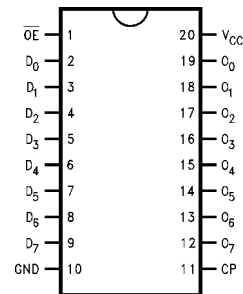
Order Number	Package Number	Package Description
74VHC574M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHC574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153
74VHC574N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Logic Symbol



#### Connection Diagram



#### Pin Descriptions

Pin Names	Description
$D_0$ – $D_7$	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
$O_0$ – $O_7$	3-STATE Outputs

## Functional Description

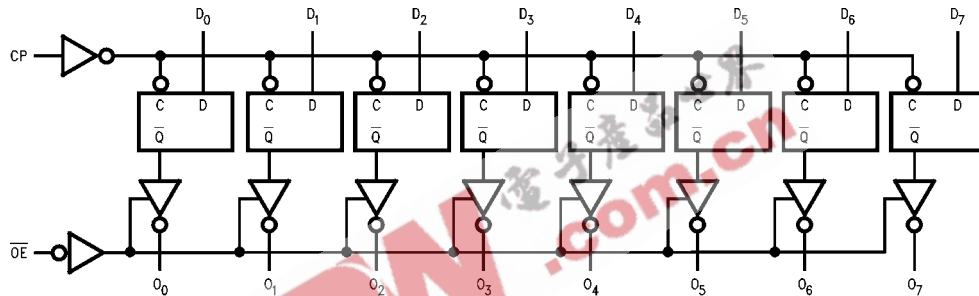
The VHC574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Truth Table

Inputs			Outputs
$D_n$	CP	$\overline{OE}$	$O_n$
H	↗	L	H
L	↗	L	L
X	X	H	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 ↗ = LOW-to-HIGH Transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +7.0V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to $V_{CC} + 0.5V$
Input Diode Current ( $I_{IK}$ )	-20 mA
Output Diode Current	$\pm 20$ mA
DC Output Current ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ /GND Current ( $I_{CC}$ )	$\pm 75$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Lead Temperature ( $T_L$ ) (Soldering, 10 seconds)	260°C

**Recommended Operating Conditions** (Note 2)

Supply Voltage ( $V_{CC}$ )	2.0V to +5.5V
Input Voltage ( $V_{IN}$ )	0V to +5.5V
Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
Operating Temperature ( $T_{OPR}$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	
$V_{CC} = 3.3V \pm 0.3V$	0 ~ 100 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ~ 20 ns/V

**Note 1:** Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions	
			Min	Typ	Max	Min	Max			
$V_{IH}$	HIGH Level Input Voltage	2.0 3.0 – 5.5	1.50			1.50		V		
$V_{IL}$	LOW Level Input Voltage	2.0 3.0 – 5.5			0.50 0.3 $V_{CC}$		0.50 0.3 $V_{CC}$	V		
$V_{OH}$	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu\text{A}$
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4		V		$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$
		3.0	2.58			2.48				
4.5	3.94			3.80						
$V_{OL}$	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu\text{A}$
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1	V		$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$
		3.0			0.36		0.44			
4.5			0.36		0.44					
$I_{OZ}$	3-STATE Output Off-State Current	5.5		$\pm 0.25$		$\pm 2.5$	$\mu\text{A}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND		
$I_{IN}$	Input Leakage Current	0 – 5.5		$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$	$V_{IN} = 5.5V$ or GND		
$I_{CC}$	Quiescent Supply Current	5.5		4.0		40.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND		

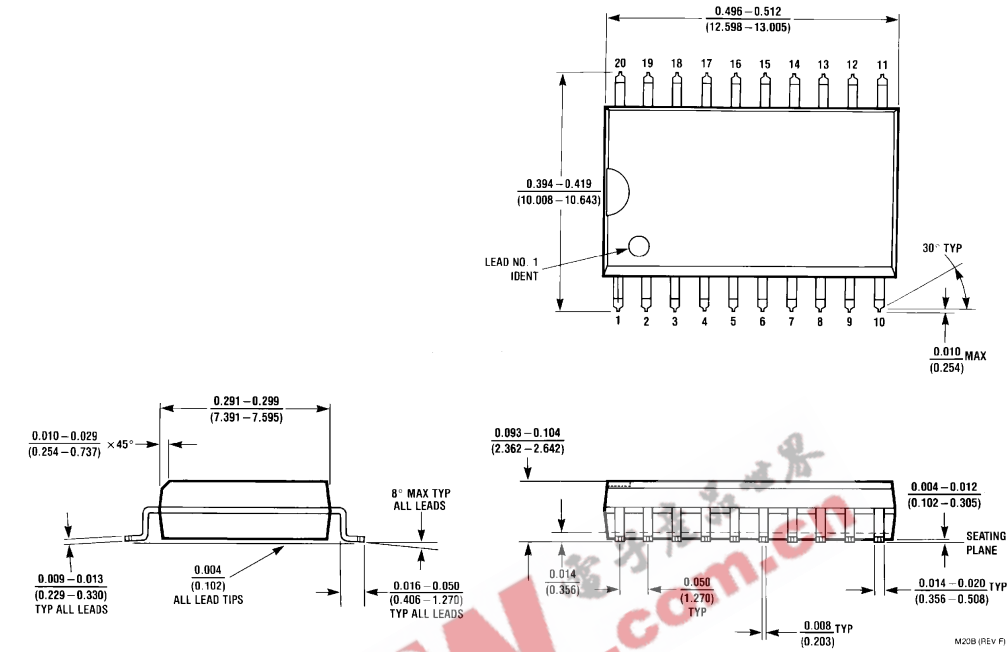
**Noise Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$		Units	Conditions
			Typ	Limits		
$V_{OLP}$ (Note 3)	Quiet Output Maximum Dynamic $V_{OL}$	5.0	1.0	1.2	V	$C_L = 50 \text{ pF}$
$V_{OLV}$ (Note 3)	Quiet Output Minimum Dynamic $V_{OL}$	5.0	-0.8	-1.0	V	$C_L = 50 \text{ pF}$
$V_{IHD}$ (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50 \text{ pF}$
$V_{ILD}$ (Note 3)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50 \text{ pF}$

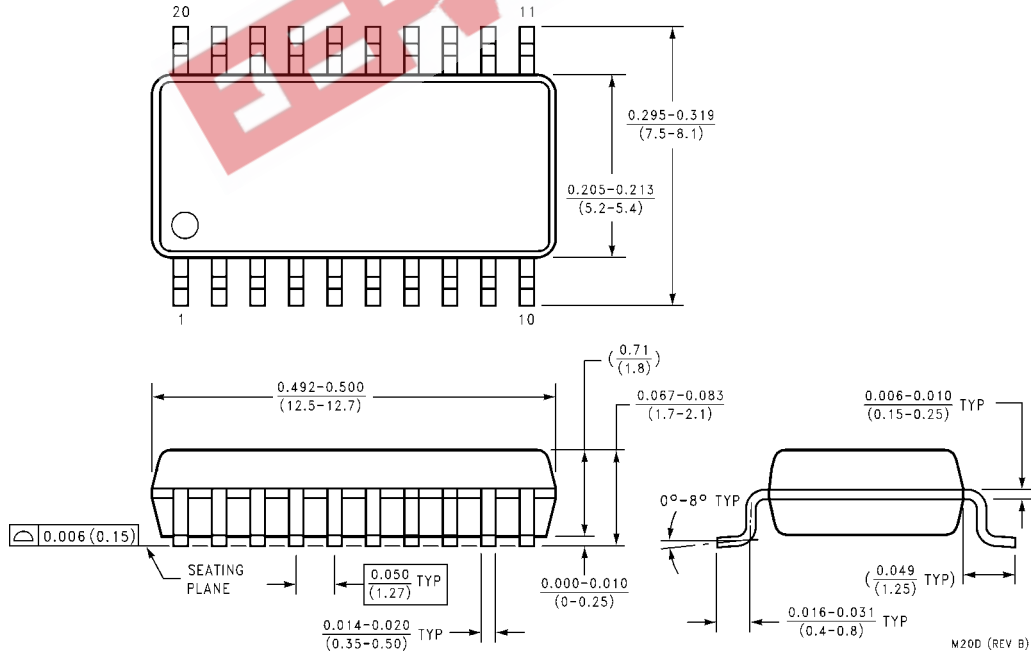
**Note 3:** Parameter guaranteed by design.

AC Electrical Characteristics									
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay Time (CP to O <sub>n</sub> )	3.3 ± 0.3	8.5	13.2	1.0	15.5	ns	C <sub>L</sub> = 15 pF	
t <sub>PHL</sub>			11.0	16.7	1.0	19.0		C <sub>L</sub> = 50 pF	
		5.0 ± 0.5	5.6	8.6	1.0	10.0	ns	C <sub>L</sub> = 15 pF	
			7.1	10.6	1.0	12.0		C <sub>L</sub> = 50 pF	
t <sub>PZL</sub>	3-STATE Output Enable Time	3.3 ± 0.3	8.2	12.8	1.0	15.0	ns	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 15 pF	
t <sub>PZH</sub>			10.7	16.3	1.0	18.5		C <sub>L</sub> = 50 pF	
		5.0 ± 0.5	5.9	9.0	1.0	10.5	ns	C <sub>L</sub> = 15 pF	
			7.4	11.0	1.0	12.5		C <sub>L</sub> = 50 pF	
t <sub>PLZ</sub>	3-STATE Output Disable Time	3.3 ± 0.3	11.0	15.0	1.0	17.0	ns	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 50 pF	
t <sub>PHZ</sub>		5.0 ± 0.5	7.1	10.1	1.0	11.5		C <sub>L</sub> = 50 pF	
t <sub>OSSLH</sub>	Output to	3.3 ± 0.3		1.5		1.5	ns	(Note 4), C <sub>L</sub> = 50 pF	
t <sub>OSSLH</sub>	Output Skew	5.0 ± 0.5		1.0		1.0		C <sub>L</sub> = 50 pF	
f <sub>MAX</sub>	Maximum Clock Frequency	3.3 ± 0.3	80	125	65		MHz	C <sub>L</sub> = 15 pF	
			50	75	45			C <sub>L</sub> = 50 pF	
		5.0 ± 0.5	130	180	110			C <sub>L</sub> = 15 pF	
			85	115	75			C <sub>L</sub> = 50 pF	
C <sub>IN</sub>	Input Capacitance		4	10	10		pF	V <sub>CC</sub> = Open	
C <sub>OUT</sub>	Output Capacitance		6				pF	V <sub>CC</sub> = 5.0V	
C <sub>PD</sub>	Power Dissipation Capacitance		28				pF	(Note 5)	
<p><b>Note 4:</b> Parameter guaranteed by design. t<sub>OSSLH</sub> =  t<sub>PLH</sub> max - t<sub>PLH</sub> min ; t<sub>OSSLH</sub> =  t<sub>PHL</sub> max - t<sub>PHL</sub> min </p> <p><b>Note 5:</b> C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC</sub> (opr.) = C<sub>PD</sub> * V<sub>CC</sub> * f<sub>IN</sub> + I<sub>CC</sub>/8 (per F/F). The total C<sub>PD</sub> when n pcs. of the Octal D Flip-Flop operates can be calculated by the equation: C<sub>PD</sub> (total) = 20 + 8n.</p>									
AC Operating Requirements									
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units	
			Min	Typ	Max	Min	Max		
t <sub>W(H)</sub>	Minimum Pulse Width (CP)	3.3 ± 0.3	5.0			5.0	ns		
t <sub>W(L)</sub>		5.0 ± 0.5	5.0			5.0			
t <sub>S</sub>	Minimum Set-Up Time	3.3 ± 0.3	3.5			3.5	ns		
		5.0 ± 0.5	3.5			3.5			
t <sub>H</sub>	Minimum Hold Time	3.3 ± 0.3	1.5			1.5	ns		
		5.0 ± 0.5	1.5			1.5			

**Physical Dimensions** inches (millimeters) unless otherwise noted

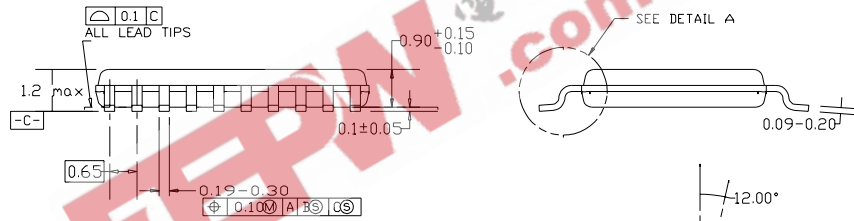
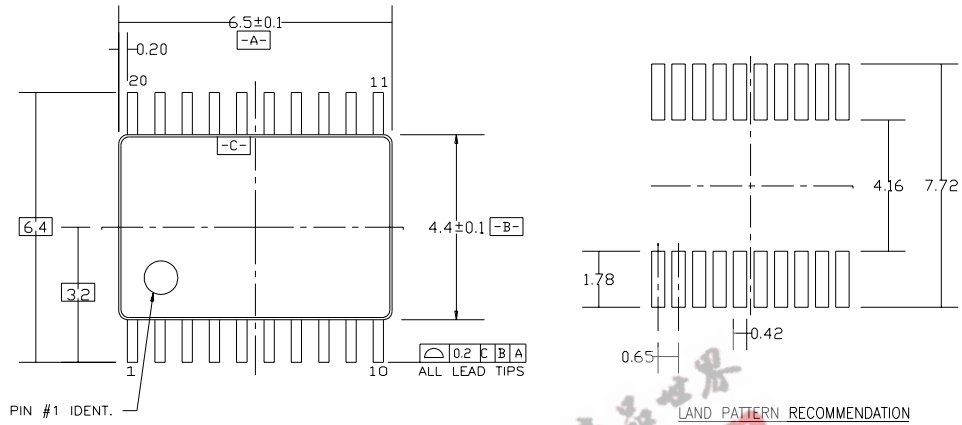


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B**

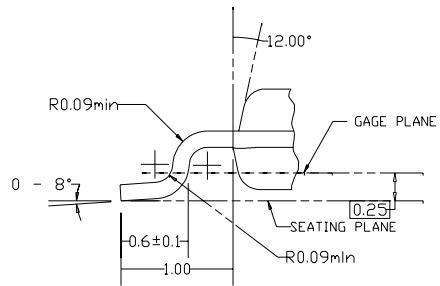


**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS



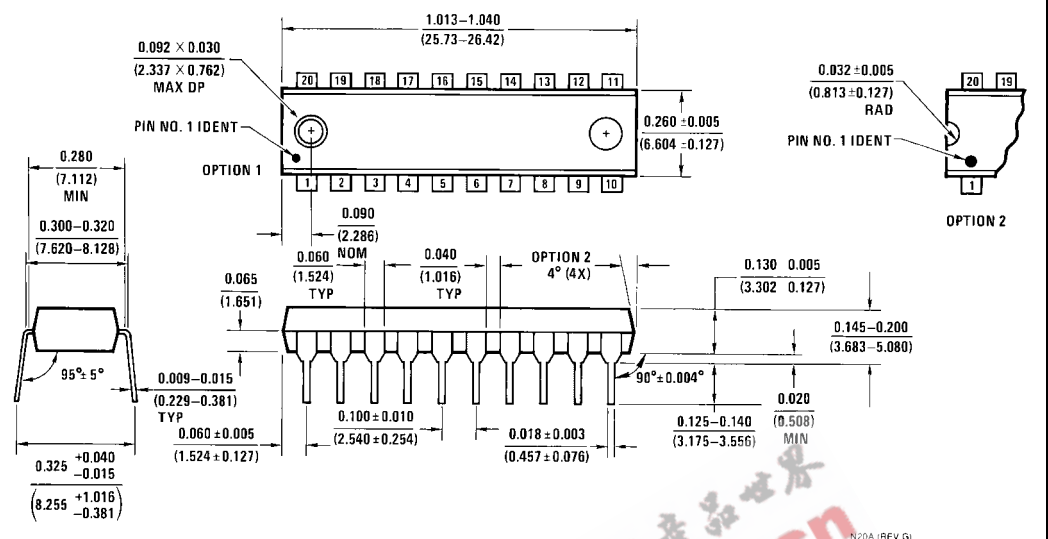
DETAIL A

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MD-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N20A

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.