

74ABT126 Quad Buffer with 3-STATE Outputs

General Description

The ABT126 contains four independent non-inverting buffers with 3-STATE outputs.

Features

- Non-inverting buffers
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed latching protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

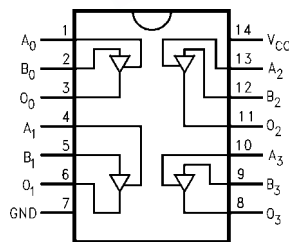
Ordering Code:

Order Number	Package Number	Package Description
74ABT126CSC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ABT126CSJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT126CMT	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ABT126CMTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Connection Diagram



Pin Descriptions

Pin Names	Descriptions
A_n, B_n	Inputs
O_n	Outputs

Function Table

Inputs		Output
A_n	B_n	O_n
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
X = Immaterial

Absolute Maximum Ratings (Note 2)		Recommended Operating Conditions	
Storage Temperature	-65°C to +150°C	Free Air Ambient Temperature	-40°C to +85°C
Ambient Temperature under Bias	-55°C to +125°C	Supply Voltage	+4.5V to +5.5V
Junction Temperature under Bias	-55°C to +150°C	Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V	Data Input	50 mV/ns
Input Voltage (Note 3)	-0.5V to +7.0V	Enable Input	100 mV/ns
Input Current (Note 3)	-30 mA to +5.0 mA		
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to 5.5V		
in the HIGH State	-0.5V to V _{CC}		
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)		
DC Latchup Source Current (Across Comm Operating Range)	-300 mA		
Over Voltage Latchup (I/O)	10V		

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage		0.8		V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.5			V	Min	I _{OH} = -3 mA
		2.0			V	Min	I _{OH} = -32 mA
V _{OL}	Output LOW Voltage			0.55	V	Min	I _{OL} = 64 mA
I _{IH}	Input HIGH Current		1		μA	Max	V _{IN} = 2.7V (Note 4)
			1		μA	Max	V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-1	μA	Max	V _{IN} = 0.5V (Note 4)
				-1	μA	Max	V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA, All Other Pin Grounded
I _{OZH}	Output Leakage Current			10	μA	0 - 5.5V	V _{OUT} = 2.7V; \overline{OE}_n = 2.0V
I _{OZL}	Output Leakage Current			-10	μA	0 - 5.5V	V _{OUT} = 0.5V; \overline{OE}_n = 2.0V
I _{OS}	Output Short-Circuit Current	-100		-275	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output HIGH Leakage Current		50		μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test			100	μA	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply Current			50	μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			15	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			50	μA	Max	\overline{OE}_n = V _{CC} ; All Others at V _{CC} or Ground
				50	μA	Max	\overline{OE}_n = V _{CC} ; All Others at V _{CC} or Ground
I _{CCT}	Additional I _{CC} /Input	Outputs Enabled		1.5	mA	Max	V _I = V _{CC} - 2.1V
		Outputs 3-STATE		1.5	mA		Enable Input V _I = V _{CC} - 2.1V
		Outputs 3-STATE		50	μA		Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or Ground
I _{CCD}	Dynamic I _{CC} (Note 4)	No Load		0.1	mA/ MHz	Max	Outputs Open \overline{OE}_n = GND, (Note 5) One Bit Toggling, 50% Duty Cycle

Note 4: Guaranteed, but not tested.

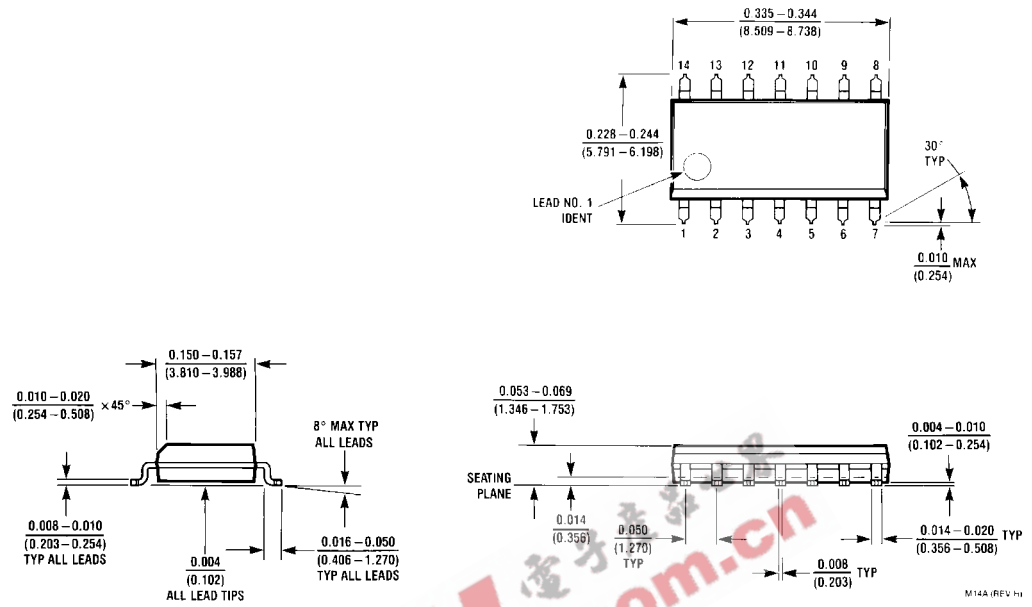
Note 5: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

AC Electrical Characteristics							
Symbol	Parameter	T _A = +25°C V _{CC} = +5V C _L = 50 pF			T _A = -40°C to +85°C V _{CC} = 4.5V–5.5V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	1.0		4.4	1.0	4.4	ns
t _{PHL}	Data to Outputs	1.0		4.6	1.0	4.6	
t _{PZH}	Output Enable	1.0		6.5	1.0	6.5	ns
t _{PZL}	Time	1.0		6.5	1.0	6.5	
t _{PHZ}	Output Disable	1.0		5.8	1.0	5.8	ns
t _{PLZ}	Time	1.0		5.5	1.0	5.5	

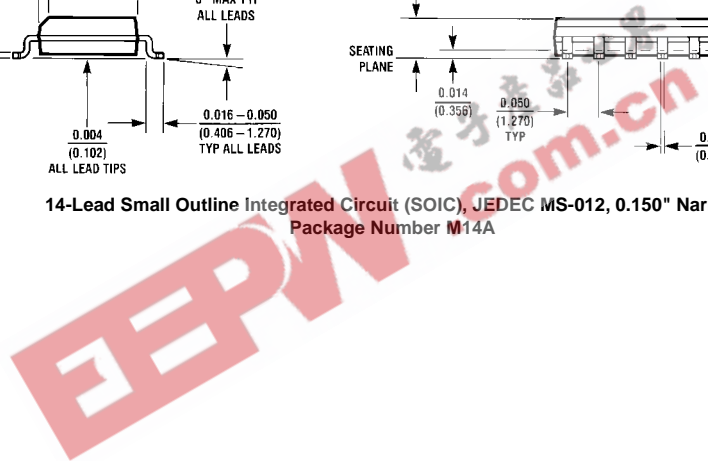
Capacitance				
Symbol	Parameter	Typ	Units	Conditions T _A = 25°C
C _{IN}	Input Capacitance	5.0	pF	V _{CC} = 0V
C _{OUT} (Note 6)	Output Capacitance	9.0	pF	V _{CC} = 5.0V

Note 6: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

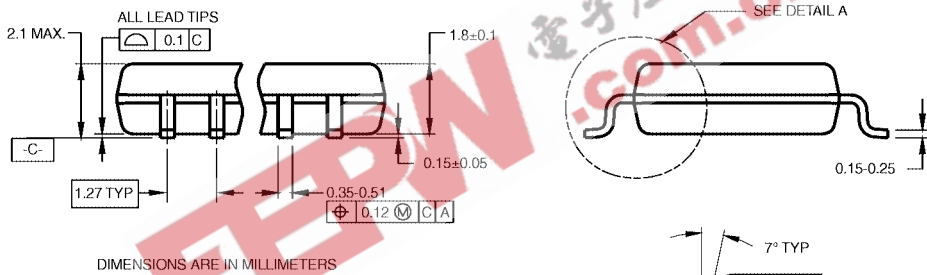
Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

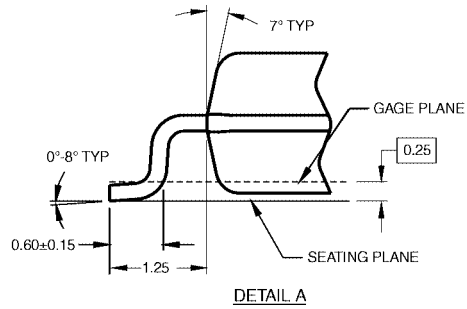


Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



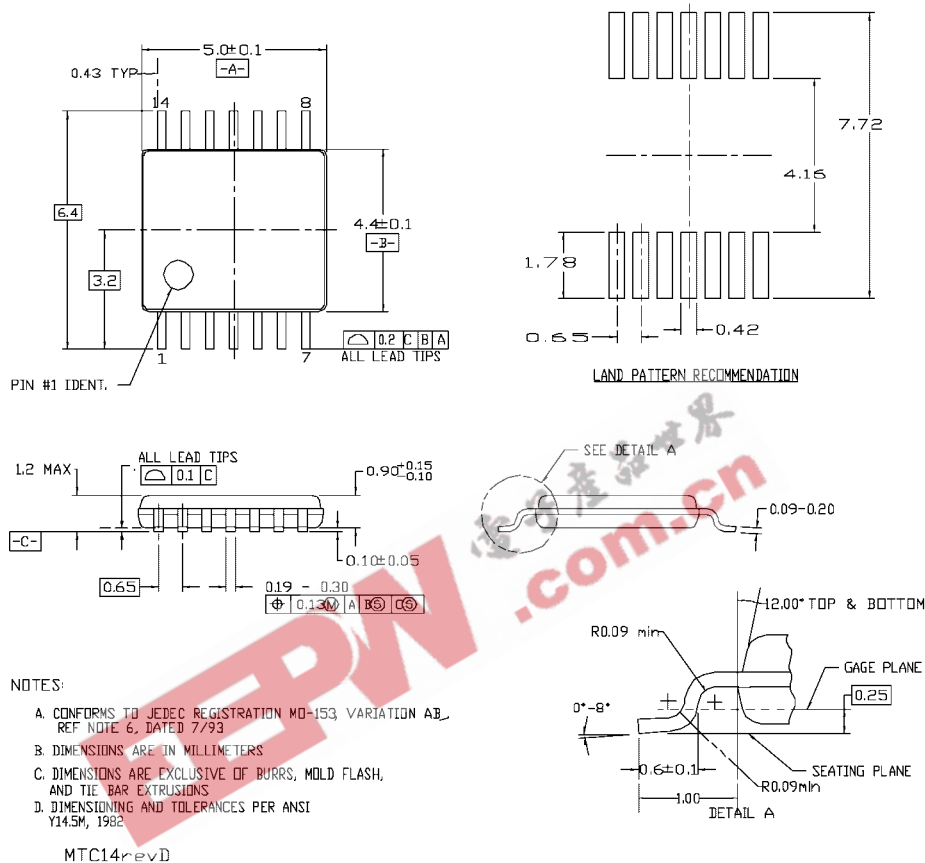
- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

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