FAIRCHILD SEMICONDUCTOR®

June 1999
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74VCX2245
Low Voltage Bidirectional Transceiver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in B Outputs

General Description

The VCX2245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The T/$\overline{R}$ input determines the direction of data flow. The $\overline{OE}$ input disables both the A and B ports by placing them in a high impedance state.

The 74VCX2245 is designed for low voltage (1.4V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V. The VCX2245 is also designed with 26Ω series resistance in the B Port outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers transmitters

The 74VCX2245 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

Features

- 1.4V - 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in B Port outputs
- Power-off high impedance inputs and outputs
- Supports Live Insertion and Withdrawal (Note 1)
- t_{PD} (A to B)
  4.4 ns max for 3.0V to 3.6V V_{CC}
- Static Drive (I_{OH}/I_{OL} B outputs):
  ±12 mA @ 3.0V V_{CC}
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Latchup performance exceeds JEDEC 78 conditions
- ESD performance:
  Human body model > 2000V
  Machine model > 200V
- Leadless DQFN Pb-Free package

Note 1: To ensure the high impedance state during power up and power down, $\overline{OE}_n$ should be tied to V_{CC} through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver.

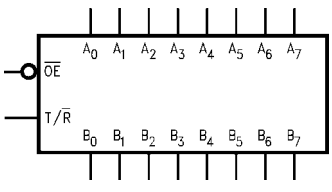
Ordering Code:

Order Number	Package Number	Package Description
74VCX2245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VCX2245BQX (Note 2)	MLP020B	Pb-Free 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
74VCX2245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 2: DQFN package available in Tape and Reel only.

Logic Symbol



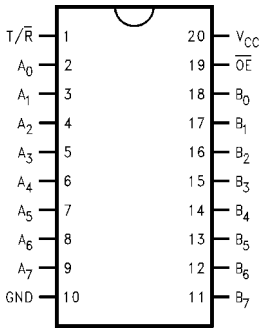
Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-STATE Outputs
B_0–B_7	Side B Inputs or 3-STATE Outputs

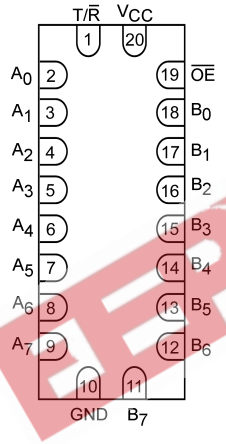
Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

Connection Diagrams

Pin Assignments for SOIC and TSSOP



Pad Assignments for DQFN



(Top Through View)

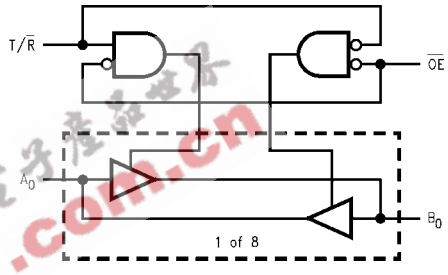
Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7 (Note 3)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Note 3: Unused bus terminals during HIGH Z State must be held HIGH or LOW.

Logic Diagram



Absolute Maximum Ratings (Note 4)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
DC Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +4.6V
Outputs Active (Note 5)	−0.5V to V_{CC} + 0.5V
DC Input Diode Current (I_{IK}) V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current	±100 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 6)

Power Supply Voltage (V_{CC})	
Operating	1.4V to 3.6V
Input Voltage	−0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0V to 3.6V
Output Current in I_{OH}/I_{OL} - A Outputs	
V_{CC} = 3.0V to 3.6V	± 24 mA
V_{CC} = 2.3V to 2.7V	± 18 mA
V_{CC} = 1.65V to 2.3V	± 6 mA
V_{CC} = 1.4V to 1.65V	± 2 mA
Output Current in I_{OH}/I_{OL} - B Outputs	
V_{CC} = 3.0V to 3.6V	± 12 mA
V_{CC} = 2.3V to 2.7V	± 8 mA
V_{CC} = 1.65V to 2.3V	± 3 mA
V_{CC} = 1.4V to 1.65V	± 1 mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: I_O Absolute Maximum Rating must be observed.

Note 6: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	0.65 x V_{CC}		
			1.4 - 1.6	0.65 x V_{CC}		
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		0.35 x V_{CC}	
			1.4 - 1.6		0.35 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7 - 3.6	V_{CC} - 0.2		V
	A Outputs	I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
		I_{OH} = −100 μA	2.3 - 2.7	V_{CC} - 0.2		
		I_{OH} = −6 mA	2.3	2.0		
		I_{OH} = −12 mA	2.3	1.8		
		I_{OH} = −18 mA	2.3	1.7		
		I_{OH} = −100 μA	1.65 - 2.3	V_{CC} - 0.2		
		I_{OH} = −8 mA	1.65	1.25		
		I_{OH} = −100 μA	1.4 - 1.6	V_{CC} - 0.2		
		I_{OH} = −2 mA	1.4	1.05		

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100 µA	2.7 - 3.6	V_{CC} - 0.2		V
	B Outputs	I_{OH} = –6 mA	2.7	2.2		
		I_{OH} = –8 mA	3.0	2.4		
		I_{OH} = –12 mA	3.0	2.2		
		I_{OH} = –100 µA	2.3 - 2.7	V_{CC} - 0.2		
		I_{OH} = –4 mA	2.3	2.0		
		I_{OH} = –6 mA	2.3	1.8		
		I_{OH} = –8 mA	2.3	1.7		
		I_{OH} = –100 µA	1.65 - 2.3	V_{CC} - 0.2		
		I_{OH} = –3 mA	1.65	1.25		
		I_{OH} = –100 µA	1.4 - 1.6	V_{CC} - 0.2		
		I_{OH} = –1 mA	1.4	1.05		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.7 - 3.6		0.2	V
	A Outputs	I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 18 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
		I_{OL} = 100 µA	2.3 - 2.7		0.2	
		I_{OL} = 12 mA	2.3		0.4	
		I_{OL} = 18 mA	2.3		0.6	
		I_{OL} = 100 µA	1.65 - 2.3		0.2	
		I_{OL} = 6 mA	1.65		0.3	
		I_{OL} = 100 µA	1.4 - 1.6		0.2	
		I_{OL} = 2 mA	1.4		0.35	
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.7 - 3.6		0.2	V
	B Outputs	I_{OL} = 6 mA	2.7		0.4	
		I_{OL} = 8 mA	3.0		0.55	
		I_{OL} = 12 mA	3.0		0.8	
		I_{OL} = 100 µA	2.7- 2.7		0.2	
		I_{OL} = 6 mA	2.3		0.4	
		I_{OL} = 8 mA	2.3		0.6	
		I_{OL} = 100 µA	1.65 - 2.3		0.2	
		I_{OL} = 3 mA	1.65		0.3	
		I_{OL} = 100 µA	1.4 - 1.6		0.2	
		I_{OL} = 1 mA	1.4		0.35	
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6V	1.4 - 3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 3.6V V_I = V_{IH} or V_{IL}	1.4 - 3.6		±10	µA
I_{OFF}	Power Off Leakage Current	0 ≤ (V_I, V_O) ≤ 3.6V	0		10	µA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	1.4 - 3.6		20	µA
		V_{CC} ≤ (V_I, V_O) ≤ 3.6V (Note 7)	1.4 - 3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} –0.6V	2.7 - 3.6		750	µA

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 8)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units	Figure Number
				Min	Max		
t_{PHL} t_{PLH}	Propagation Delay B_n to A_n	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.6	3.5	ns	Figures 1, 2
			2.5 ± 0.2	0.8	4.2		
			1.8 ± 0.15	1.5	8.4		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	16.8		Figures 5, 6
t_{PZL} t_{PZH}	Output Enable Time B_n to A_n	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.6	4.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	5.6		
			1.8 ± 0.15	1.5	9.8		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 5, 7, 8
t_{PLZ} t_{PHZ}	Output Disable Time B_n to A_n	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.6	3.6	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	4.0		
			1.8 ± 0.15	1.5	7.2		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	14.4		Figures 5, 7, 8
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 9)	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1		1.5		
t_{PHL} t_{PLH}	Propagation Delay A_n to B_n	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.6	4.4	ns	Figures 1, 2
			2.5 ± 0.2	0.8	5.6		
			1.8 ± 0.15	1.5	9.8		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 5, 6
t_{PZL} t_{PZH}	Output Enable Time A_n to B_n	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.6	5.0	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	6.6		
			1.8 ± 0.15	1.5	9.8		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 5, 7, 8
t_{PLZ} t_{PHZ}	Output Disable Time A_n to B_n	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.6	4.2	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	4.7		
			1.8 ± 0.15	1.5	8.5		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	16.9		Figures 5, 7, 8

Note 8: For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}, B to A	C_L = 30 pF, V_{IH} = V_{CC}, V_{IL} = 0V	1.8	0.3	V
			2.5	0.7	
			3.3	1.0	
	Quiet Output Dynamic Peak V_{OL}, A to B	C_L = 30 pF, V_{IH} = V_{CC}, V_{IL} = 0V	1.8	0.2	V
			2.5	0.45	
			3.3	0.65	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}, B to A	C_L = 30 pF, V_{IH} = V_{CC}, V_{IL} = 0V	1.8	–0.3	V
			2.5	–0.7	
			3.3	–1.0	
	Quiet Output Dynamic Valley, V_{OL}, A to B	C_L = 30 pF, V_{IH} = V_{CC}, V_{IL} = 0V	1.8	–0.2	V
			2.5	–0.45	
			3.3	–0.65	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}, B to A	C_L = 30 pF, V_{IH} = V_{CC}, V_{IL} = 0V	1.8	1.3	V
			2.5	1.7	
			3.3	2.0	
	Quiet Output Dynamic Valley V_{OH}, A to B	C_L = 30 pF, V_{IH} = V_{CC}, V_{IL} = 0V	1.8	1.5	V
			2.5	2.0	
			3.3	2.5	

Capacitance

Symbol	Parameter	Conditions	T_A = +25°C Typical	Units
C_{IN}	Input Capacitance	V_I = 0V or V_{CC}, V_{CC} = 1.8V, 2.5V or 3.3V	6	pF
$C_{I/O}$	Input/Output Capacitance	V_I = 0V or V_{CC}, V_{CC} = 1.8V, 2.5V or 3.3V	7	pF
C_{PD}	Power Dissipation Capacitance	V_I = 0V or V_{CC}, f = 10 MHz, V_{CC} = 1.8V, 2.5V or 3.3V	20	pF

AC Loading and Waveforms (V_{CC} 3.3V ± 0.3V to 1.8V ± 0.15V)

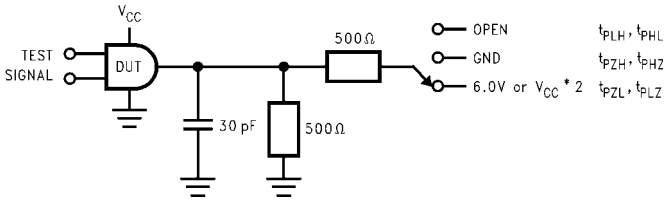


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V; V_{CC} x 2 at V_{CC} = 2.5V ± 0.2V; 1.8V ± 0.15V
t_{PZH}, t_{PHZ}	GND

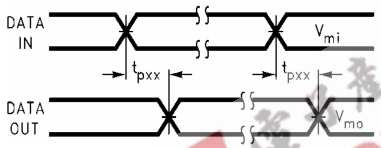


FIGURE 2. Waveform for Inverting and Non-inverting Functions

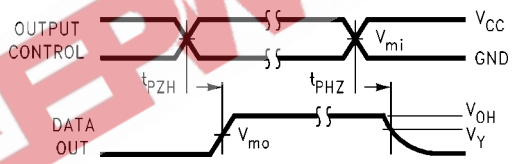


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

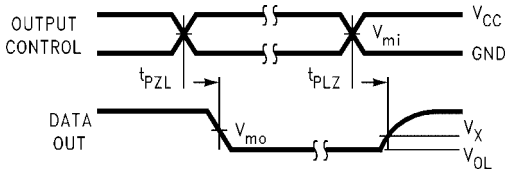


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	V_{CC}/2	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V

AC Loading and Waveforms (V_{CC} 1.5V ± 0.1V)

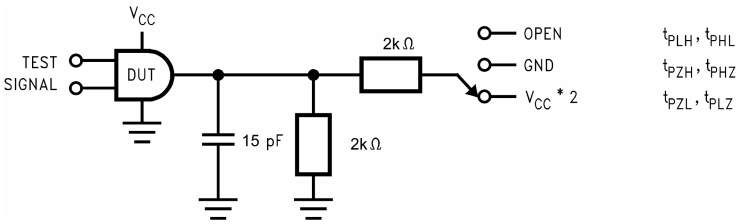


FIGURE 5. AC Test Circuit

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC} x 2 at V_{CC} = 1.5V ± 0.1V
t_{PZH}, t_{PHZ}	GND

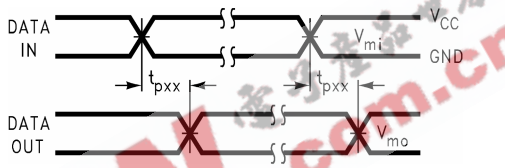


FIGURE 6. Waveform for Inverting and Non-inverting Functions

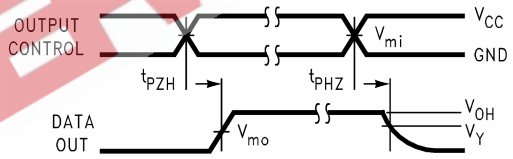


FIGURE 7. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

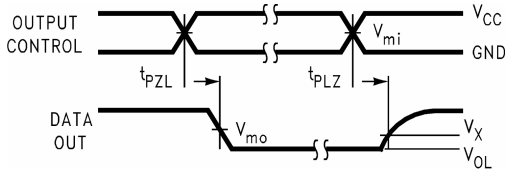


FIGURE 8. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

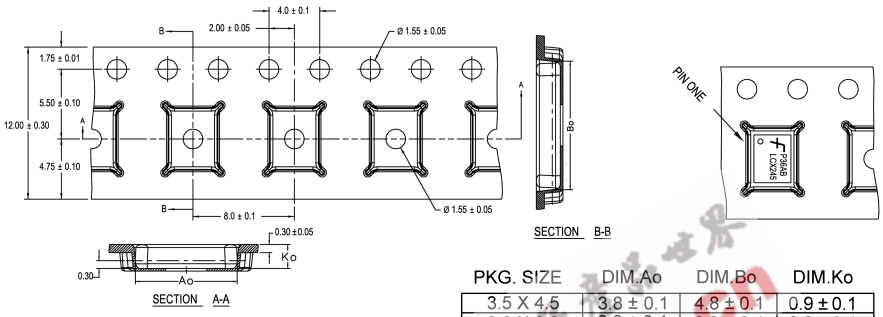
Symbol	V_{CC}
	1.5V ± 0.1V
V_{mi}	V_{CC}/2
V_{mo}	V_{CC}/2
V_x	V_{OL} + 0.1V
V_y	V_{OH} − 0.1V

Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



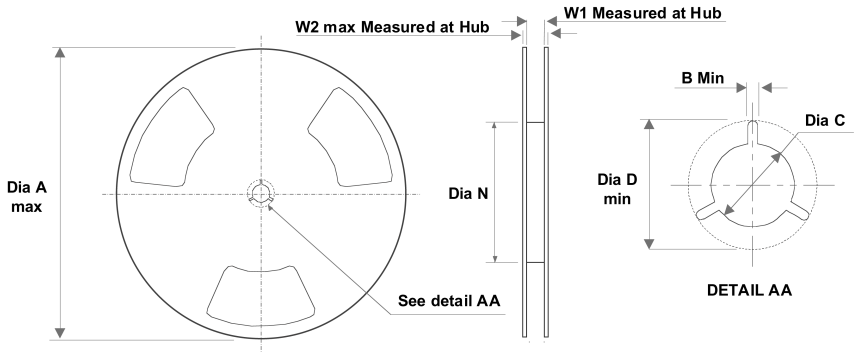
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

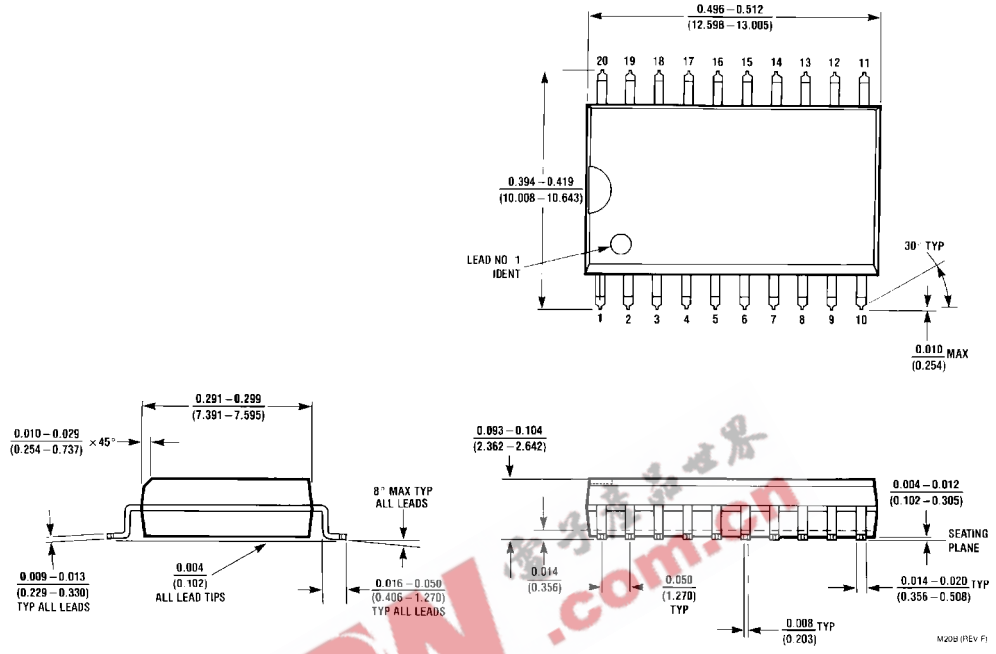
1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.

REEL DIMENSIONS inches (millimeters)



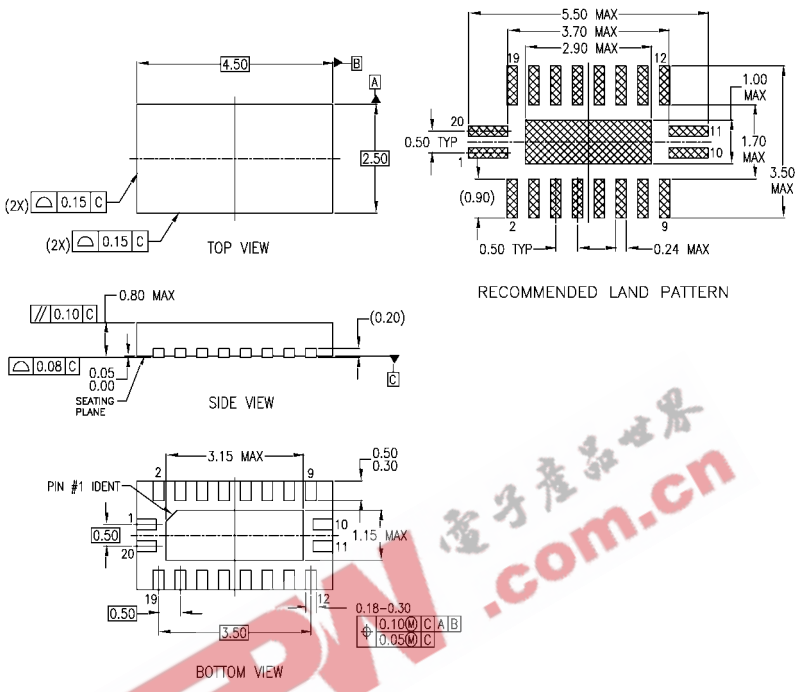
Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



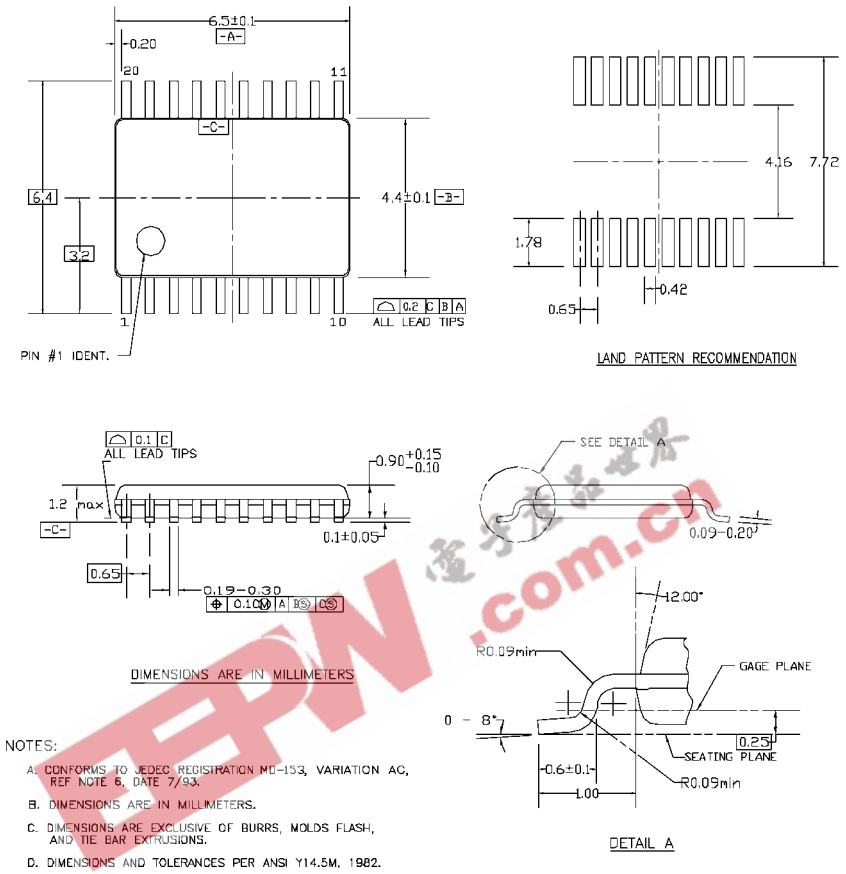
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AC
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP020BrevA

Pb-Free 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
Package Number MLP020B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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