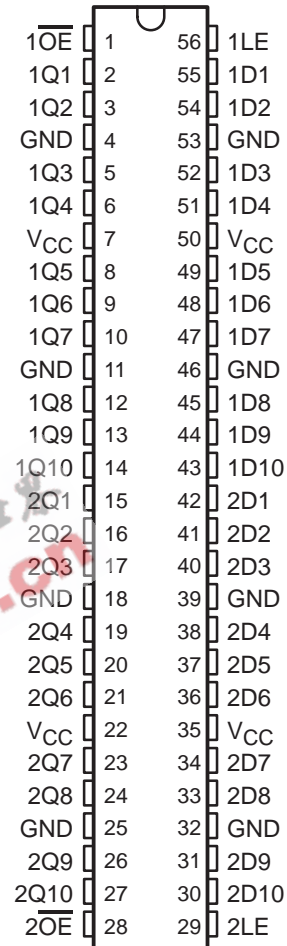


54ACT16841, 74ACT16841 20-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS174A – MAY 1991 – REVISED APRIL 1996

- Members of the Texas Instruments *Widebus*™ Family
- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Provide Extra Bus Driving/Latches Necessary for Wider Address/Data Paths or Buses With Parity
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) Packages, 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

54ACT16841 . . . WD PACKAGE
74ACT16841 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 20-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ACT16841 can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable ($\overline{1OE}$ or $\overline{2OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

\overline{OE} does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1996, Texas Instruments Incorporated

54ACT16841, 74ACT16841 20-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS174A – MAY 1991 – REVISED APRIL 1996

description (continued)

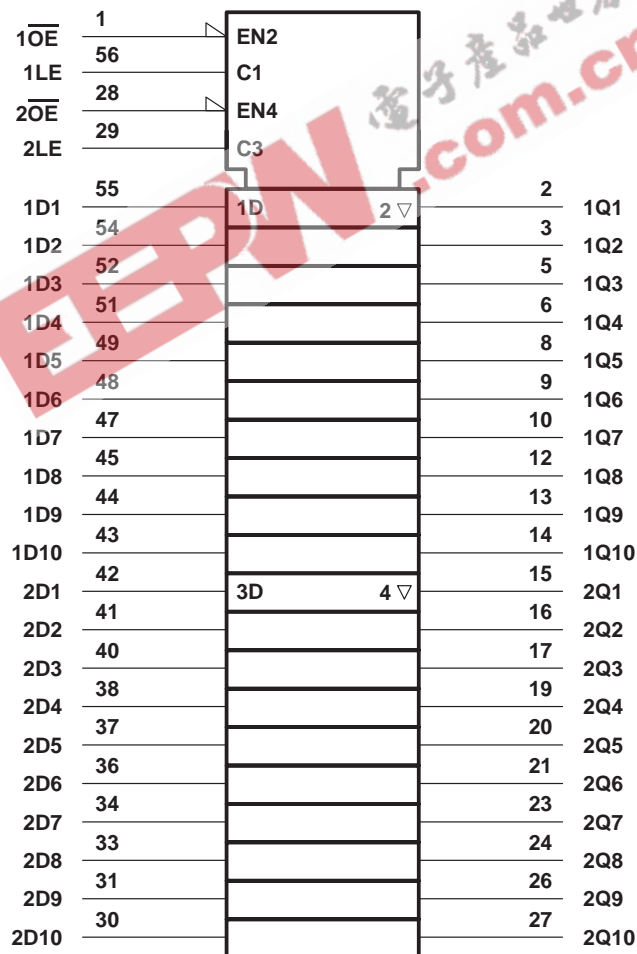
The 74ACT16841 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16841 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT16841 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 10-bit latch)

INPUTS			OUTPUT
$\overline{\text{OE}}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†

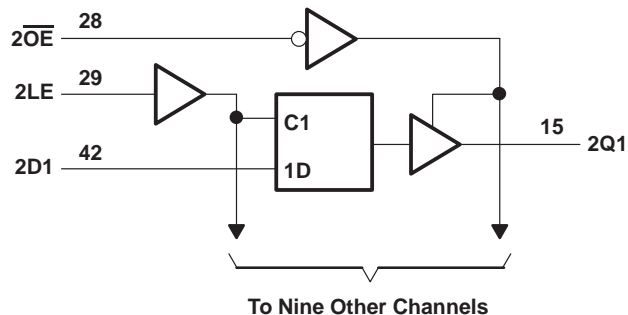
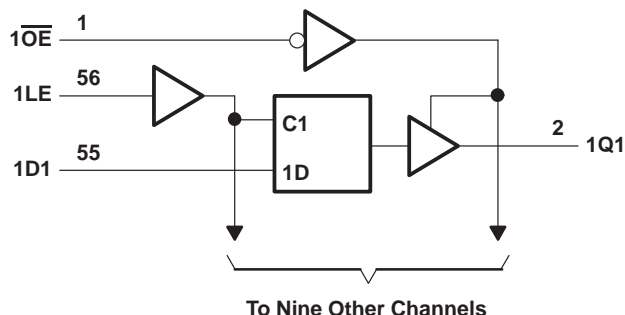


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

54ACT16841, 74ACT16841 20-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS174A – MAY 1991 – REVISED APRIL 1996

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 500 mA
Maximum package power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DGG package	1 W
DL package	1.4 W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

	54ACT16841			74ACT16841			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
V_I Input voltage	0		V_{CC}	0		V_{CC}	V
V_O Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH} High-level output current			-24			-24	mA
I_{OL} Low-level output current			24			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0		10	0		10	ns/V
T_A Operating free-air temperature	-55		125	-40		85	$^\circ\text{C}$

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

54ACT16841, 74ACT16841 20-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS174A – MAY 1991 – REVISED APRIL 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT16841		74ACT16841		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4	V	
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
	I _{OH} = -75 mA†	5.5 V				3.85		3.85		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1	0.1	V	
		5.5 V			0.1		0.1	0.1		
	I _{OL} = 24 mA	4.5 V			0.36		0.44	0.44		
		5.5 V			0.36		0.44	0.44		
	I _{OL} = 75 mA†	5.5 V				1.65		1.65		
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1	±1	μA	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±5	±5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		80	80	μA	
ΔI _{CC} ‡	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			0.9		1	1	mA	
C _i	V _I = V _{CC} or GND	5 V			3				pF	
C _o	V _O = V _{CC} or GND	5 V			11				pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		54ACT16841		74ACT16841		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	4		4		4		ns
t _{su}	Setup time, data before LE↓	1.5		1.5		1.5		ns
t _h	Hold time, data after LE↓	High	3	3		3		ns
		Low	4.5	4.5		4.5		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54ACT16841		74ACT16841		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	4	7.1	10.3	4	11.8	4	11.8	ns
t _{PHL}			3.2	6.9	11	3.2	12.2	3.2	12.2	
t _{PLH}	LE	Q	4.5	7.7	11.3	4.5	12.7	4.5	12.7	ns
t _{PHL}			4.3	7.8	11.4	4.3	12.7	4.3	12.7	
t _{PZH}	\overline{OE}	Q	3.1	6.4	10.1	3.1	11.3	3.1	11.3	ns
t _{PZL}			3.8	7.6	12.1	3.8	13.7	3.8	13.7	
t _{PHZ}	\overline{OE}	Q	4	7.3	9.5	4	10.2	4	10.2	ns
t _{PLZ}			4	6.8	8.9	4	9.6	4	9.6	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

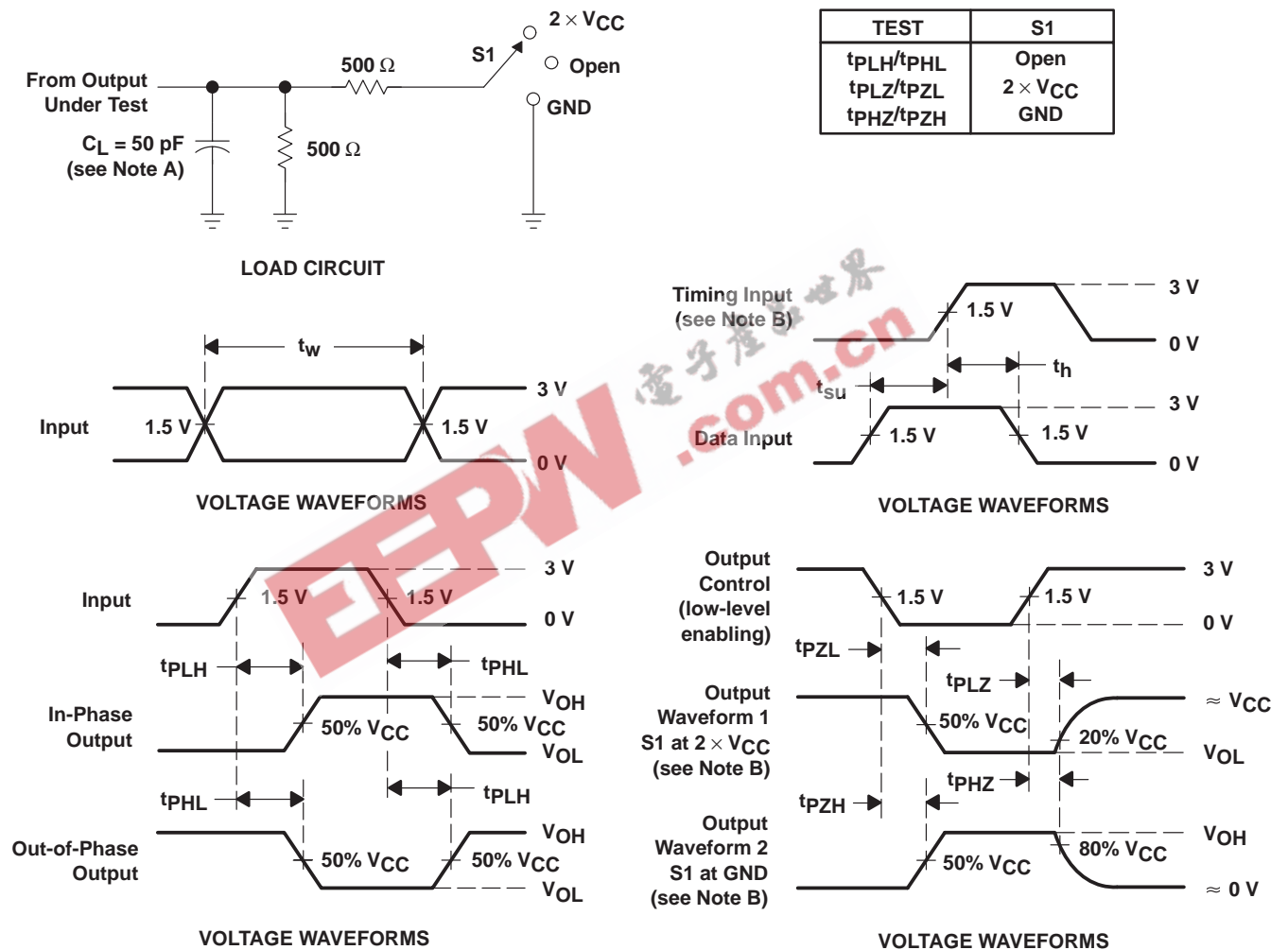
54ACT16841, 74ACT16841
20-BIT BUS-INTERFACE D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCAS174A – MAY 1991 – REVISED APRIL 1996

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	Outputs enabled	41	pF
		Outputs disabled	10	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.