

# DATA SHEET

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## 74LV595

8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

Product specification

1998 Apr 20

IC24 Data Handbook

## 8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

74LV595

### FEATURES

- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between  $V_{CC} = 2.7V$  and  $V_{CC} = 3.6V$
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8V$  at  $V_{CC} = 3.3V$ ,  $T_{amb} = 25^{\circ}C$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2V$  at  $V_{CC} = 3.3V$ ,  $T_{amb} = 25^{\circ}C$
- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-State outputs
- Shift register with direct clear
- Output capability:
  - parallel outputs; bus driver
  - serial output; standard
- $I_{CC}$  category: MSI

### APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register

### DESCRIPTION

The 74LV595 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT595.

The 74LV595 is an 8-stage serial shift register with a storage register and 3-State outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the  $SH_{CP}$  input. The data in each register is transferred to the storage register on a positive-going transition of the  $ST_{CP}$  input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input ( $D_S$ ) and a serial standard output ( $Q_7$ ) all for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-State bus driver outputs. Data in the storage register appears at the output whenever the output enable input ( $\overline{OE}$ ) is LOW.

### QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^{\circ}C$ ;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay $SH_{CP}$ to $Q_7$ , $ST_{CP}$ to $Q_7$ , MR to $Q_7$	$C_L = 15pF$ $V_{CC} = 3.3V$	15 16 14	ns
$f_{max}$	Maximum clock frequency $SH_{CP}$ , $ST_{CP}$		77	MHz
$C_I$	Input capacitance		3.5	pF
$C_{PD}$	Power dissipation capacitance per gate	$V_{CC} = 3.3V$ Notes 1 and 2	115	pF

#### NOTES:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
- The condition is  $V_I = GND$  to  $V_{CC}$ .

### ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	-40°C to +125°C	74LV595 N	74LV595 N	SOT38-4
16-Pin Plastic SO	-40°C to +125°C	74LV595 D	74LV595 D	SOT109-1
16-Pin Plastic SSOP Type II	-40°C to +125°C	74LV595 DB	74LV595 DB	SOT338-1
16-Pin Plastic TSSOP Type I	-40°C to +125°C	74LV595 PW	74LV595PW DH	SOT403-1

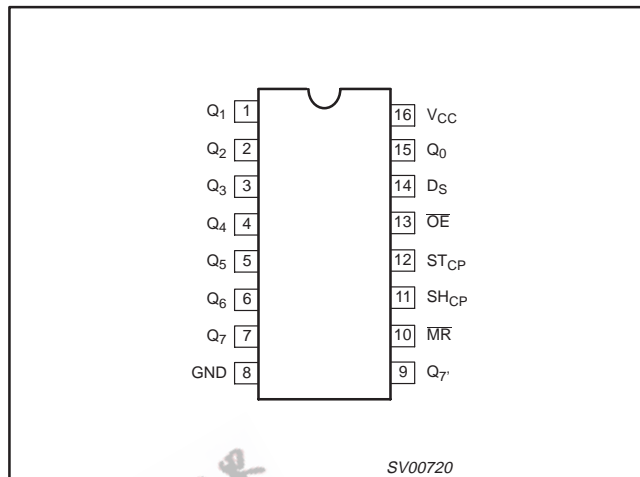
# 8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

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## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
15, 1, 2, 3, 4, 5, 6, 7	Q <sub>0</sub> to Q <sub>7</sub>	Parallel data output
8	GND	Ground (0V)
9	Q <sub>7</sub> '	Serial data output
10	$\overline{MR}$	Master reset (active LOW)
11	SH <sub>CP</sub>	Shift register clock input
12	ST <sub>CP</sub>	Storage register clock input
13	$\overline{OE}$	Output enable input (active LOW)
14	D <sub>S</sub>	Serial data input
16	V <sub>CC</sub>	Positive supply voltage

## PIN CONFIGURATION



## FUNCTION TABLE

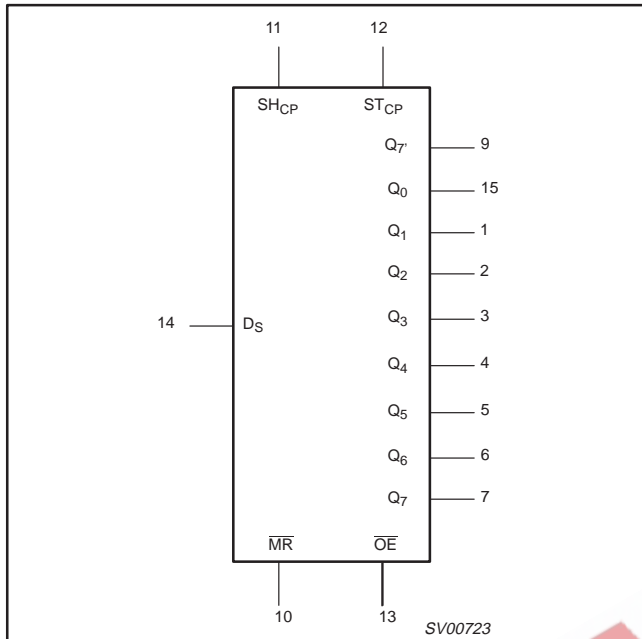
INPUTS				OUTPUTS		FUNCTION	
SH <sub>CP</sub>	ST <sub>CP</sub>	OE	MR	D <sub>S</sub>	Q <sub>7</sub> '		
X	X	L	L	X	L	NC	A LOW level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	Empty shift register loaded into storage register
X	X	H	L	X	L	Z	Shift register clear. Parallel outputs in high-impedance OFF-states
↑	X	L	H	H	Q <sub>6</sub> '	NC	Logic high level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q <sub>6</sub> ') appears on the serial output (Q <sub>7</sub> ')
X	↑	L	H	X	NC	Q <sub>n</sub> '	Contents of shift register stages (internal Q <sub>n</sub> ') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q <sub>6</sub> '	Q <sub>n</sub> '	Contents of shift register shifted through. Previous contents of the shift register are transferred to the storage register and the parallel output stages

- H = HIGH voltage level
- L = LOW voltage level
- X = Don't care
- Z = High impedance OFF-state
- NC = No change
- ↑ = LOW-to-HIGH clock transition
- ↓ = HIGH-to-LOW transition

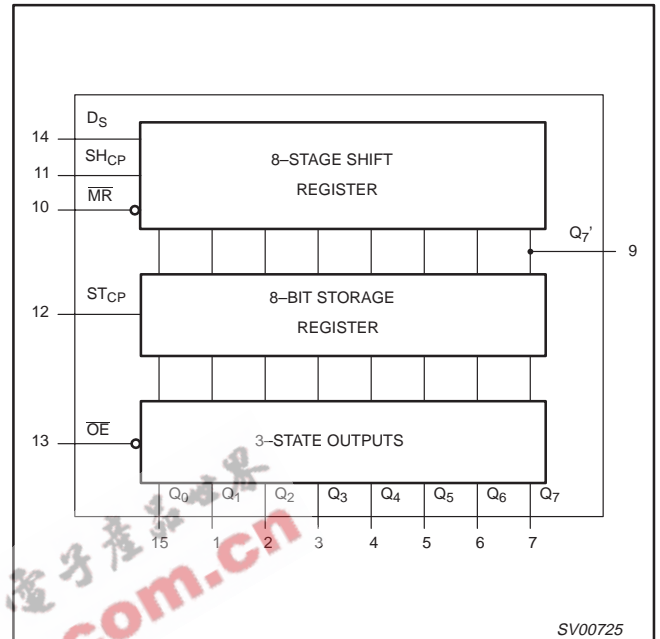
# 8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

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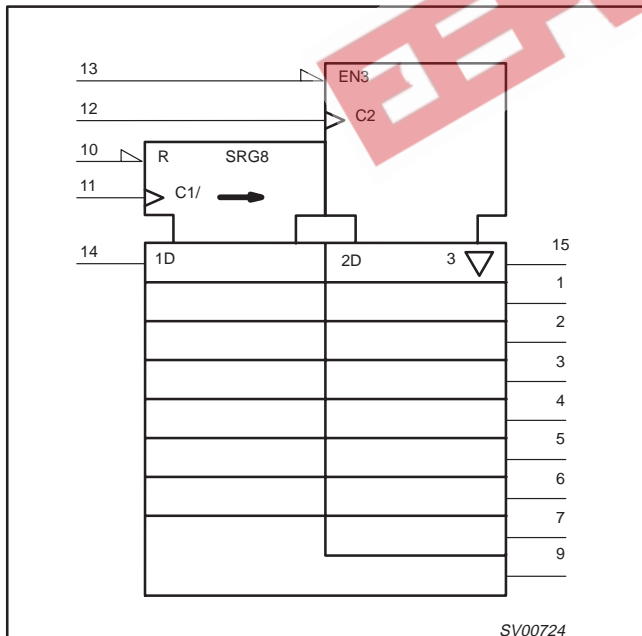
### LOGIC SYMBOL



### FUNCTIONAL DIAGRAM



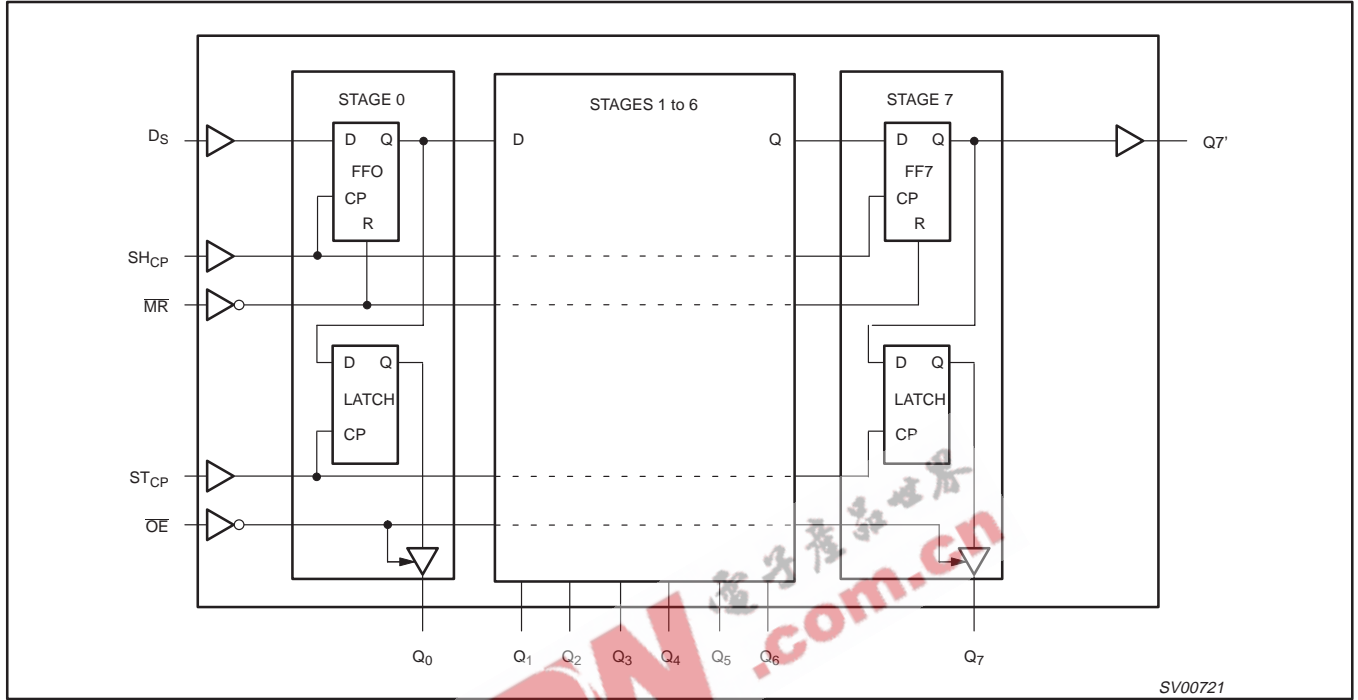
### LOGIC SYMBOL (IEEE/IEC)



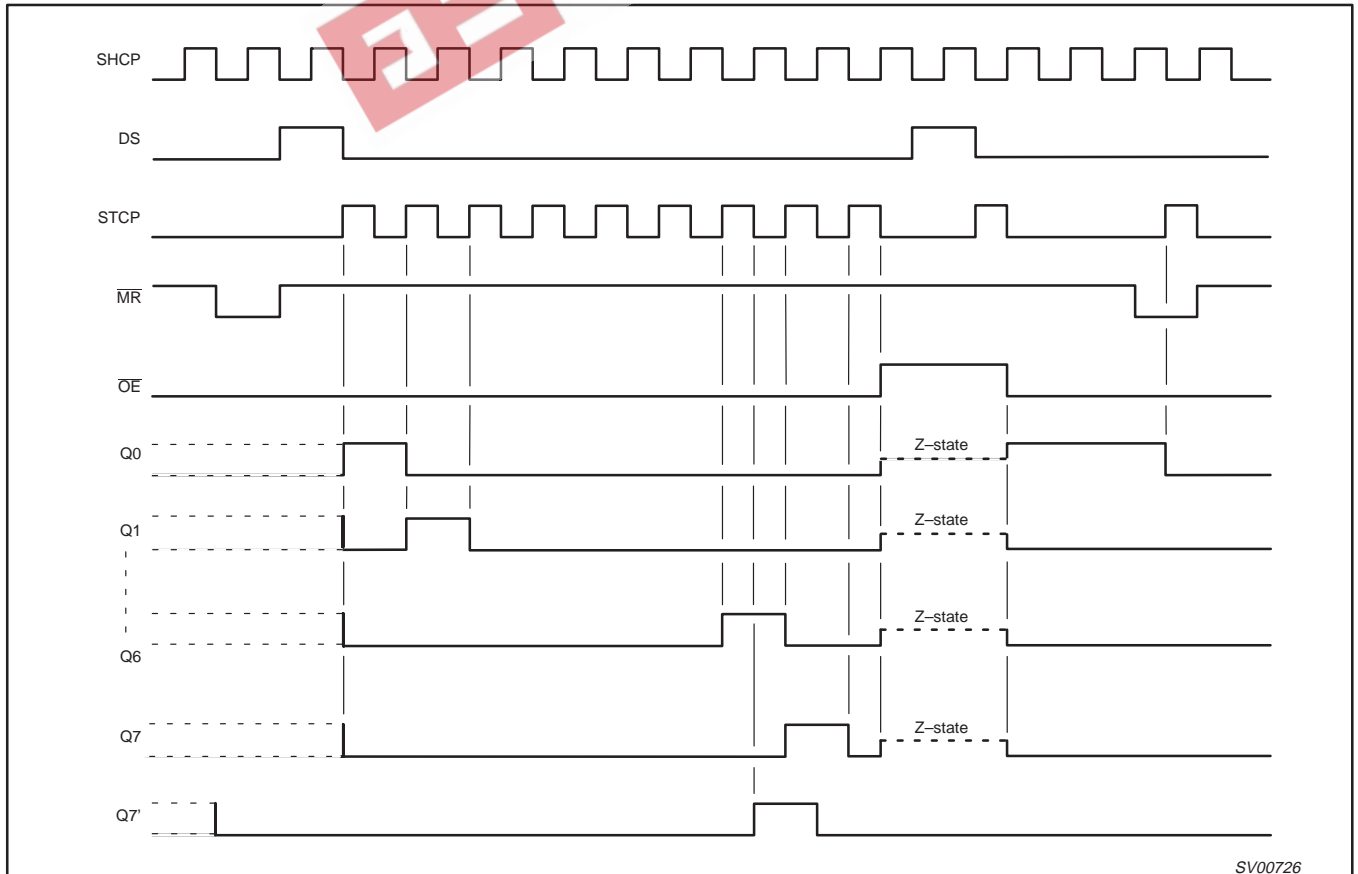
# 8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

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## LOGIC DIAGRAM



## TIMING DIAGRAM



# 8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CC}$	DC supply voltage	See Note1	1.0	3.3	3.6	V
$V_I$	Input voltage		0	–	$V_{CC}$	V
$V_O$	Output voltage		0	–	$V_{CC}$	V
$T_{amb}$	Operating ambient temperature range in free air	See DC and AC characteristics	–40		+85 +125	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$	–	–	500 200 100	ns/V

### NOTE:

- The LV is guaranteed to function down to  $V_{CC} = 1.0V$  (input levels GND or  $V_{CC}$ ); DC characteristics are guaranteed from  $V_{CC} = 1.2V$  to  $V_{CC} = 3.6V$ .

## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25 35	mA
$\pm I_{GND}, \pm I_{CC}$	DC $V_{CC}$ or GND current for types with –standard outputs –bus driver outputs		50 70	mA
$T_{stg}$	Storage temperature range		–65 to +150	°C
$P_{TOT}$	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## DC CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			–40°C to +85°C			–40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$V_{IH}$	HIGH level Input voltage	$V_{CC} = 1.2V$	0.9			0.9		V
		$V_{CC} = 2.0V$	1.4			1.4		
		$V_{CC} = 2.7$ to $3.6V$	2.0			2.0		
$V_{IL}$	LOW level Input voltage	$V_{CC} = 1.2V$			0.3		0.3	V
		$V_{CC} = 2.0V$			0.6		0.6	
		$V_{CC} = 2.7$ to $3.6V$			0.8		0.8	
$V_{OH}$	HIGH level output voltage; all outputs	$V_{CC} = 1.2V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$		1.2				V
		$V_{CC} = 2.0V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	1.8	2.0		1.8		
		$V_{CC} = 2.7V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	2.5	2.7		2.5		
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	2.8	3.0		2.8		
$V_{OH}$	HIGH level output voltage; STANDARD outputs	$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; -I_O = 6mA$	2.40	2.82		2.20		V

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## DC CHARACTERISTICS (Continued)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				UNIT
			-40°C to +85°C		-40°C to +125°C		
$V_{OH}$	HIGH level output voltage; BUS driver outputs	$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = 8mA$	2.40	2.82		2.20	V
$V_{OL}$	LOW level output voltage; all outputs	$V_{CC} = 1.2V; V_I = V_{IH} \text{ or } V_{IL}; I_O = 100\mu A$		0			V
		$V_{CC} = 2.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = 100\mu A$		0	0.2	0.2	
		$V_{CC} = 2.7V; V_I = V_{IH} \text{ or } V_{IL}; I_O = 100\mu A$		0	0.2	0.2	
		$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = 100\mu A$		0	0.2	0.2	
$V_{OL}$	LOW level output voltage; STANDARD outputs	$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = 6mA$		0.25	0.40	0.50	V
$V_{OL}$	LOW level output voltage; BUS driver outputs	$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = 8mA$		0.20	0.40	0.50	V
$I_I$	Input leakage current	$V_{CC} = 3.6V; V_I = V_{CC} \text{ or } GND$			1.0	1.0	$\mu A$
$I_{OZ}$	3-State output OFF-state current	$V_{CC} = 3.6V; V_I = V_{IH} \text{ or } V_{IL}; V_O = V_{CC} \text{ or } GND$			5	10	$\mu A$
$I_{CC}$	Quiescent supply current; MSI	$V_{CC} = 3.6V; V_I = V_{CC} \text{ or } GND; I_O = 0$			20.0	160	$\mu A$
$\Delta I_{CC}$	Additional quiescent supply current per input	$V_{CC} = 2.7V \text{ to } 3.6V; V_I = V_{CC} - 0.6V$			500	850	$\mu A$

### NOTE:

1. All typical values are measured at  $T_{amb} = 25^\circ C$ .

## AC CHARACTERISTICS

GND = 0V;  $t_r = t_f \leq 2.5ns$ ;  $C_L = 50pF$ ;  $R_L = 1K\Omega$ 

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS -40 to +85 °C			LIMITS -40 to +125 °C		UNIT
				$V_{CC}(V)$	MIN	TYP <sup>1</sup>	MAX	MIN	
$t_{PHL}/t_{PLH}$	Propagation delay SH <sub>CP</sub> to Q <sub>7'</sub>	Figure 1	1.2	–	95	–	–	–	ns
			2.0	–	32	61	–	75	
			2.7	–	24	45	–	55	
			3.0 to 3.6	–	18 <sup>2</sup>	36	–	44	
$t_{PHL}/t_{PLH}$	Propagation delay ST <sub>CP</sub> to Q <sub>n</sub>	Figure 2	1.2	–	100	–	–	–	ns
			2.0	–	34	65	–	77	
			2.7	–	25	48	–	56	
			3.0 to 3.6	–	19 <sup>2</sup>	38	–	45	
$t_{PHL}$	Propagation delay MR to Q <sub>7'</sub>	Figure 5	1.2	–	85	–	–	–	ns
			2.0	–	29	56	–	66	
			2.7	–	21	41	–	49	
			3.0 to 3.6	–	16 <sup>2</sup>	33	–	33	
$t_{PZH}/t_{PZL}$	3-State output enable time OE to Q <sub>n</sub>	Figure 3	1.2	–	85	–	–	–	ns
			2.0	–	29	56	–	66	
			2.7	–	21	41	–	49	
			3.0 to 3.6	–	16 <sup>2</sup>	33	–	39	
$t_{PHZ}/t_{PLZ}$	3-State output disable time OE to Q <sub>n</sub>	Figure 3	1.2	–	65	–	–	–	ns
			2.0	–	24	40	–	49	
			2.7	–	18	32	–	37	
			3.0 to 3.6	–	14 <sup>2</sup>	26	–	30	

# 8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

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**AC CHARACTERISTICS (Continued)**GND = 0V;  $t_r = t_f \leq 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 1\text{K}\Omega$ 

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS -40 to +85 °C			LIMITS -40 to +125 °C		UNIT
				$V_{CC}(\text{V})$	MIN	TYP <sup>1</sup>	MAX	MIN	
$t_w$	Shift clock pulse width HIGH or LOW	Figure 1	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6 <sup>2</sup>	–	24	–	
$t_w$	Storage clock pulse width HIGH or LOW	Figure 2	2.0	34	7	–	41	–	ns
			2.7	25	5	–	30	–	
			3.0 to 3.6	20	4 <sup>2</sup>	–	24	–	
$t_w$	Master reset pulse width LOW	Figure 5	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6 <sup>2</sup>	–	24	–	
$t_{su}$	Set-up time $D_S$ to $SH_{CP}$	Figure 4	1.2	–	40	–	–	–	ns
			2.0	26	14	–	31	–	
			2.7	19	10	–	23	–	
			3.0 to 3.6	15	8 <sup>2</sup>	–	18	–	
$t_{su}$	Set-up time $SH_{CP}$ to $ST_{CP}$	Figure 2	1.2	–	40	–	–	–	ns
			2.0	26	14	–	31	–	
			2.7	19	10	–	23	–	
			3.0 to 3.6	15	8 <sup>2</sup>	–	18	–	
$t_h$	Hold time $D_S$ to $SH_{CP}$	Figure 4	1.2	–	–10	–	–	–	ns
			2.0	5	–4	–	5	–	
			2.7	5	–3	–	5	–	
			3.0 to 3.6	5	–2 <sup>2</sup>	–	5	–	
$t_{rem}$	Removal time $MR$ to $SH_{CP}$	Figure 5	1.2	–	–35	–	–	–	ns
			2.0	5	–12	–	5	–	
			2.7	5	–9	–	5	–	
			3.0 to 3.6	5	–7 <sup>2</sup>	–	5	–	
$f_{max}$	Maximum clock pulse frequency $SH_{CP}$ or $ST_{CP}$	Figure 1, 2	2.0	14	40	–	12	–	MHz
			2.7	19	58	–	16	–	
			3.0 to 3.6	24	70 <sup>2</sup>	–	20	–	

**NOTES:**

1. Unless otherwise stated, all typical values are at  $T_{amb} = 25^\circ\text{C}$ .
2. Typical value measured at  $V_{CC} = 3.3\text{V}$ .



# 8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

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### AC WAVEFORMS

$V_M = 1.5V$  at  $V_{CC} \geq 2.7V$   
 $V_M = 0.5 * V_{CC}$  at  $V_{CC} < 2.7V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$   
 $V_X = V_{OL} + 0.1V_{CC}$  at  $V_{CC} < 2.7V$   
 $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$   
 $V_Y = V_{OH} - 0.1V_{CC}$  at  $V_{CC} < 2.7V$

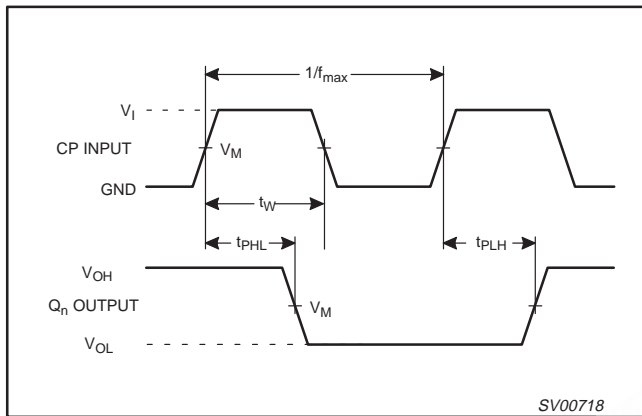


Figure 1. Clock (SH<sub>CP</sub>) to output (Q<sub>7</sub>), propagation delays, the shift clock pulse width and the maximum shift clock frequency.

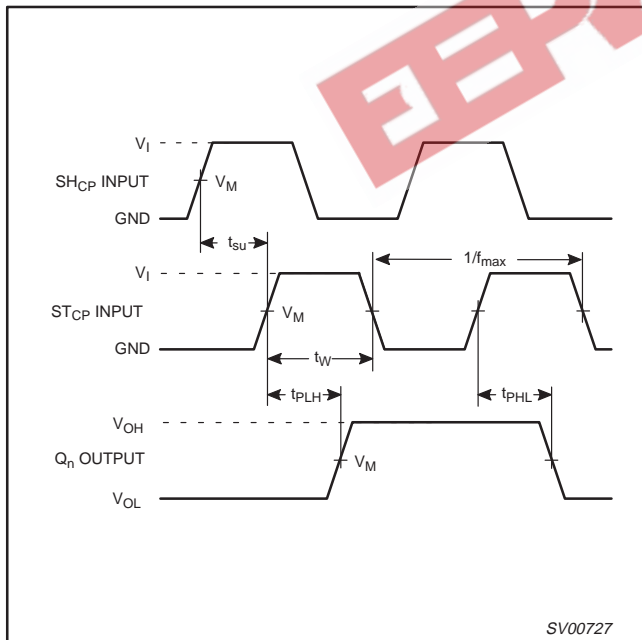


Figure 2. Storage clock (ST<sub>CP</sub>) to output (Q<sub>n</sub>) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time.

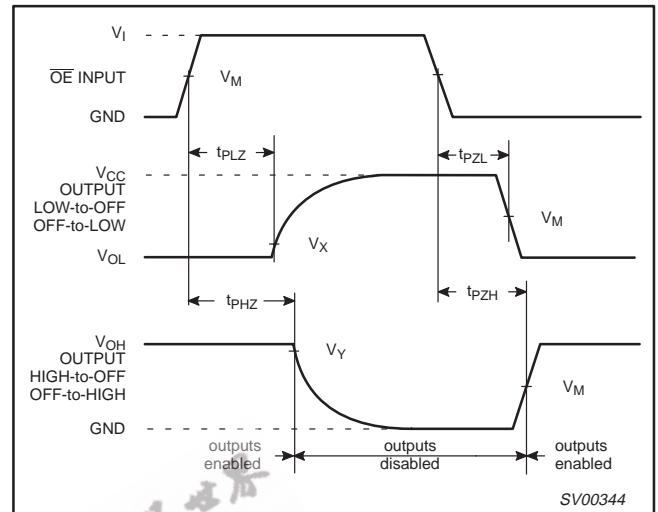


Figure 3. 3-State enable and disable times for input OE.

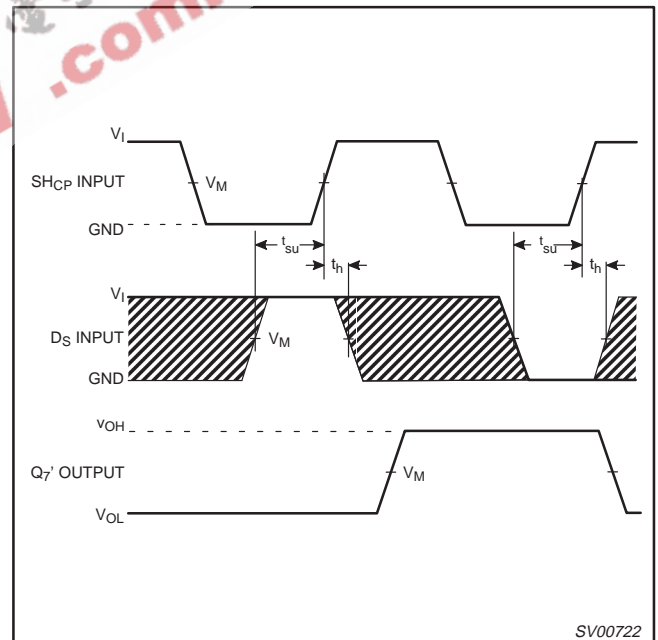


Figure 4. Data set-up and hold times for the data input (D<sub>S</sub>).

# 8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

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### AC WAVEFORMS (Continued)

- $V_M = 1.5V$  at  $V_{CC} \geq 2.7V$
- $V_M = 0.5 * V_{CC}$  at  $V_{CC} < 2.7V$
- $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.
- $V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$
- $V_X = V_{OL} + 0.1V_{CC}$  at  $V_{CC} < 2.7V$
- $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$
- $V_Y = V_{OH} - 0.1V_{CC}$  at  $V_{CC} < 2.7V$

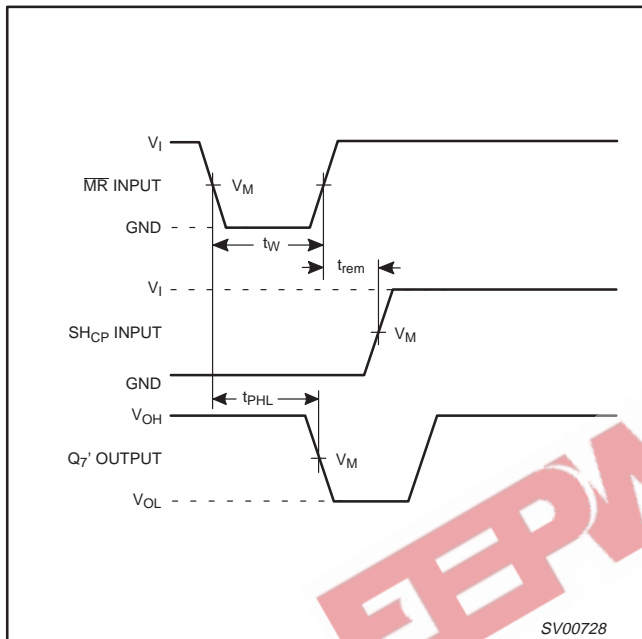


Figure 5. Master reset (MR) pulse width, the master reset to output (Q7') propagation delay and the master reset to shift clock (SHCP) removal time.

### TEST CIRCUIT

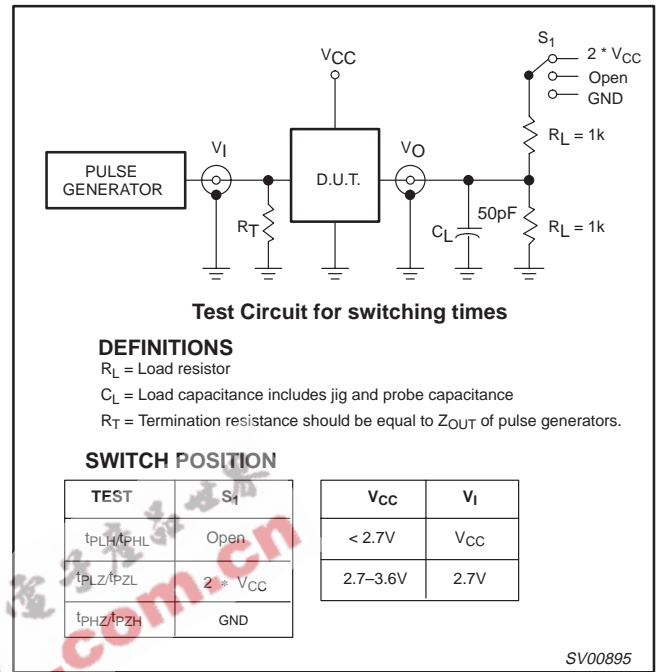


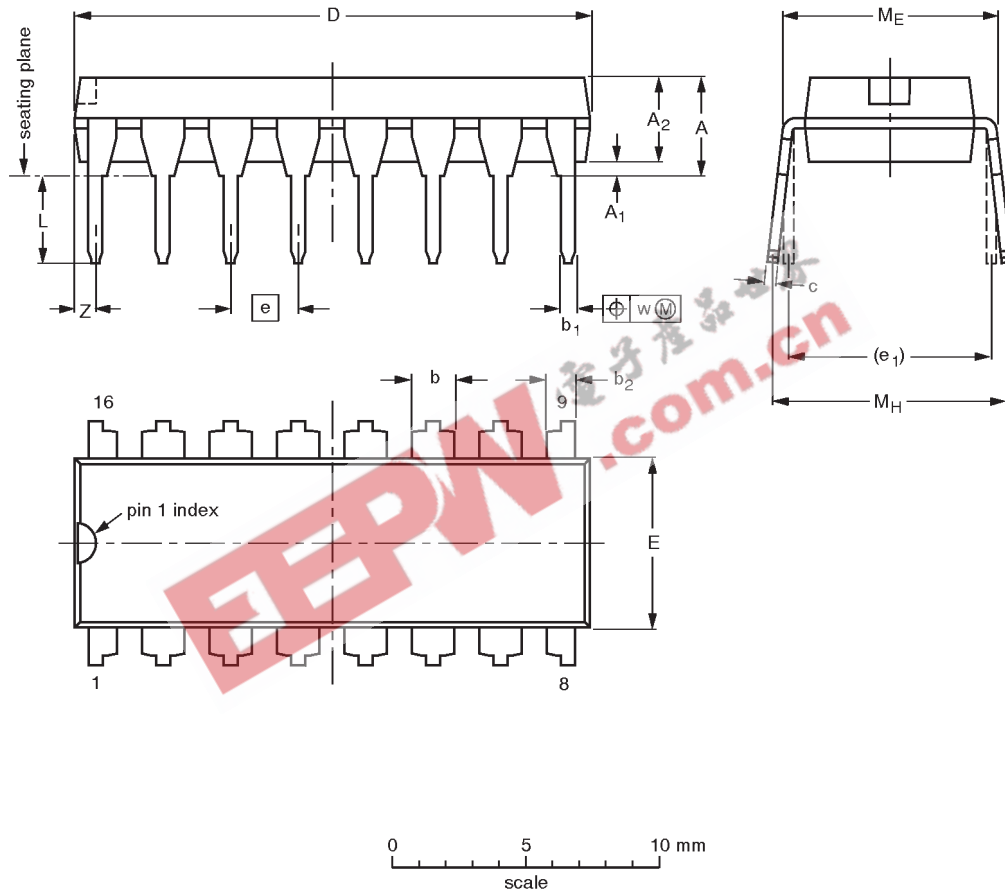
Figure 6. Load circuitry for switching times.

8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

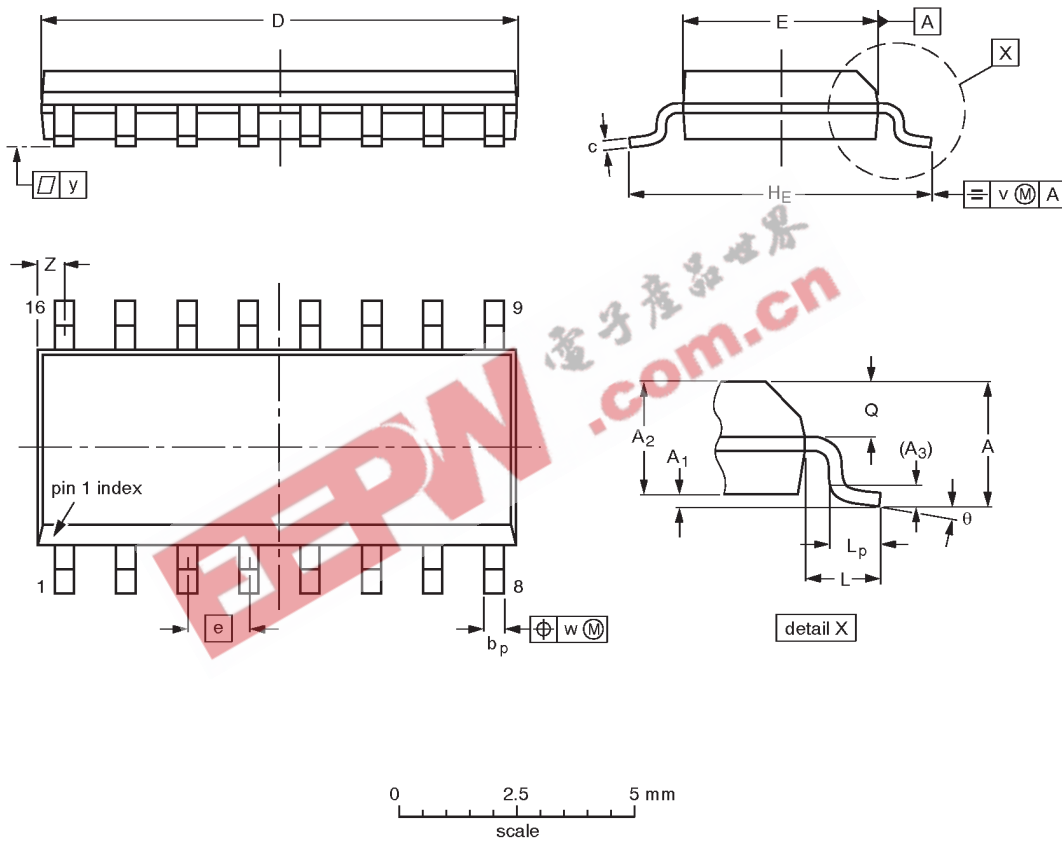
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

74LV595

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

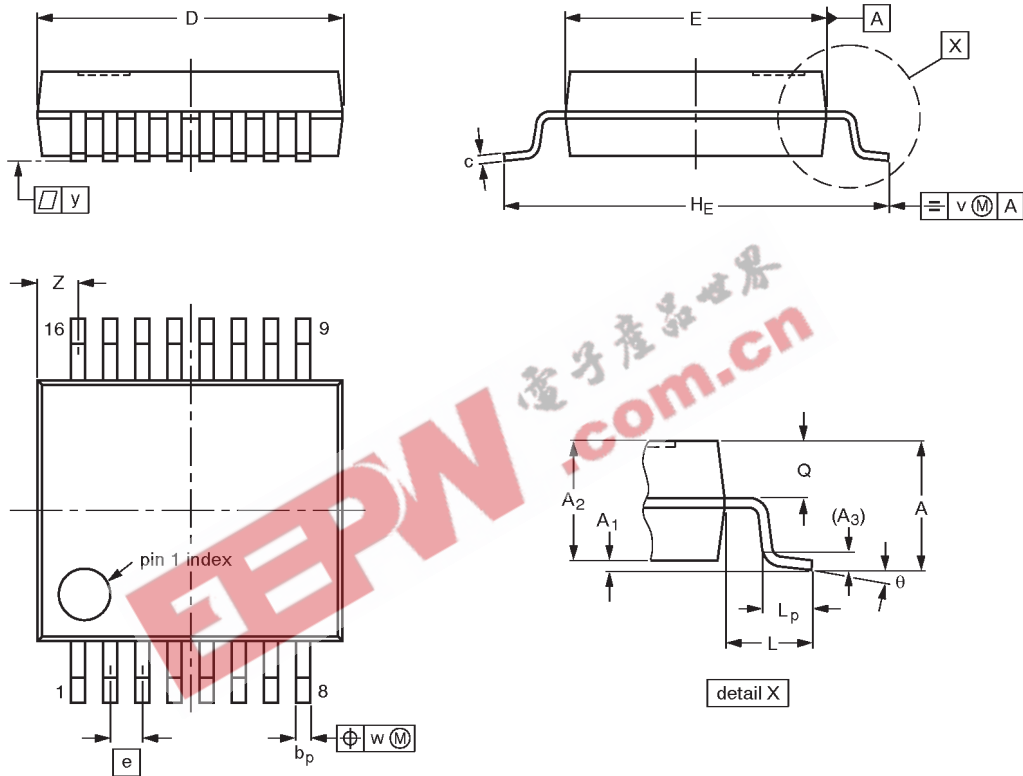
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT109-1	076E07S	MS-012AC			91-08-13 95-01-23

8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

74LV595

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

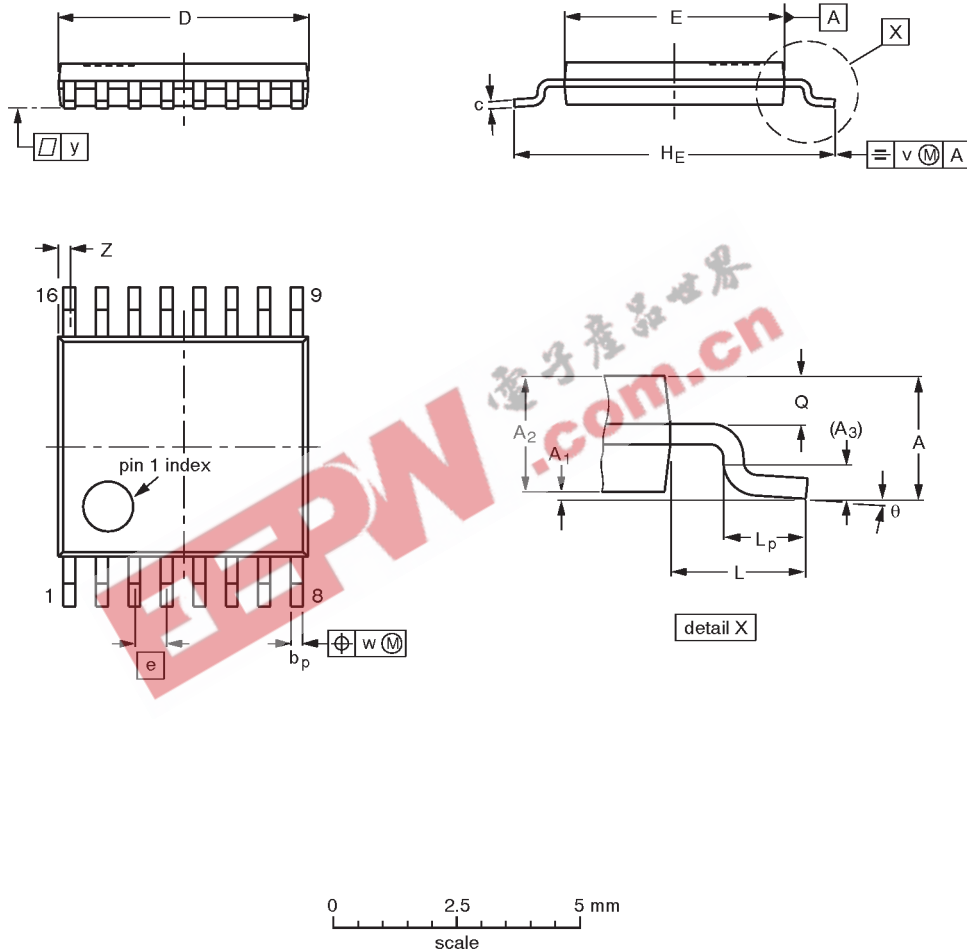
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14 95-02-04

8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

74LV595

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04

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8-bit serial-in/serial or parallel-out shift register  
with output latches (3-State)

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74LV595

NOTES



# 8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

74LV595

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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