INTEGRATED CIRCUITS

DATA SHEET



74LVC10Triple 3-input NAND gate

Product specification Replaces data sheet of 1996 Feb IC24 Data Handbook 1997 Apr 28





Triple 3-input NAND gate

74LVC10

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LVC10 is a high performance, low power, low voltage, Si gate CMOS device and superior to most advanced CMOS compatible

The 74LVC10 provides the 3-input NAND function.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^{\circ}C$; $t_r = t_f \le 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PHL} /t _{PLH}	Propagation delay nA, nB, nC to nY	$C_L = 50 \text{ pF};$ $V_{CC} = 3.3 \text{ V}$	3.9	ns
C _I	Input capacitance	3 15	5.0	pF
C _{PD}	Power dissipation capacitance per gate	$V_I = GND \text{ to } V_{CC}^{-1}$	26	pF
$P_D = C_{PD} \times V_{CC}^2 \times f_i$ $f_i = \text{input frequency in}$	ine the dynamic power dissipation (P_D in $\mu V + \sum (C_L \times V_{CC}^2 \times f_0)$ where: MHz; C_L = output load capacity in pF; in MHz; V_{CC} = supply voltage in V ; sum of the outputs.	v) Com.c		

NOTE:

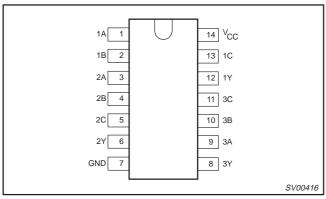
- 1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW) $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum_i (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacity in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V;

 - $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of the outputs.}$

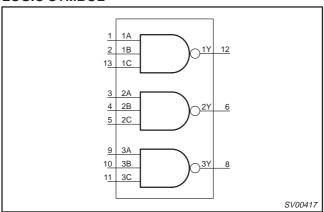
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	-40°C to +85°C	74LVC10 D	74LVC10 D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to +85°C	74LVC10 DB	74LVC10 DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVC10 PW	74LVC10PW DH	SOT402-1

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

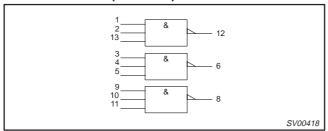
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A – 3A	Data inputs
2, 4, 10	1B – 3B	Data inputs
7	GND	Ground (0 V)
12, 6, 8	1Y – 3Y	Data outputs
13, 5, 11	1C – 3C	Data inputs
14	V _{CC}	Positive supply voltage

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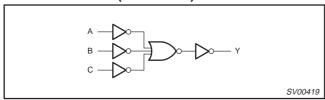
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LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



FUNCTION TABLE

	INPUTS		OUTPUTS
nA	nB	nC	nY
L	L	L	Н
L	L	Н	Н
L	Н	L	Н
L	Н	Н	Н
Н	L	L	Н
Н	L	Н	Н
Н	Н	L	Н
Н	Н	Н	L

NOTES:

H = HIGH voltage level L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

RECOMM	SV00419 ENDED OPERATING CONDITIONS	"是为"。C	0		
SYMBOL	PARAMETER	CONDITIONS	LIN	IITS	UNIT
STWIBOL	PANAIVIETEN	CONDITIONS	MIN	MAX	ONIT
V _{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V _{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	٧
VI	DC input voltage range		0	5.5	V
V _{I/O}	DC input voltage range for I/Os		0	V _{CC}	V
Vo	DC output voltage range		0	V _{CC}	V
T _{amb}	Operating free-air temperature range		-40	+85	°C
t _r , t _f	Input rise and fall times	$V_{CC} = 1.2 \text{ to } 2.7V$ $V_{CC} = 2.7 \text{ to } 3.6V$	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +6.5	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage	Note 2	-0.5 to +5.5	V
V _{I/O}	DC input voltage range for I/Os		-0.5 to V _{CC} +0.5	V
I _{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V _{OUT}	DC output voltage	Note 2	-0.5 to V _{CC} +0.5	V
I _{OUT}	DC output source or sink current	$V_O = 0$ to V_{CC}	±50	mA
I _{GND} , I _{CC}	DC V _{CC} or GND current		±100	mA
T _{stg}	Storage temperature range		-60 to +150	°C
P _{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

- 1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

			L	IMITS		
SYMBOL	PARAMETER	TEST CONDITIONS	Temp = -	40°C to ⋅	°C to +85°C	
			MIN	TYP ¹	MAX	
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	LUCI Lloyed Innut valtage	V _{CC} = 1.2V	V _{CC}			V
V _{IH}	HIGH level Input voltage	V _{CC} = 2.7 to 3.6V	2.0			V
V	LOW/ lovel Input voltage	V _{CC} = 1.2V			GND	V
V _{IL}	LOW level Input voltage	V _{CC} = 2.7 to 3.6V			0.8	l ^v
		$V_{CC} = 2.7V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -12mA$	V _{CC} -0.5			
\ \ \	LUCI Llevel evitavit veltege	$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = -100\mu\text{A}$	V _{CC} -0.2	V _{CC}		
V _{OH}	HIGH level output voltage	$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -12mA$	V _{CC} -0.6			V
		$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -24$ mA	V _{CC} - 1.0			
		$V_{CC} = 2.7V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = 12mA$			0.40	
V _{OL}	LOW level output voltage	$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = 100 \mu A$			0.20	V
		$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = 24\text{mA}$			0.55	
II	Input leakage current	$V_{CC} = 3.6V$; $V_I = 5.5V$ or GND Not for I/O pins		± 0.1	±5	μΑ
I _{IHZ} /I _{ILZ}	Input current for common I/O pins	$V_{CC} = 3.6V$; $V_{I} = V_{CC}$ or GND		± 0.1	± 15	μΑ
I _{OZ}	3-State output OFF-state current	$V_{CC} = 3.6V$; $V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND		0.1	±10	μΑ
I _{CC}	Quiescent supply current	$V_{CC} = 3.6V$; $V_{I} = V_{CC}$ or GND; $I_{O} = 0$		0.1	20	μΑ
Δl _{CC}	Additional quiescent supply current per input pin	$V_{CC} = 2.7V$ to 3.6V; $V_{I} = V_{CC} - 0.6V$; $I_{O} = 0$		5	500	μА

NOTE

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \le 2.5 \text{ ns}$; $C_L = 50 \text{ pF}$

				LIMITS							
SYMBOL	PARAMETER	WAVEFORM	V _{CC}	= 3.3V ±0).3V	V _{CC} =	: 2.7V	V _{CC} = 1.2V	UNIT		
			MIN	TYP ¹	MAX	MIN	MAX	TYP			
t _{PHL} / t _{PLH}	Propagation delay nA, nB, nC to nY	Figures 1, 2	-	3.9	6.4	-	7.5	-	ns		

NOTE:

AC WAVEFORMS

 V_M = 1.5 V at $V_{CC} \ge 2.7$ V V_M = 0.5 • V_{CC} at $V_{CC} < 2.7$ V

 $V_{\mbox{\scriptsize OL}}$ and $V_{\mbox{\scriptsize OH}}$ are the typical output voltage drop that occur with the output load.

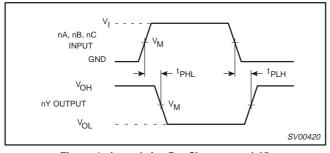


Figure 1. Input (nA, nB, nC) to output (nY) propagation delays.

TEST CIRCUIT

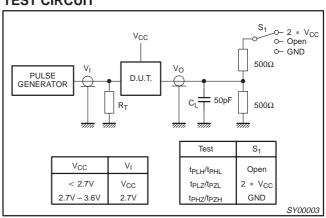


Figure 2. Load circuitry for switching times.

^{1.} All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

^{1.} These typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25$ °C.

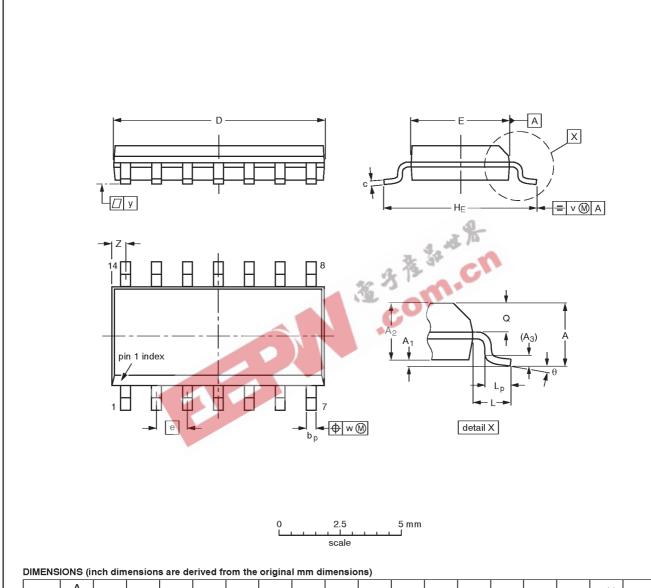
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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Dillin	MENOIONO (mon annensiono are derived nom the original min annensiono)																	
UNIT	A max.	Α1	A ₂	A ₃	bp	ပ	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	٧	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.0098 0.0039		0.01	1	0.0098 0.0075		0.16 0.15	0.050	0.24 0.23	0.041		0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		REFER		EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	PROJECTION	ISSUE DATE		
SOT108-1	076E06\$	MS-012AB				91 08-13 95-01-23

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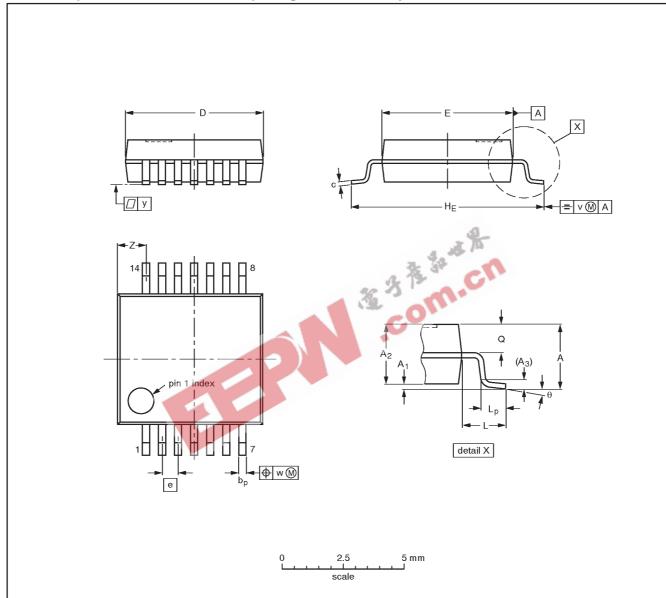
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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

	(-,												
UNIT	A max.	Α ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		EUROPEAN	ISSUE DATE			
VERSION	ERSION IEC JEDEC EIAJ			PROJECTION	ISSUE DATE	
SOT337-1		MO-150AB				-95-02-04 96-01-18

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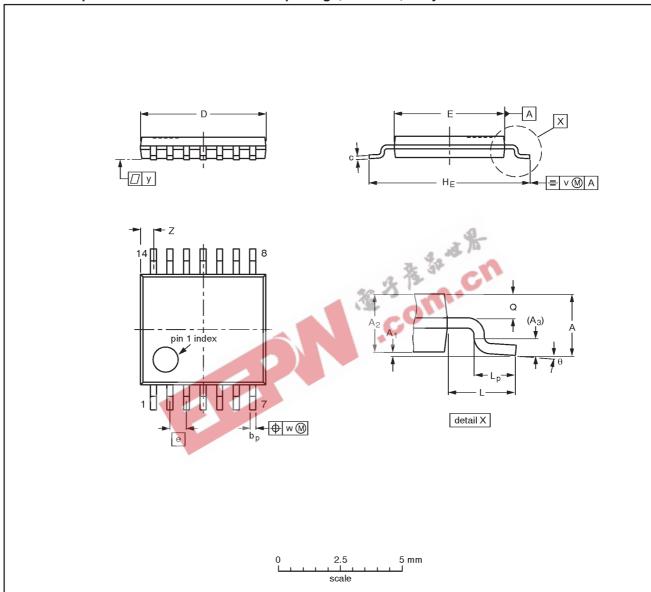
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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

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UNIT	A max.	Α1	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT402-1		MO-153				-94-07-12 95-04-04	

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Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
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