

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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74HC/HCT240

Octal buffer/line driver; 3-state;
inverting

Product specification
File under Integrated Circuits, IC06

December 1990

Octal buffer/line driver; 3-state; inverting

74HC/HCT240

FEATURES

- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT240 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT240 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{1OE}$ and $\overline{2OE}$. A HIGH on \overline{nOE} causes the outputs to assume a high impedance OFF-state. The "240" is identical to the "244" but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n	C _L = 15 pF; V _{CC} = 5 V	9	9	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

ORDERING INFORMATION

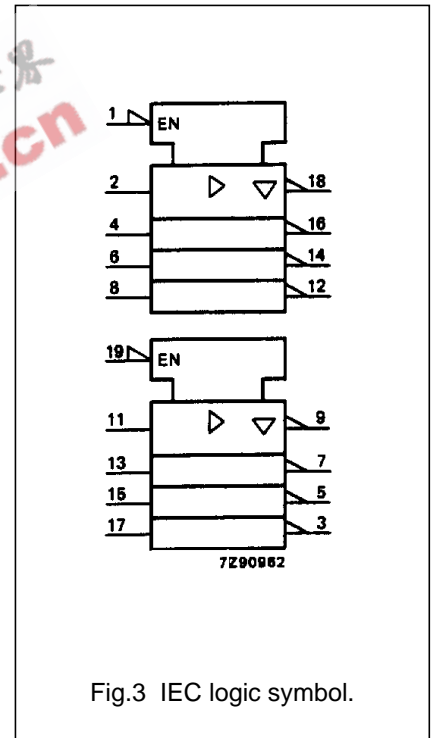
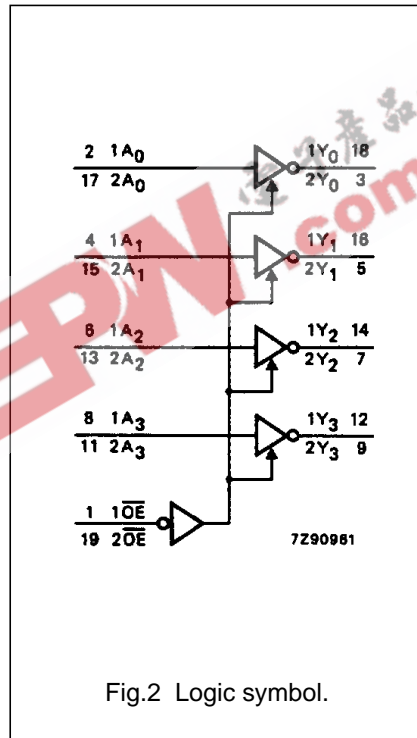
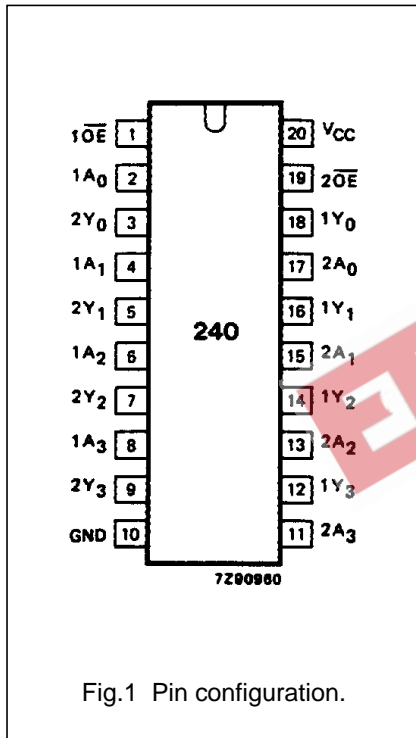
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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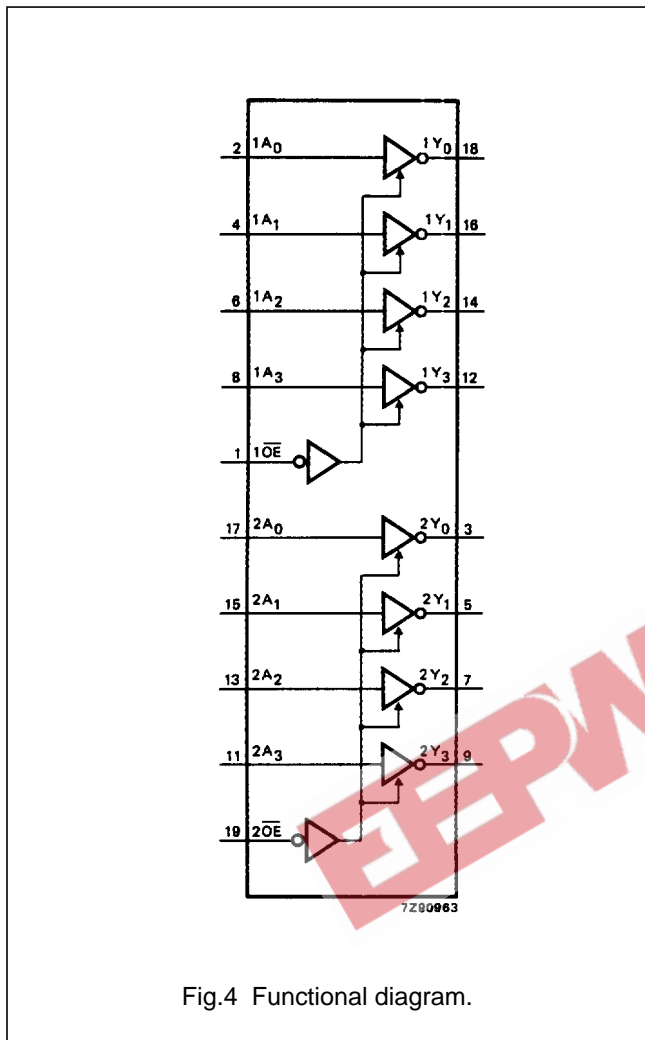
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage



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FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

Notes

1. H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high impedance OFF-state



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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						ns	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n		30 11 9	100 20 17		125 25 21	150 30 26		2.0 4.5 6.0	Fig.5	
t _{PZH} / t _{PZL}	3-state output enable time 1OE to 1Y _n ; 2OE to 2Y _n		39 14 11	150 30 26		190 38 33	225 45 38		2.0 4.5 6.0	Fig.6	
t _{PHZ} / t _{PLZ}	3-state output disable time 1OE to 1Y _n ; 2OE to 2Y _n		41 15 12	150 30 26		190 38 33	225 45 38		2.0 4.5 6.0	Fig.6	
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13	90 18 15		2.0 4.5 6.0	Fig.5	

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1A _n	1.50
2A _n	1.50
1 \overline{OE}	0.70
2 \overline{OE}	0.70

AC CHARACTERISTICS FOR 74HCT

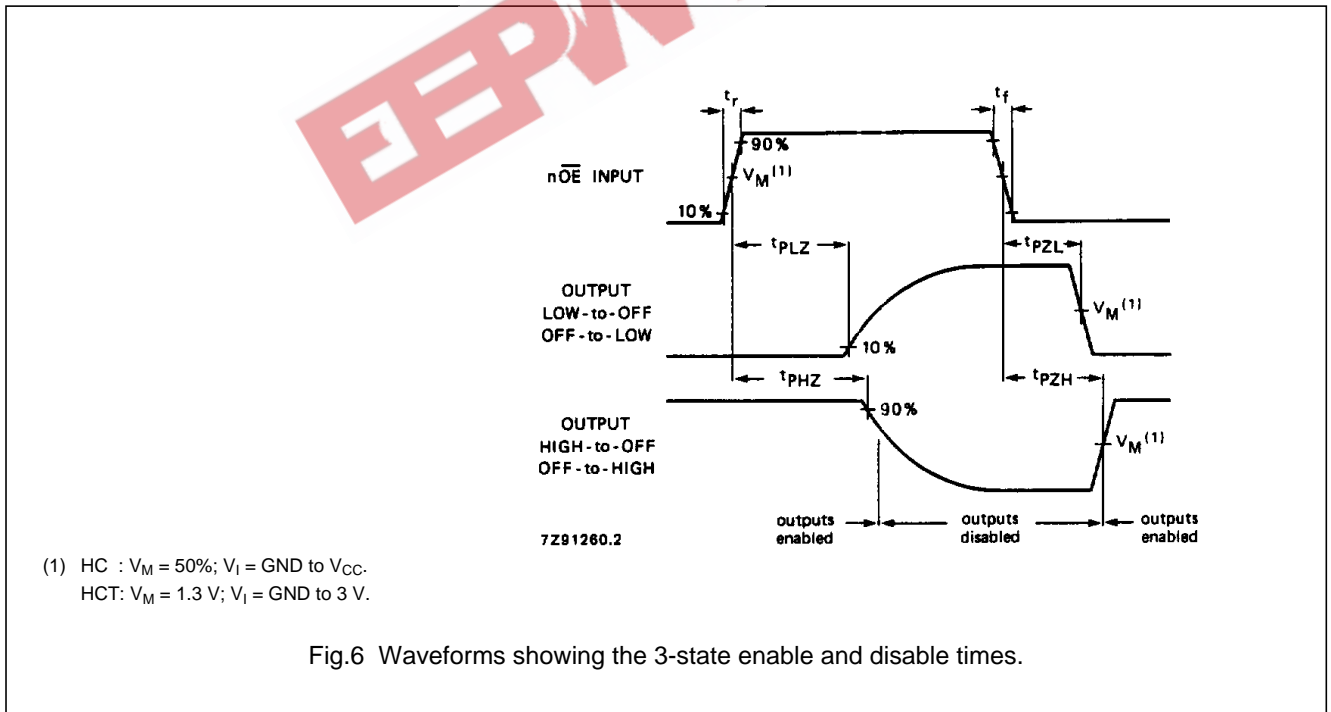
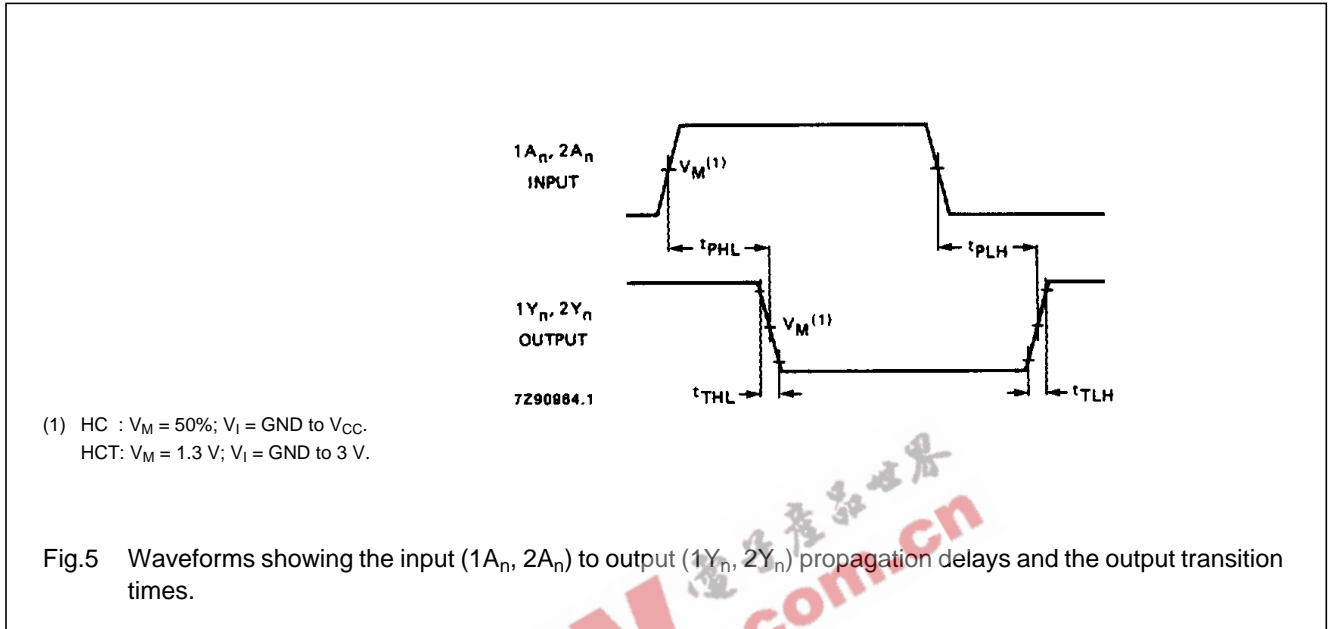
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n		11	20		25		30	ns	4.5	Fig.5
t _{PZH} / t _{PZL}	3-state output enable time 1 \overline{OE} to 1Y _n ; 2 \overline{OE} to 2Y _n		13	30		38		45	ns	4.5	Fig.6
t _{PHZ} / t _{PLZ}	3-state output disable time 1 \overline{OE} to 1Y _n ; 2 \overline{OE} to 2Y _n		13	25		31		38	ns	4.5	Fig.6
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.5

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".