

May 2002 Revised May 2002

74ALVCF322835

Low Voltage 36-Bit Universal Bus Driver with 3.6V Tolerant Outputs and 26 Ω Series Resistors in Outputs

General Description

The 74ALVCF322835 low voltage 36-bit universal bus driver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

Data flow is controlled by output-enable (\overline{OE}) , latch-enable (LE), and clock (CLK) inputs. The device operates in Transparent Mode when LE is held HIGH. The device operates in clocked mode when LE is LOW and CLK is toggled. Data transfers from the Inputs (I_n) to Outputs (O_n) on a Positive Edge Transition of the Clock. When \overline{OE} is LOW, the output data is enabled. When \overline{OE} is HIGH the output port is in a high impedance state.

The 74ALVCF322835 is designed with 26Ω series resistors in the outputs. This design reduces noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74ALVCF322835 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The 74ALVCF322835 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- Compatible with PC133 DIMM module specifications
- \blacksquare 1.65V to 3.6V V_{CC} specifications provided
- 3.6V tolerant outputs
- \blacksquare 26 Ω series resistors in outputs
- t_{PD} (CLK to O_n)
 3.7 ns max for 3.0V to 3.6V V_{CC}
- 4.6 ns max for 2.3V to 2.7V V_{CC}7.4 ns max for 1.65V to 1.95V V_{CC}
- Power-down high impedance outputs
 Latchup conforms to JEDEC JED78
- ESD performance
 - Human body model > 2000V Machine model >200V

Ordering Code:

Order Number	Package Number	Package Description
74ALVCF322835G (Note 1) (Note 2)	BGA114A	114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

Note 1: Ordering Code "G" indicates Trays.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

(Top Thru View)

Pin Descriptions

Pin Names	Description
OE n	Output Enable Input (Active LOW)
LE _n	Latch Enable Input
CLK _n	Clock Input
1I ₁ - 1I ₁₈	Data Inputs
2l ₁ - 2l ₁₈	Data Inputs
10 ₁ - 10 ₁₈ 20 ₁ - 20 ₁₈	3-STATE Outputs
2O ₁ - 2O ₁₈	3-STATE Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
Α	102	101	NC	NC	1I ₁	1l ₂
В	104	103	NC	GND	1l ₃	1I ₄
С	10 ₆	10 ₅	GND	GND	1I ₅	1I ₆
D	1O ₈	107	V _{CC}	V _{CC}	11 ₇	11 ₈
Е	10 ₁₀	10 ₉	GND	GND	1l ₉	1I ₁₀
F	1I ₁₂	10 ₁₁	GND	GND	11 ₁₁	1I ₁₂
G	10 ₁₄	10 ₁₃	V _{CC}	V _{CC}	1I ₁₃	1I ₁₄
Н	10 ₁₅	10 ₁₆	GND	GND	1I ₁₆	1I ₁₅
J	10 ₁₇	10 ₁₈	OE ₁	CLK ₁	1I ₁₈	1I ₁₇
K	NC	NC	LE ₁	GND	NC	NC
L	2O ₂	2O ₁	NC	GND	2l ₁	2l ₂
М	204	2O ₃	GND	GND	2l ₃	2l ₄
N	2O ₆	2O ₅	Vcc	V _{CC}	2l ₅	2l ₆
Р	2O ₈	207	GND	GND	2O ₇	2l ₈
R	2010	20 ₉	GND	GND	2l ₉	2l ₁₀
Т	2O ₁₂	20 ₁₁	V _{CC}	V _{CC}	2l ₁₁	2l ₁₂
U	20 ₁₄	20 ₁₃	GND	GND	2l ₁₃	2l ₁₄
V	2O ₁₅	20 ₁₆	OE ₂	CLK ₂	2I ₁₆	2I ₁₅
W	20 ₁₇	20 ₁₈	LE ₂	GND	2l ₁₈	2l ₁₇

Truth Table

		Inp	Outputs		
Ī	ΟE _n	LEn	CLK _n	In	O _n
ĺ	Н	Х	Х	Х	Z
	L	Н	Χ	L	L
	L	Н	X	Н	Н
	L	L	1	L	L
	L	L	1	Н	Н
	L	L	Н	X	O ₀ (Note 3)
	L	L	L	Χ	O ₀ (Note 4)

- H = Logic HIGH

- T = Logic LOW

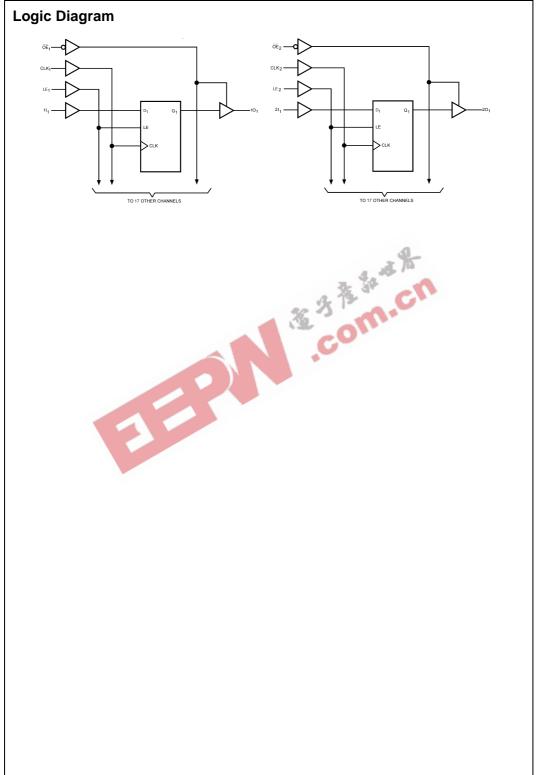
 X = Don't Care, but not floating

 Z = High Impedance

 ↑ = LOW-to-HIGH Clock Transition

Note 3: Output level before the indicated steady-state input conditions were established provided that CLK was HIGH before LE went LOW.

Note 4: Output level before the indicated steady-state input conditions



Absolute Maximum Ratings(Note 5)

DC Input Diode Current (I_{IK})

 $V_I < 0V$ –50 mA

DC Output Diode Current (I_{OK})

V_O < 0V

DC Output Source/Sink Current

 (I_{OH}/I_{OL}) ±50 mA

DC V_{CC} or GND Current per

Supply Pin (I $_{CC}$ or GND) ± 100 mA

Storage Temperature Range (T_{STG}) -65°C to +150°C

Recommended Operating Conditions (Note 7)

Power Supply

-50 mA

 $\begin{array}{ccc} Operating & 1.65 V \ to \ 3.6 V \\ Input \ Voltage & 0 V \ to \ V_{CC} \\ Output \ Voltage \ (V_O) & 0 V \ to \ V_{CC} \\ Free \ Air \ Operating \ Temperature \ (T_A) & -40 ^{\circ} C \ to \ +85 ^{\circ} C \end{array}$

Minimum Input Edge Rate (Δt/ΔV)

 $V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$ 10 ns/V

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage	3 3 7	1.65 - 1.95 2.3 - 2.7 2.7 - 3.6	0.65 x V _{CC} 1.7 2.0		V
V _{IL}	LOW Level Input Voltage	·co	1.65 - 1.95 2.3 - 2.7 2.7 - 3.6		0.35 x V _{CC} 0.7 0.8	V
V _{OH}	HIGH Level Output Voltage	$\begin{aligned} & I_{OH} = -100 \ \mu\text{A} \\ & I_{OH} = -2 \ \text{mA} \\ & I_{OH} = -4 \ \text{mA} \\ & I_{OH} = -6 \ \text{mA} \end{aligned}$	1.65 - 3.6 1.65 2.3 2.3 3.0 2.7	V _{CC} - 0.2 1.2 1.9 1.7 2.4		V
		I _{OH} = -12 mA	3.0	2		
V _{OL}	LOW Level Output Voltage	$\begin{split} I_{OL} &= 100 \ \mu\text{A} \\ I_{OL} &= 2 \ \text{mA} \\ I_{OL} &= 4 \ \text{mA} \\ I_{OL} &= 6 \ \text{mA} \end{split}$	1.65 - 3.6 1.65 2.3 2.3 3.0		0.2 0.45 0.4 0.55 0.55	V
		$I_{OL} = 8 \text{ mA}$ $I_{OL} = 12 \text{ mA}$	2.7 3.0		0.6	
I _{OH}	High Level Output Current		1.65 2.3 2.7 3.0		-2 -6 -8 -12	mA
I _{OL}	Low Level Output Current		1.65 2.3 2.7 3.0		2 6 8 12	mA
I	Input Leakage Current	$0 \le V_1 \le 3.6V$	1.65 - 3.6		±5.0	μΑ
l _{oz}	3-STATE Output Leakage	$0 \le V_O \le 3.6V$, $V_I = V_{IH}$ or V_{IL}	1.65 - 3.6		±10	μА
loff	Power Off Leakage Current	$0V \le (V_1, V_0) \le 3.6V$	0		10	mA
I _{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	μΑ
Δl _{CC}	Increase in I _{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7 - 3.6		750	μА

AC Electrical Characteristics

	Parameter		$T_A = -40^{\circ}C$ to $+85^{\circ}C$, $R_L = 500\Omega$							
Symbol			C _L = 50 pF			C _L = 30 pF				Units
	Parameter	V _{CC} = 3.	$V_{CC} = 3.3V \pm 0.3V$		V _{CC} = 2.7V		$\textrm{V}_{\textrm{CC}}=\textrm{2.5}\pm\textrm{0.2V}$		$V_{CC}=1.8V\pm0.15V$	
		Min	Max	Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	250		200		200		100		MHz
t _{PHL} , t _{PLH}	Propagation Delay	4.4	2.0	4.0	4.5		4.0			
Bus-to-Bus	1.1	3.6	1.3	4.5	0.8	4.0	1.5	7.2	ns	
t _{PHL} , t _{PLH}	Propagation Delay	1.5	3.7	2.0	4.0	4.5	4.1	2.0	7.4	
	Clock to Bus	1.5	3.7	2.0	4.6	1.5	4.1	2.0	7.4	ns
t _{PHL} , t _{PLH}	Propagation Delay	1.1	1.1 4.2	1.3	5.2	0.8	4.7	1.5	8.5	ns
	LE to Bus	1.1	4.2	1.3	5.2	0.8	4.7	1.5	8.5	ns
t _{PZL} , t _{PZH}	Output Enable Time	1.1	4.8	1.3	6.4	0.8	5.9	1.5	9.8	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	1.1	4.7	1.3	5.2	0.8	4.7	1.5	7.9	ns
t _S	Setup Time	1.5		1.5		1.5	48	2.5		ns
t _H	Hold Time	0.7		0.7		0.7	JE I	1.0		ns
t _W	Pulse Width	1.5		1.5		1.5		4.0		ns

Capacitance

Compleal	Parameter		Conditions	$T_A = +25^{\circ}C$		Units
Symbol			Conditions	V _{CC}	Typical	Units
C _{IN}	Input Capacitance		$V_I = 0V$ or V_{CC}	3.3	3.5	pF
C _{OUT}	Output Capacitance		$V_I = 0V \text{ or } V_{CC}$	3.3	5.5	pF
C _{PD}	Power Dissipation Capacitance	Outputs Enabled	$f = 10 \text{ MHz}, C_L = 0 \text{ pF}$	3.3	13	pF
				2.5	13	ρı

I_{OUT} - V_{OUT} Characteristics

TEST DUT CL 5

FIGURE 1. Characteristics for Output - Pull Up Drive

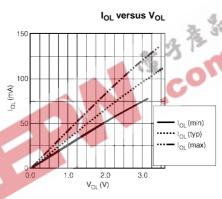


FIGURE 2. Characteristics for Output - Pull Down Driver

AC Loading and Waveforms

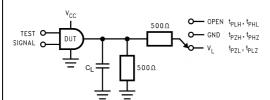


Table 1: Values for Figure 1

TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t_{PZL} , t_{PLZ}	V _L
t _{PZH} , t _{PHZ}	GND

FIGURE 3. AC Test Circuit

Table 2: Variable Matrix (Input Characteristics: f = 1MHz; t_r = t_f = 2ns; Z_0 = 50 Ω)

Symbol	V _{CC}						
Oyillboi -	$\textbf{3.3V} \pm \textbf{0.3V}$	2.7V	2.5V ± 0.2V	1.8V ± 0.15V			
V_{mi}	1.5V	1.5V	V _{CC} /2	V _{CC} /2			
V_{mo}	1.5V	1.5V	V _{CC} /2	V _{CC} /2			
V_X	V _{OL} + 0.3V	V _{OL} + 0.3V	V _{OL} + 0.15V	V _{OL} + 0.15V			
V_{Y}	V _{OH} – 0.3V	V _{OH} – 0.3V	V _{OH} – 0.15V	V _{OH} – 0.15V			
V_L	6V	6V	V _{CC} *2	V _{CC} *2			

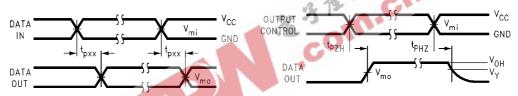


FIGURE 4. Waveform for Inverting and Non-inverting Functions

FIGURE 5. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

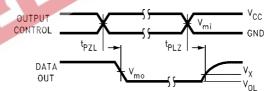
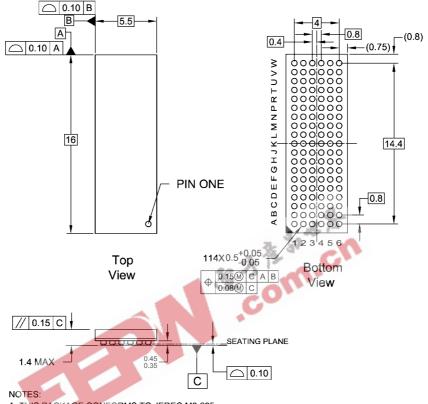


FIGURE 6. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Outputs

Physical Dimensions inches (millimeters) unless otherwise noted



- A. THIS PACKAGE CONFORMS TO JEDEC M0-205

 B. ALL DIMENSIONS IN MILLIMETERS

 C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)

 .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA114ArevE

56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD56

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