

## 74ALVCF322835

### Low Voltage 36-Bit Universal Bus Driver with 3.6V Tolerant Outputs and 26Ω Series Resistors in Outputs

#### General Description

The 74ALVCF322835 low voltage 36-bit universal bus driver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

Data flow is controlled by output-enable ( $\overline{OE}$ ), latch-enable (LE), and clock (CLK) inputs. The device operates in Transparent Mode when LE is held HIGH. The device operates in clocked mode when LE is LOW and CLK is toggled. Data transfers from the Inputs ( $I_n$ ) to Outputs ( $O_n$ ) on a Positive Edge Transition of the Clock. When  $\overline{OE}$  is LOW, the output data is enabled. When  $\overline{OE}$  is HIGH the output port is in a high impedance state.

The 74ALVCF322835 is designed with 26Ω series resistors in the outputs. This design reduces noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74ALVCF322835 is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O capability up to 3.6V.

The 74ALVCF322835 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

- Compatible with PC133 DIMM module specifications
- 1.65V to 3.6V  $V_{CC}$  specifications provided
- 3.6V tolerant outputs
- 26Ω series resistors in outputs
- $t_{PD}$  (CLK to  $O_n$ )
  - 3.7 ns max for 3.0V to 3.6V  $V_{CC}$
  - 4.6 ns max for 2.3V to 2.7V  $V_{CC}$
  - 7.4 ns max for 1.65V to 1.95V  $V_{CC}$
- Power-down high impedance outputs
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model >200V

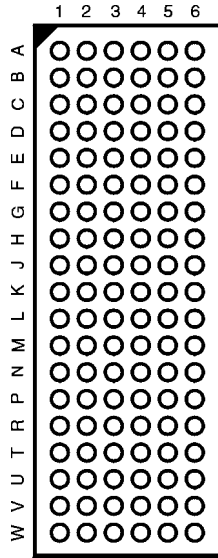
#### Ordering Code:

Order Number	Package Number	Package Description
74ALVCF322835G (Note 1) (Note 2)	BGA114A	114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

**Note 1:** Ordering Code "G" indicates Trays.

**Note 2:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



(Top Thru View)

FBGA Pin Assignments

	1	2	3	4	5	6
A	1O <sub>2</sub>	1O <sub>1</sub>	NC	NC	1I <sub>1</sub>	1I <sub>2</sub>
B	1O <sub>4</sub>	1O <sub>3</sub>	NC	GND	1I <sub>3</sub>	1I <sub>4</sub>
C	1O <sub>6</sub>	1O <sub>5</sub>	GND	GND	1I <sub>5</sub>	1I <sub>6</sub>
D	1O <sub>8</sub>	1O <sub>7</sub>	V <sub>CC</sub>	V <sub>CC</sub>	1I <sub>7</sub>	1I <sub>8</sub>
E	1O <sub>10</sub>	1O <sub>9</sub>	GND	GND	1I <sub>9</sub>	1I <sub>10</sub>
F	1I <sub>12</sub>	1O <sub>11</sub>	GND	GND	1I <sub>11</sub>	1I <sub>12</sub>
G	1O <sub>14</sub>	1O <sub>13</sub>	V <sub>CC</sub>	V <sub>CC</sub>	1I <sub>13</sub>	1I <sub>14</sub>
H	1O <sub>15</sub>	1O <sub>16</sub>	GND	GND	1I <sub>16</sub>	1I <sub>15</sub>
J	1O <sub>17</sub>	1O <sub>18</sub>	$\overline{OE}_1$	CLK <sub>1</sub>	1I <sub>18</sub>	1I <sub>17</sub>
K	NC	NC	LE <sub>1</sub>	GND	NC	NC
L	2O <sub>2</sub>	2O <sub>1</sub>	NC	GND	2I <sub>1</sub>	2I <sub>2</sub>
M	2O <sub>4</sub>	2O <sub>3</sub>	GND	GND	2I <sub>3</sub>	2I <sub>4</sub>
N	2O <sub>6</sub>	2O <sub>5</sub>	V <sub>CC</sub>	V <sub>CC</sub>	2I <sub>5</sub>	2I <sub>6</sub>
P	2O <sub>8</sub>	2O <sub>7</sub>	GND	GND	2O <sub>7</sub>	2I <sub>8</sub>
R	2O <sub>10</sub>	2O <sub>9</sub>	GND	GND	2I <sub>9</sub>	2I <sub>10</sub>
T	2O <sub>12</sub>	2O <sub>11</sub>	V <sub>CC</sub>	V <sub>CC</sub>	2I <sub>11</sub>	2I <sub>12</sub>
U	2O <sub>14</sub>	2O <sub>13</sub>	GND	GND	2I <sub>13</sub>	2I <sub>14</sub>
V	2O <sub>15</sub>	2O <sub>16</sub>	$\overline{OE}_2$	CLK <sub>2</sub>	2I <sub>16</sub>	2I <sub>15</sub>
W	2O <sub>17</sub>	2O <sub>18</sub>	LE <sub>2</sub>	GND	2I <sub>18</sub>	2I <sub>17</sub>

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
LE <sub>n</sub>	Latch Enable Input
CLK <sub>n</sub>	Clock Input
1I <sub>1</sub> - 1I <sub>18</sub>	Data Inputs
2I <sub>1</sub> - 2I <sub>18</sub>	Data Inputs
1O <sub>1</sub> - 1O <sub>18</sub>	3-STATE Outputs
2O <sub>1</sub> - 2O <sub>18</sub>	3-STATE Outputs

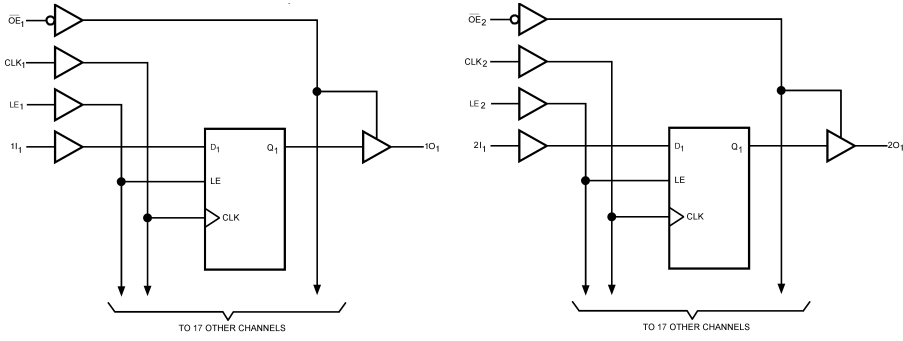
Truth Table

Inputs				Outputs
$\overline{OE}_n$	LE <sub>n</sub>	CLK <sub>n</sub>	I <sub>n</sub>	O <sub>n</sub>
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	O <sub>0</sub> (Note 3)
L	L	L	X	O <sub>0</sub> (Note 4)

H = Logic HIGH  
 L = Logic LOW  
 X = Don't Care, but not floating  
 Z = High Impedance  
 ↑ = LOW-to-HIGH Clock Transition

**Note 3:** Output level before the indicated steady-state input conditions were established provided that CLK was HIGH before LE went LOW.  
**Note 4:** Output level before the indicated steady-state input conditions were established.

### Logic Diagram



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Absolute Maximum Ratings (Note 5)		Recommended Operating Conditions (Note 7)	
Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V	Power Supply	
DC Input Voltage ( $V_I$ )	-0.5V to 4.6V	Operating	1.65V to 3.6V
Output Voltage ( $V_O$ ) (Note 6)	-0.5V to $V_{CC} + 0.5V$	Input Voltage	0V to $V_{CC}$
DC Input Diode Current ( $I_{IK}$ )		Output Voltage ( $V_O$ )	0V to $V_{CC}$
$V_I < 0V$	-50 mA	Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
DC Output Diode Current ( $I_{OK}$ )		Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_O < 0V$	-50 mA	$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	10 ns/V
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA	<b>Note 5:</b> The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.	
DC $V_{CC}$ or GND Current per Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA	<b>Note 6:</b> $I_O$ Absolute Maximum Rating must be observed.	
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C	<b>Note 7:</b> Floating or unused control inputs must be held HIGH or LOW.	

### DC Electrical Characteristics

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6	$0.65 \times V_{CC}$ 1.7 2.0		V
$V_{IL}$	LOW Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6		$0.35 \times V_{CC}$ 0.7 0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -2$ mA $I_{OH} = -4$ mA $I_{OH} = -6$ mA $I_{OH} = -8$ mA $I_{OH} = -12$ mA	1.65 - 3.6 1.65 2.3 3.0 2.7 3.0	$V_{CC} - 0.2$ 1.2 1.9 1.7 2 2		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$ $I_{OL} = 2$ mA $I_{OL} = 4$ mA $I_{OL} = 6$ mA $I_{OL} = 8$ mA $I_{OL} = 12$ mA	1.65 - 3.6 1.65 2.3 3.0 2.7 3.0		0.2 0.45 0.4 0.55 0.55 0.6 0.8	V
$I_{OH}$	High Level Output Current		1.65 2.3 2.7 3.0		-2 -6 -8 -12	mA
$I_{OL}$	Low Level Output Current		1.65 2.3 2.7 3.0		2 6 8 12	mA
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	1.65 - 3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ , $V_I = V_{IH}$ or $V_{IL}$	1.65 - 3.6		$\pm 10$	$\mu A$
$I_{OFF}$	Power Off Leakage Current	$0V \leq (V_I, V_O) \leq 3.6V$	0		10	mA
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	$\mu A$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	2.7 - 3.6		750	$\mu A$

AC Electrical Characteristics										
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, R_L = 500\Omega$								Units
		$C_L = 50\text{ pF}$				$C_L = 30\text{ pF}$				
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5 \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency	250		200		200		100		MHz
$t_{PHL}, t_{PLH}$	Propagation Delay Bus-to-Bus	1.1	3.6	1.3	4.5	0.8	4.0	1.5	7.2	ns
$t_{PHL}, t_{PLH}$	Propagation Delay Clock to Bus	1.5	3.7	2.0	4.6	1.5	4.1	2.0	7.4	ns
$t_{PHL}, t_{PLH}$	Propagation Delay LE to Bus	1.1	4.2	1.3	5.2	0.8	4.7	1.5	8.5	ns
$t_{PZL}, t_{PZH}$	Output Enable Time	1.1	4.8	1.3	6.4	0.8	5.9	1.5	9.8	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time	1.1	4.7	1.3	5.2	0.8	4.7	1.5	7.9	ns
$t_S$	Setup Time	1.5		1.5		1.5		2.5		ns
$t_H$	Hold Time	0.7		0.7		0.7		1.0		ns
$t_W$	Pulse Width	1.5		1.5		1.5		4.0		ns
Capacitance										
Symbol	Parameter	Conditions	$T_A = +25^\circ\text{C}$		Units					
			$V_{CC}$	Typical						
$C_{IN}$	Input Capacitance	$V_I = 0V \text{ or } V_{CC}$	3.3	3.5	pF					
$C_{OUT}$	Output Capacitance	$V_I = 0V \text{ or } V_{CC}$	3.3	5.5	pF					
$C_{PD}$	Power Dissipation Capacitance	Outputs Enabled $f = 10\text{ MHz}, C_L = 0\text{ pF}$	3.3	13	pF					
			2.5	13						

### I<sub>OUT</sub> - V<sub>OUT</sub> Characteristics

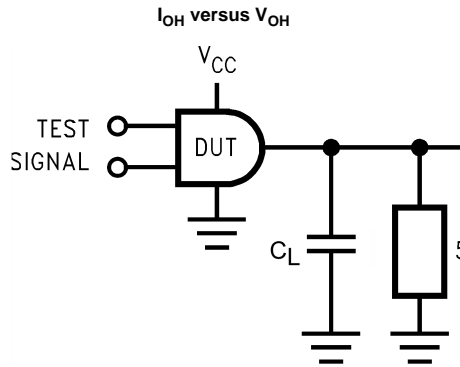


FIGURE 1. Characteristics for Output - Pull Up Drive

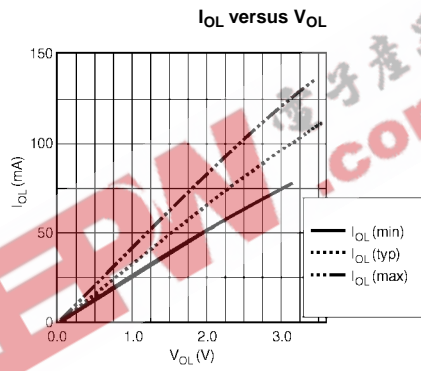


FIGURE 2. Characteristics for Output - Pull Down Driver

### AC Loading and Waveforms

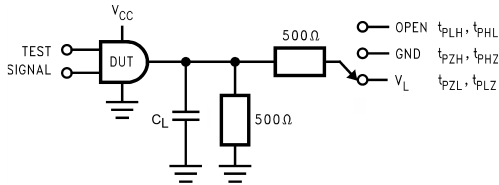


FIGURE 3. AC Test Circuit

Table 1: Values for Figure 1

TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$V_L$
$t_{PZH}$ , $t_{PHZ}$	GND

Table 2: Variable Matrix  
(Input Characteristics:  $f = 1\text{MHz}$ ;  $t_r = t_f = 2\text{ns}$ ;  $Z_0 = 50\Omega$ )

Symbol	$V_{CC}$			
	$3.3\text{V} \pm 0.3\text{V}$	2.7V	$2.5\text{V} \pm 0.2\text{V}$	$1.8\text{V} \pm 0.15\text{V}$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.15\text{V}$	$V_{OL} + 0.15\text{V}$
$V_Y$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.15\text{V}$	$V_{OH} - 0.15\text{V}$
$V_L$	6V	6V	$V_{CC} * 2$	$V_{CC} * 2$

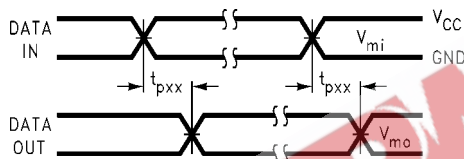


FIGURE 4. Waveform for Inverting and Non-inverting Functions

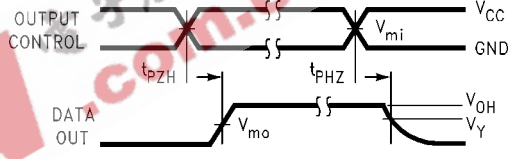


FIGURE 5. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

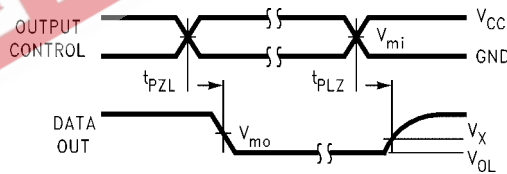


FIGURE 6. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

