FAIRCHILD SEMICONDUCTOR™

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74LVTH652
Low Voltage Octal Transceiver/Register with 3-STATE Outputs

General Description

The LVTH652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function. (See Functional Description).

The LVTH652 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

This octal transceiver/register is designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH652 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

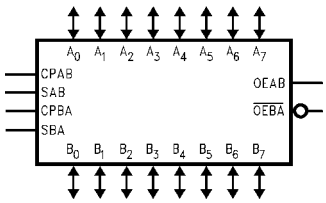
- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Functionally compatible with the 74 series 652
- Latch-up performance exceeds 500 mA

Ordering Code:

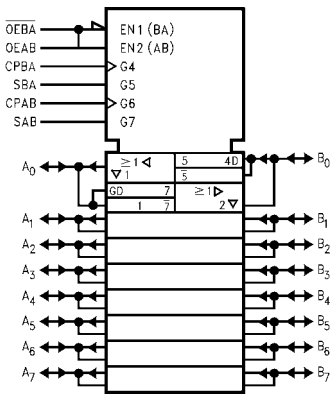
Order Number	Package Number	Package Description
74LVTH652WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVTH652MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



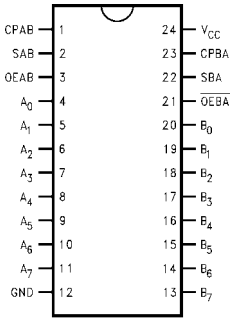
IEEE/IEC



Pin Descriptions

Pin Names	Description
A_0–A_7	Data Register A Inputs/ 3-STATE Outputs
B_0–B_7	Data Register B Inputs/ 3-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

Connection Diagram



Truth Table

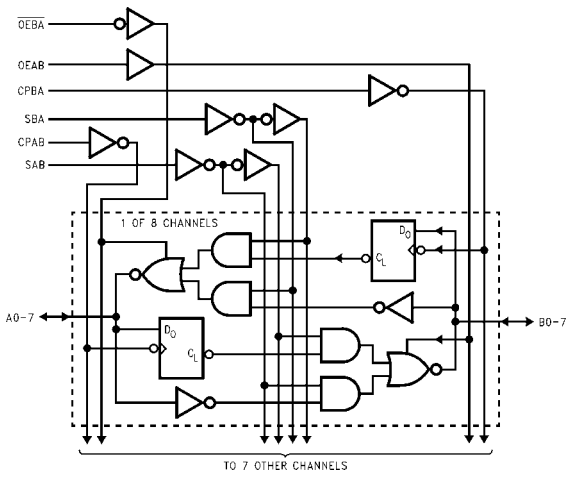
(Note 1)

Inputs						Inputs/Outputs		Operating Mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↗	↗	X	X			Store A and B Data
X	H	↗	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↗	↗	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↗	X	X	Not Specified	Input	Hold A, Store B
L	L	↗	↗	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial ↗ = LOW to HIGH Clock Transition

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

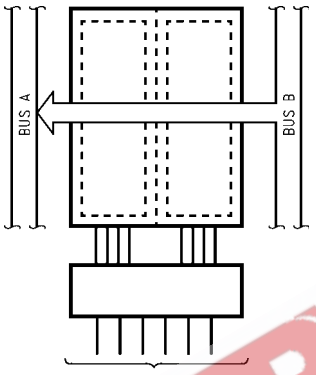
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) controls can multiplex stored and real-time.

The examples below demonstrate the four fundamental bus-management functions that can be performed with the LVTH652.

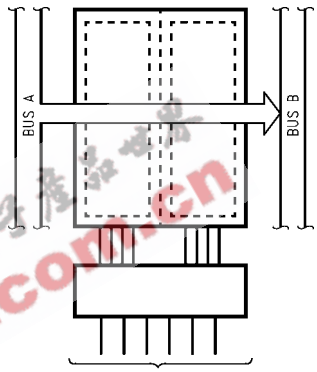
Data on the A or B data bus, or both can be stored in the internal D-type flip-flop by LOW-to-HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Real-Time Transfer
Bus B to Bus A



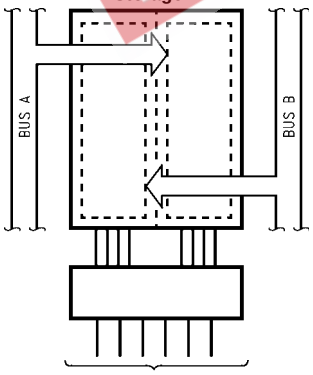
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus A to Bus B



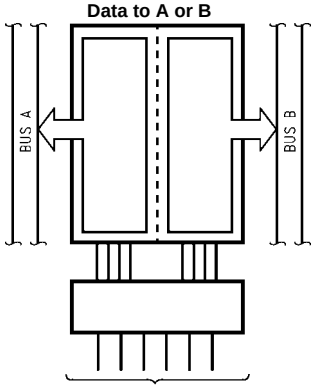
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

Storage



OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Transfer Storage
Data to A or B



OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to +7.0	Output in HIGH or LOW State (Note 3)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH Level Output Current		−32	mA
I_{OL}	LOW Level Output Current		64	mA
T_A	Free-Air Operating Temperature	−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note 2: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 3: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	$T_A = -40°C$ to $+85°C$ Max	Units	Conditions
V_{IK}	Input Clamp Diode Voltage		2.7		−1.2	V	$I_I = -18$ mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0		V	$V_O \le 0.1V$ or
V_{IL}	Input LOW Voltage		2.7–3.6		0.8		$V_O \ge V_{CC} - 0.1V$
V_{OH}	Output HIGH Voltage		2.7–3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100$ µA
			2.7	2.4		V	$I_{OH} = -8$ mA
			3.0	2.0		V	$I_{OH} = -32$ mA
V_{OL}	Output LOW Voltage		2.7		0.2	V	$I_{OL} = 100$ µA
			2.7		0.5	V	$I_{OL} = 24$ mA
			3.0		0.4	V	$I_{OL} = 16$ mA
			3.0		0.5	V	$I_{OL} = 32$ mA
			3.0		0.55	V	$I_{OL} = 64$ mA
$I_{I(HOLD)}$	Bushold Input Minimum Drive		3.0	75		µA	$V_I = 0.8V$
				−75		µA	$V_I = 2.0V$
$I_{I(OD)}$	Bushold Input Over-Drive		3.0	500		µA	(Note 4)
	Current to Change State			−500		µA	(Note 5)
I_I	Input Current		3.6		10	µA	$V_I = 5.5V$
		Control Pins	3.6		±1	µA	$V_I = 0V$ or V_{CC}
		Data Pins	3.6		−5	µA	$V_I = 0V$
					1	µA	$V_I = V_{CC}$
I_{OFF}	Power OFF Leakage Current		0		±100	µA	$0V \le V_I$ or $V_O \le 5.5V$
$I_{PU/PD}$	Power Up/Down 3-STATE		0–1.5V		±100	µA	$V_O = 0.5V$ to $3.0V$
	Output Current						V_I = GND or V_{CC}
I_{OZL}	3-STATE Output Leakage Current		3.6		−5	µA	$V_O = 0.0V$
I_{OZH}	3-STATE Output Leakage Current		3.6		5	µA	$V_O = 3.6V$
I_{OZH+}	3-STATE Output Leakage Current		3.6		10	µA	$V_{CC} < V_O \le 5.5V$
I_{CCH}	Power Supply Current		3.6		0.19	mA	Outputs HIGH
I_{CCL}	Power Supply Current		3.6		5	mA	A or B Port Outputs LOW
I_{CCZ}	Power Supply Current		3.6		0.19	mA	Outputs Disabled
I_{CCZ+}	Power Supply Current		3.6		0.19	mA	$V_{CC} \le V_O \le 5.5V$
							Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current		3.6		0.2	mA	One Input at $V_{CC} - 0.6V$
	(Note 6)						Other Inputs at V_{CC} or GND

Note 4: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 6: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 7)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 8)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 8)

Note 7: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 8: Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150		150		MHz
t_{PLH}	Propagation Delay Data to Output	1.8	5.6	1.8	6.2	ns
t_{PHL}	Clock to A or B	1.8	4.8	1.8	5.6	
t_{PLH}	Propagation Delay Data to Output	1.3	4.5	1.3	4.9	ns
t_{PHL}	Data to A or B	1.3	4.6	1.3	5.2	
t_{PLH}	Propagation Delay Data to Output	1.5	5.5	1.5	6.4	ns
t_{PHL}	SBA or SAB to A or B	1.5	5.4	1.5	6.1	
t_{PZH}	Output Enable Time	1.1	5.2	1.1	6.5	ns
t_{PZL}	$\overline{OE}$ to A	1.1	5.6	1.1	6.6	
t_{PHZ}	Output Disable Time	2.0	5.5	2.0	6.1	ns
t_{PLZ}	$\overline{OE}$ to A	2.0	5.5	2.0	5.9	
t_{PZH}	Output Enable Time	1.3	4.9	1.3	5.7	ns
t_{PZL}	OE to B	1.3	5.3	1.3	5.8	
t_{PHZ}	Output Disable Time	1.5	5.6	1.5	6.7	ns
t_{PLZ}	OE to B	1.5	5.6	1.5	6.3	
t_W	Pulse Duration — Clock HIGH or LOW	3.3		3.3		ns
t_S	Setup Time — Data HIGH before CP	1.2		1.5		ns
	Data LOW before CP	1.6		2.2		
t_H	Hold Time — Data HIGH or LOW after CP	0.8		0.8		ns
t_{OSHL}	Output to Output Skew		1.0		1.0	ns
t_{OSLH}	(Note 9)		1.0		1.0	

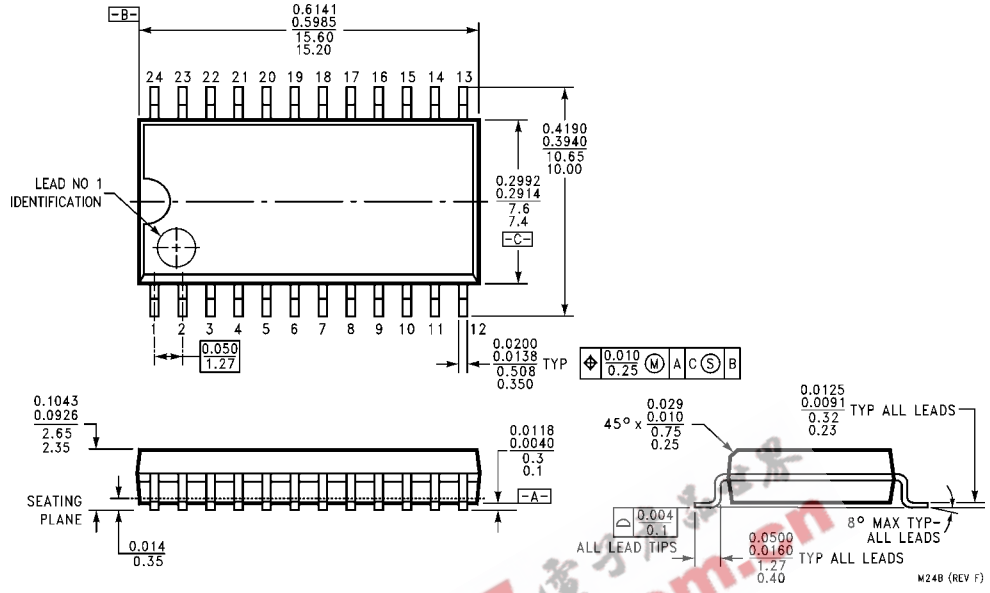
Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 10)

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}	4	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}	8	pF

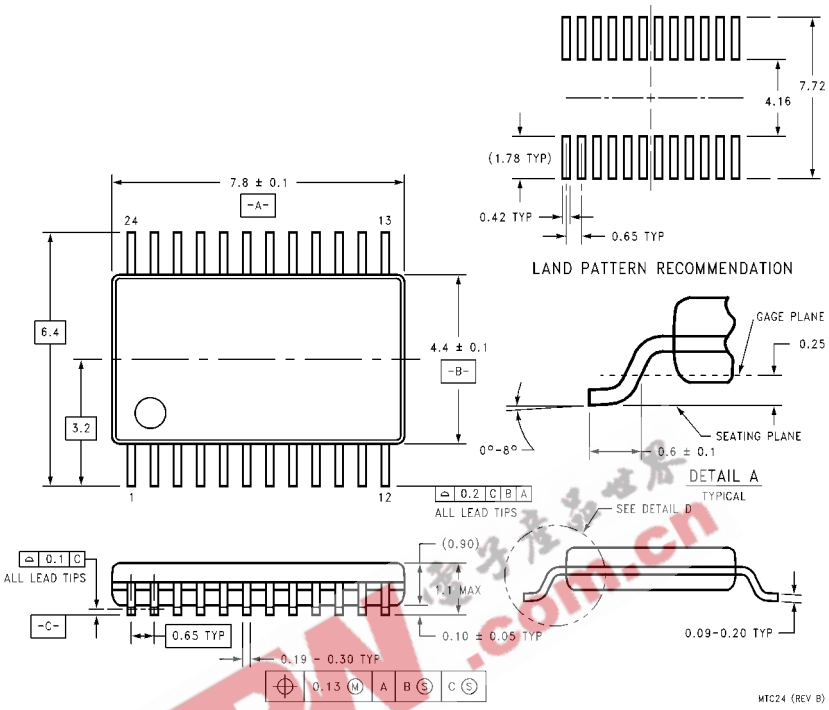
Note 10: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead (0.300' Wide) Molded Small Outline Package, SOIC JEDEC
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Molded Small Outline Package, TSSOP JEDEC
Package Number MTC24

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