

## 8-bit transceiver with 9-bit parity checker/ generator and flag latch (3-State)

# 74ABT853

### FEATURES

- Low static and dynamic power dissipation with high speed and high output drive
- Open-collector  $\overline{\text{ERROR}}$  output
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted

### DESCRIPTION

The 74ABT853 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT853 is an octal transceiver with a parity generator/checker and is intended for bus-oriented applications.

When Output Enable A ( $\overline{\text{OEA}}$ ) is High, it will place the A outputs in a high impedance state. Output Enable B ( $\overline{\text{OEB}}$ ) controls the B outputs in the same way.

The parity generator creates an odd parity output (PARITY) when  $\overline{\text{OEB}}$  is Low. When  $\overline{\text{OEA}}$  is Low, the parity of the B port, including the PARITY input, is checked for odd parity. When an error is detected, the error data is sent to the input of a latch. The error data can then be passed, stored, cleared, or sampled depending on the  $\overline{\text{ENABLE}}$  and  $\overline{\text{CLEAR}}$  control signals.

If both  $\overline{\text{OEA}}$  and  $\overline{\text{OEB}}$  are Low, data will flow from the A bus to the B bus and the part is forced into an error condition which creates an inverted PARITY output. This error condition can be used by the designer for system diagnostics.

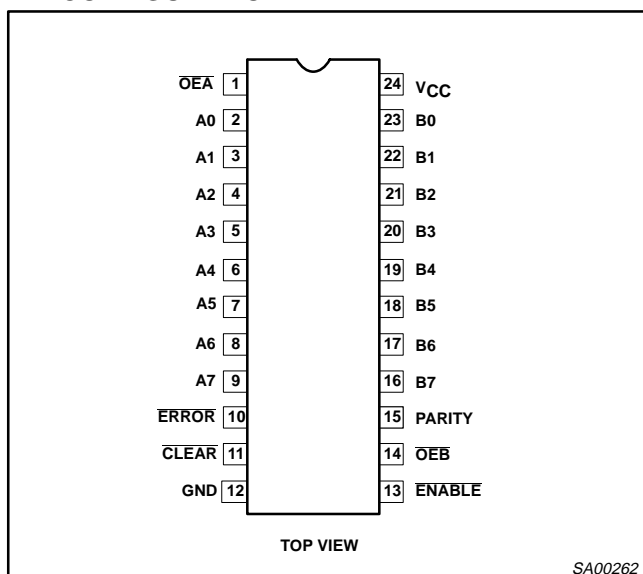
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
		$T_{\text{amb}} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$		
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF}; V_{\text{CC}} = 5\text{V}$	3.4	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay An to PARITY	$C_L = 50\text{pF}; V_{\text{CC}} = 5\text{V}$	7.4	ns
$C_{\text{IN}}$	Input capacitance	$V_I = 0\text{V}$ or $V_{\text{CC}}$	4	pF
$C_{\text{I/O}}$	I/O capacitance	Outputs disabled; $V_O = 0\text{V}$ or $V_{\text{CC}}$	7	pF
$I_{\text{CCZ}}$	Total supply current	Outputs disabled; $V_{\text{CC}} = 5.5\text{V}$	50	$\mu\text{A}$

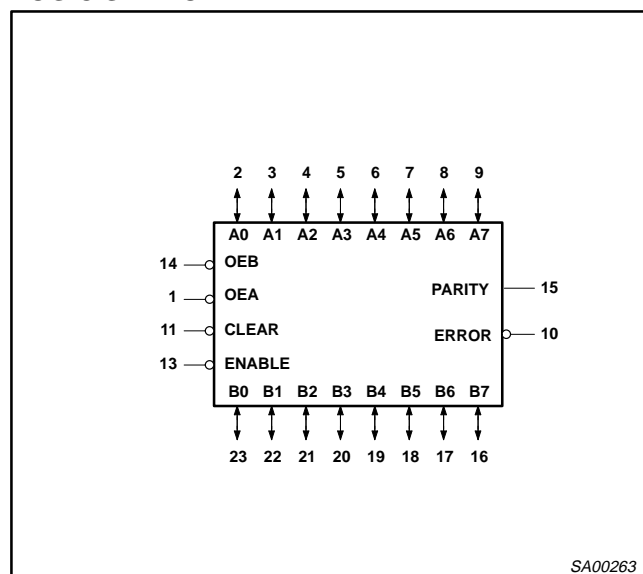
### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	-40°C to +85°C	74ABT853 N	74ABT853 N	SOT222-1
24-Pin plastic SO	-40°C to +85°C	74ABT853 D	74ABT853 D	SOT137-1
24-Pin Plastic SSOP Type II	-40°C to +85°C	74ABT853 DB	74ABT853 DB	SOT340-1
24-Pin Plastic TSSOP Type I	-40°C to +85°C	74ABT853 PW	74ABT853PW DH	SOT355-1

### PIN CONFIGURATION



### LOGIC SYMBOL



# 8-bit transceiver with 9-bit parity checker/ generator and flag latch (3-State)

74ABT853

## PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 – A7	2, 3, 4, 5, 6, 7, 8, 9	A port 3-State inputs/outputs
B0 – B7	23, 22, 21, 20, 19, 18, 17, 16	B port 3-State inputs/outputs
$\overline{\text{OEA}}$	1	Enables the A outputs when Low
$\overline{\text{OEB}}$	14	Enables the B outputs when Low
PARITY	15	Parity output/input
ERROR	10	Error output (open collector)
$\overline{\text{CLEAR}}$	11	Clears the error flag register when Low
$\overline{\text{ENABLE}}$	13	Enable input (active-Low)
GND	12	Ground (0V)
V <sub>CC</sub>	24	Positive supply voltage

## FUNCTION TABLE

MODE	INPUTS				OUTPUTS		
	$\overline{\text{OEB}}$	$\overline{\text{OEA}}$	A <sub>n</sub> Σ OF HIGHS	B <sub>n</sub> + PARITY Σ OF HIGHS	A <sub>n</sub>	B <sub>n</sub>	PARITY
A data to B bus and generate odd parity output	L	H	Odd Even	(output)	(input)	A <sub>n</sub>	L H
B data to A bus and check for parity error <sup>1</sup>	H	L	(output)	X	B <sub>n</sub>	(input)	(input)
A bus and B bus disabled <sup>2</sup>	H	H	X	X	Z	Z	Z
A data to B bus and generate inverted parity output	L	L	Odd Even	(output)	(input)	A <sub>n</sub>	H L

### NOTES:

- Error checking is detailed in the Error Flag Function Table below.
- When  $\overline{\text{ENABLE}}$  is Low, ERROR is Low if the sum of A inputs is even or ERROR is High if the sum of A inputs is odd.

## ERROR FLAG FUNCTION TABLE

MODE	INPUTS			INTERNAL NODE POINT "P"	OUTPUT PRE-STATE ERROR <sub>n-1</sub>	ERROR OUTPUT
	$\overline{\text{ENABLE}}$	$\overline{\text{CLEAR}}$	B <sub>n</sub> + PARITY Σ OF HIGHS			
Pass	L	L	Odd Even	H L	X	H L
Sample	L	H	Odd Even X	H L X	H X L	H L L
Clear	H	L	X	X	X	H
Store	H	H	X	X	L H	L H

- H = High voltage level steady state  
 L = Low voltage level steady state  
 X = Don't care  
 Z = High impedance "off" state



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74ABT853

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Low-level input voltage		0.8	V
$I_{OH}$	High-level output current		-32	mA
$I_{OL}$	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_{amb} = +25^\circ\text{C}$			$T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$		
			Min	Typ	Max	Min	Max	
$V_{IK}$	Input clamp voltage	$V_{CC} = 4.5\text{V}; I_{IK} = -18\text{mA}$		-0.9	-1.2		-1.2	V
$V_{OH}$	High-level output voltage All outputs except ERROR	$V_{CC} = 4.5\text{V}; I_{OH} = -3\text{mA}; V_I = V_{IL}$ or $V_{IH}$	2.5	3.5		2.5		V
		$V_{CC} = 5.0\text{V}; I_{OH} = -3\text{mA}; V_I = V_{IL}$ or $V_{IH}$	3.0	4.0		3.0		V
		$V_{CC} = 4.5\text{V}; I_{OH} = -32\text{mA}; V_I = V_{IL}$ or $V_{IH}$	2.0	2.6		2.0		V
$V_{OL}$	Low-level output voltage	$V_{CC} = 4.5\text{V}; I_{OL} = 64\text{mA}; V_I = V_{IL}$ or $V_{IH}$		0.42	0.55		0.55	V
$I_I$	Input leakage current	Control pins $V_{CC} = 5.5\text{V}; V_I = \text{GND}$ or $5.5\text{V}$		$\pm 0.01$	$\pm 1.0$		$\pm 1.0$	$\mu\text{A}$
		Data pins $V_{CC} = 5.5\text{V}; V_I = \text{GND}$ or $5.5\text{V}$		$\pm 5$	$\pm 100$		$\pm 100$	$\mu\text{A}$
$I_{OFF}$	Power-off leakage current	$V_{CC} = 0.0\text{V}; V_O$ or $V_I \leq 4.5\text{V}$		$\pm 5.0$	$\pm 100$		$\pm 100$	$\mu\text{A}$
$I_{PU/PD}$	Power-up/down 3-State output current <sup>3</sup>	$V_{CC} = 2.1\text{V}; V_O = 0.5\text{V}; V_I = \text{GND}$ or $V_{CC}$ ; $V_{OE} = \text{Don't care}$		$\pm 5.0$	$\pm 50$		$\pm 50$	$\mu\text{A}$
$I_{IH} + I_{OZH}$	3-State output High current	$V_{CC} = 5.5\text{V}; V_O = 2.7\text{V}; V_I = V_{IL}$ or $V_{IH}$		5.0	50		50	$\mu\text{A}$
$I_{IL} + I_{OZL}$	3-State output Low current	$V_{CC} = 5.5\text{V}; V_O = 0.5\text{V}; V_I = V_{IL}$ or $V_{IH}$		-5.0	-50		-50	$\mu\text{A}$
$I_{CEX}$	Output high leakage current	$V_{CC} = 5.5\text{V}; V_O = 5.5\text{V}; V_I = \text{GND}$ or $V_{CC}$		5.0	50		50	$\mu\text{A}$
$I_O$	Output current <sup>1</sup>	$V_{CC} = 5.5\text{V}; V_O = 2.5\text{V}$	-50	-100	-180	-50	-180	mA
$I_{CCH}$	Quiescent supply current	$V_{CC} = 5.5\text{V}; \text{Outputs High}, V_I = \text{GND}$ or $V_{CC}$		0.5	250		250	$\mu\text{A}$
$I_{CCL}$		$V_{CC} = 5.5\text{V}; \text{Outputs Low}, V_I = \text{GND}$ or $V_{CC}$		25	38		38	mA
$I_{CCZ}$		$V_{CC} = 5.5\text{V}; \text{Outputs 3-State}; V_I = \text{GND}$ or $V_{CC}$		0.5	50		50	$\mu\text{A}$
$\Delta I_{CC}$	Additional supply current per input pin <sup>2</sup>	Outputs enabled, one input at 3.4V, other inputs at $V_{CC}$ or GND; $V_{CC} = 5.5\text{V}$		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at $V_{CC}$ or GND; $V_{CC} = 5.5\text{V}$		0.01	50		50	$\mu\text{A}$
		Outputs 3-State, one enable input at 3.4V, other inputs at $V_{CC}$ or GND; $V_{CC} = 5.5\text{V}$		0.5	1.5		1.5	mA

## NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This parameter is valid for any  $V_{CC}$  between 0V and 2.1V, with a transition time of up to 10msec. From  $V_{CC} = 2.1\text{V}$  to  $V_{CC} = 5\text{V} \pm 10\%$ , a transition time of up to 100 $\mu\text{sec}$  is permitted. The ERROR output pin 10 is not included in this spec due to the open collector design.

# 8-bit transceiver with 9-bit parity checker/ generator and flag latch (3-State)

74ABT853

## AC CHARACTERISTICS

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ 

SYMBOL	PARAMETER	WAVEFORMS	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$			$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 10\%$		
			Min	Typ	Max	Min	Max	
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay An to Bn or Bn to An	4	1.2 1.0	3.4 2.6	4.8 4.0	1.2 1.0	5.3 4.5	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay An to PARITY	1, 4	2.1 2.5	7.4 7.4	9.5 9.7	2.1 2.5	11.2 11.0	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay OEA to PARITY	1, 4	1.8 2.3	6.6 6.7	8.5 8.6	1.8 2.3	10.5 10.0	ns
$t_{\text{PLH}}$	Propagation delay CLEAR to ERROR	3	1.0	3.6	5.5	1.0	6.2	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay ENABLE to ERROR	4	1.8 1.8	3.8 4.5	5.1 5.8	1.8 1.8	6.0 6.6	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay Bn or PARITY to ERROR	1, 4	2.0 3.0	7.9 9.0	10.1 11.5	2.0 3.0	11.7 12.8	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time OEA to An or OEB to Bn, PARITY	2, 5	1.0 2.1	3.2 4.1	5.1 5.8	1.0 2.1	6.2 6.7	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time OEA to An or OEB to Bn, PARITY	2, 5	3.1 3.2	5.1 5.6	7.3 7.2	3.1 3.2	7.9 8.1	ns

## AC SETUP REQUIREMENTS

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ 

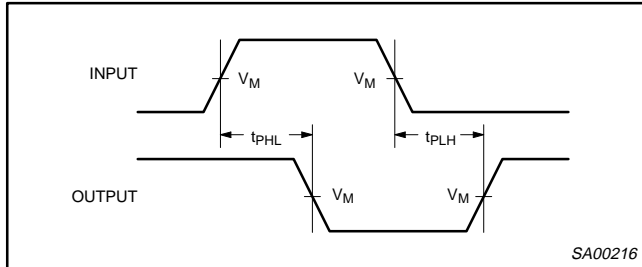
SYMBOL	PARAMETER	WAVEFORMS	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 10\%$	
			MIN	TYP	MIN	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low Bn or PARITY to ENABLE	6	8.5 8.5	6.5 3.6	8.5 8.5	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low Bn or PARITY to ENABLE	6	0.0 0.0	-3.4 -6.3	0.0 0.0	ns
$t_s(\text{H})$	Setup time, High CLEAR to ENABLE	6	2.0	-1.6	2.0	ns
$t_h(\text{L})$	Hold time, Low CLEAR to ENABLE	6	3.0	1.8	3.0	ns
$t_w(\text{L})$	Pulse width, Low CLEAR	3	3.5	1.0	3.5	ns
$t_w(\text{L})$	Pulse width, Low ENABLE	6	4.0	2.5	4.0	ns

# 8-bit transceiver with 9-bit parity checker/ generator and flag latch (3-State)

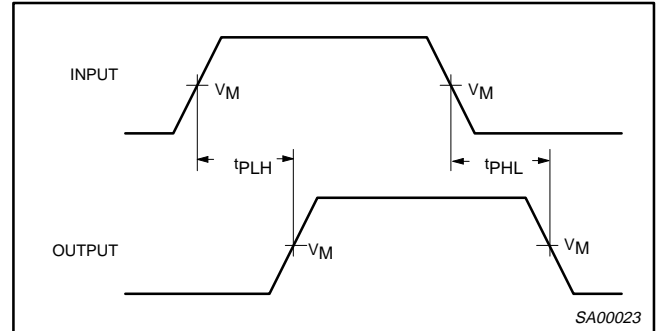
74ABT853

## AC WAVEFORMS

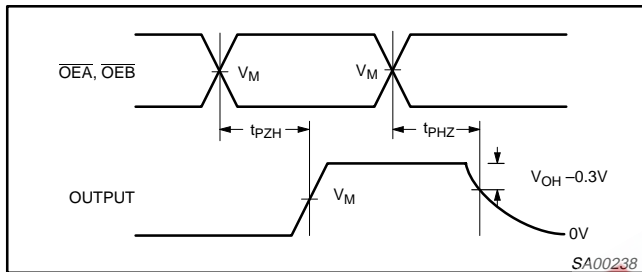
$V_M = 1.5V, V_{IN} = GND \text{ to } 3.0V$



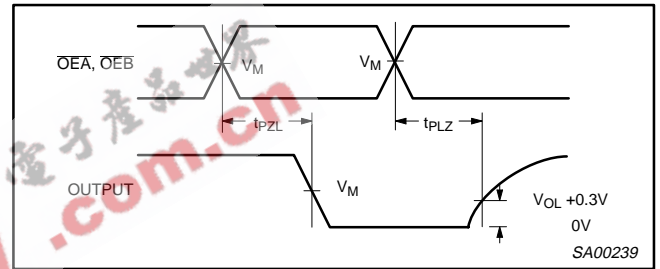
Waveform 1. Propagation Delay For Inverting Output



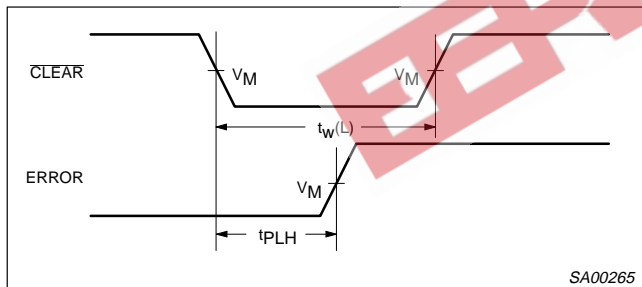
Waveform 4. Propagation Delay For Non-Inverting Output



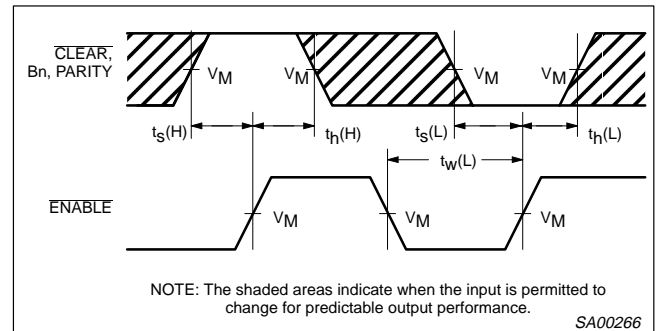
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 3. CLEAR Pulse Width and CLEAR to ERROR Delay

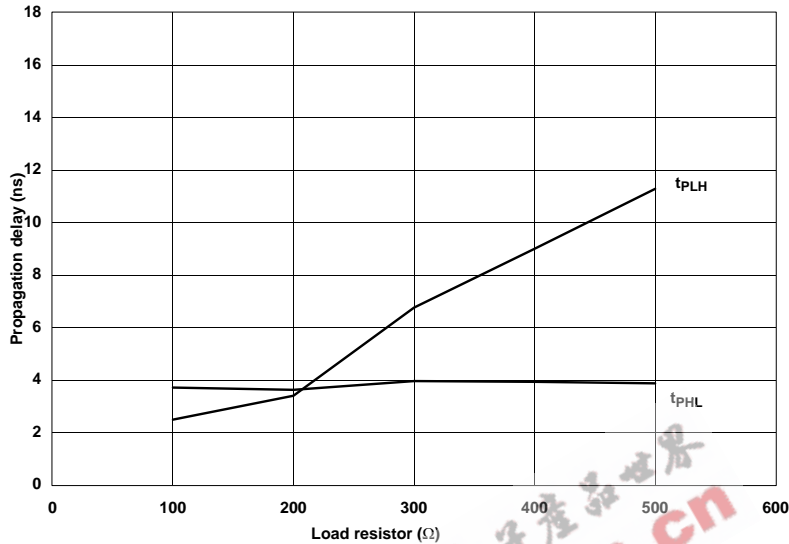


Waveform 6. Data Setup and Hold Times and ENABLE Pulse Width

# 8-bit transceiver with 9-bit parity checker/ generator and flag latch (3-State)

74ABT853

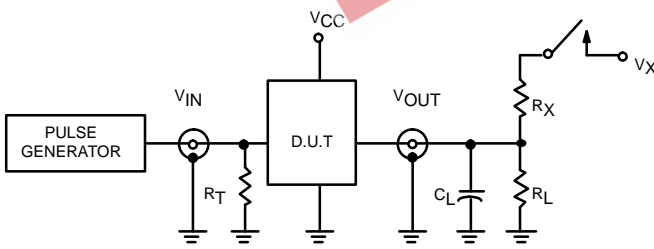
## TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



**NOTE:** When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t<sub>PLH</sub>. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t<sub>PLH</sub> over 300% with only a slight change in the t<sub>PHL</sub>. However, if the value of the pull-up resistor is changed, the user must make certain that the total I<sub>OL</sub> current through the resistor and the total I<sub>L</sub>'s of the receivers does not exceed the I<sub>OL</sub> maximum specification.

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## TEST CIRCUIT AND WAVEFORM



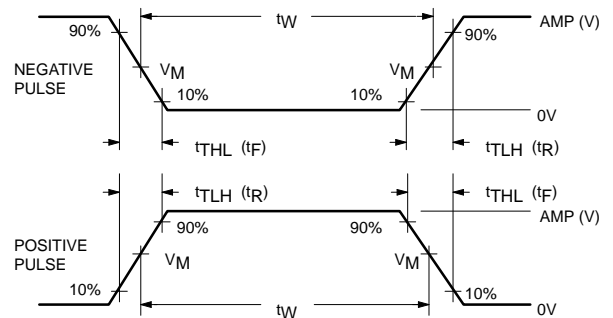
Test Circuit for 3-State Outputs

### SWITCH POSITION

TEST	SWITCH
t <sub>PLZ</sub>	closed
t <sub>PZL</sub>	closed
All other	open

### LOAD VALUES

OUTPUT	R <sub>X</sub>	V <sub>X</sub>
ERROR	100Ω	V <sub>CC</sub>
All other	500Ω	7.0V



V<sub>M</sub> = 1.5V  
Input Pulse Definition

### DEFINITIONS

R<sub>L</sub> = Load resistor; see AC CHARACTERISTICS for value.

C<sub>L</sub> = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R<sub>T</sub> = Termination resistance should be equal to Z<sub>OUT</sub> of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t <sub>w</sub>	t <sub>R</sub>	t <sub>F</sub>
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

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