DATA SHEET

74LVCH32373A

32-bit transparent D-type latch with 5 V tolerant inputs/outputs; 3-state

Product specification
File under Integrated Circuits, IC24

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Philips Semiconductors

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32-bit transparent D-type latch with 5 V tolerant inputs/outputs; 3-state

74LVCH32373A

FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- MULTIBYTE™ flow-trough standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on data inputs
- Typical output ground bounce voltage: V_{OLP} < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical output undershoot voltage: V_{OHV} > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Power off disables outputs, permitting live insertion
- Packaged in plastic fine-pitch ball grid array package.

DESCRIPTION

The 74LVCH32373A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 or 5 V environment.

The 74LVCH32373A is a 32-bit transparent D-type latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. One latch enable (nLE) input and one output enable ($n\overline{OE}$) are provided for each octal. Inputs can be driven from either 3.3 or 5 V devices.

The 74LVCH32373A consists of 4 sections of eight D-type transparent latches with 3-state true outputs. When input nLE is HIGH, data at the nD_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes.

When input nLE is LOW the latches store the information that was present at the D-inputs one set-up time preceding the HIGH-to-LOW transition of nLE. When input $n\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When input $n\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $n\overline{OE}$ input does not affect the state of the latches.

The 74LVCH32373A bus hold data input circuits eliminate the need for external pull-up resistors to hold unused inputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay			
	nD_n to nQ_n	C_L = 50 pF; V_{CC} = 3.3 V	3.0	ns
	nLE to nQ_n	C_L = 50 pF; V_{CC} = 3.3 V	3.4	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	V_I = GND to V_{CC}; note 1	26	pF

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   C_L = output load capacitance in pF;

   V_{CC} = supply voltage in Volts;

   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

FUNCTION TABLE

See note 1.

OPERATING MODE	INPUTS			INTERNAL LATCHES	OUTPUTS
	$n\overline{OE}$	nLE	nD_n		nQ_n
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

Note

1. H = HIGH voltage level;
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
   L = LOW voltage level;
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVCH32373AEC	−40 to +85 °C	96	LFBGA96	plastic	SOT536-1

PINNING

SYMBOL	DESCRIPTION
nD_n	data inputs
nLE	latch enable inputs (active HIGH)
nQ_n	data outputs
GND	ground (0 V)
$n\overline{OE}$	output enable inputs (active LOW)
V_{CC}	DC supply voltage

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	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
6	$1D_1$	$1D_3$	$1D_5$	$1D_7$	$2D_1$	$2D_3$	$2D_5$	$2D_7$	$3D_1$	$3D_3$	$3D_5$	$3D_7$	$4D_1$	$4D_3$	$4D_5$	$4D_6$
5	$1D_0$	$1D_2$	$1D_4$	$1D_6$	$2D_0$	$2D_2$	$2D_4$	$2D_6$	$3D_0$	$3D_2$	$3D_4$	$3D_6$	$4D_0$	$4D_2$	$4D_4$	$4D_7$
4	1LE	GND	V_{CC}	GND	GND	V_{CC}	GND	2LE	3LE	GND	V_{CC}	GND	GND	V_{CC}	GND	4LE
3	$1\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$2\overline{OE}$	$3\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$4\overline{OE}$
2	$1Q_0$	$1Q_2$	$1Q_4$	$1Q_6$	$2Q_0$	$2Q_2$	$2Q_4$	$2Q_6$	$3Q_0$	$3Q_2$	$3Q_4$	$3Q_6$	$4Q_0$	$4Q_2$	$4Q_4$	$4Q_7$
1	$1Q_1$	$1Q_3$	$1Q_5$	$1Q_7$	$2Q_1$	$2Q_3$	$2Q_5$	$2Q_7$	$3Q_1$	$3Q_3$	$3Q_5$	$3Q_7$	$4Q_1$	$4Q_3$	$4Q_5$	$4Q_6$

Fig.1 Pin configuration.

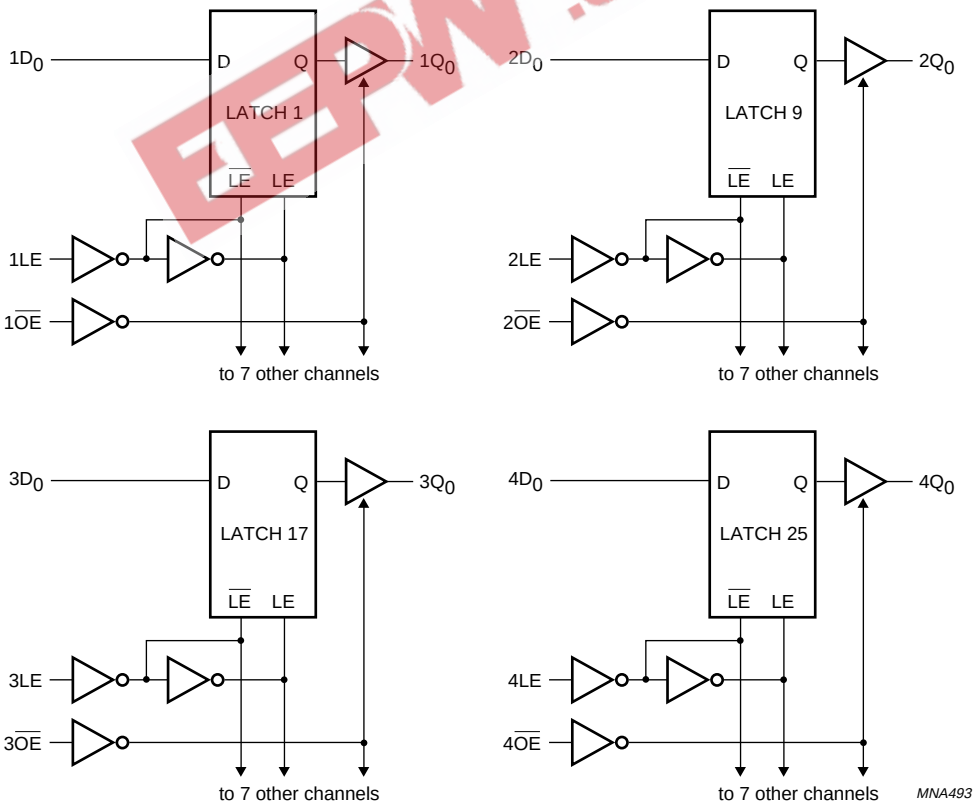


Fig.2 Logic symbol.

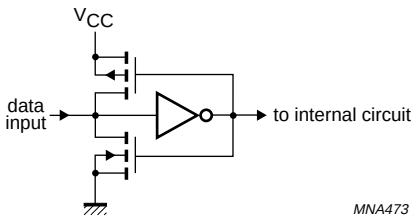


Fig.3 Bus hold circuit.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CC}	DC supply voltage	maximum speed performance	2.7	3.6	V
		low-voltage applications	1.2	3.6	V
V_I	DC input voltage		0	5.5	V
V_O	DC output voltage	HIGH or LOW state	0	V_{CC}	V
		3-state	0	5.5	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+85	°C
t_r, t_f ($\Delta t/\Delta f$)	input rise and fall times	V_{CC} = 1.2 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 3.6 V	0	10	

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		–0.5	+6.5	V
V_I	DC input voltage	note 1	–0.5	+6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–	–50	mA
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$; note 1	–	±50	mA
V_O	DC output voltage	HIGH or LOW state; note 1	–0.5	V_{CC} + 0.5	V
		3-state; note 1	–0.5	+6.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	temperature range –40 to +85 °C; note 2	–	1000	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 70 °C the value of P_D derates linearly with 1.8 mW/K.

DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} −40 to +85°C			UNIT
		OTHER	V_{CC}(V)	MIN.	TYP.(1)	MAX.	
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –12 mA	2.7	V_{CC} – 0.5	–	–	V
		I_O = –100 µA	3.0	V_{CC} – 0.2	V_{CC}	–	
		I_O = –18 mA	3.0	V_{CC} – 0.6	–	–	
		I_O = –24 mA	3.0	V_{CC} – 0.8	–	–	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 12 mA	2.7	–	–	0.40	V
		I_O = 100 µA	3.0	–	–	0.20	
		I_O = 24 mA	3.0	–	–	0.55	
I_I	input leakage current	V_I = 5.5 V or GND; note 2	3.6	–	±0.1	±5	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; V_O = 5.5 V or GND	3.6	–	0.1	±5	µA
I_{off}	power off leakage supply current	V_I or V_O = 5.5 V	0.0	–	0.1	±10	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	3.6	–	0.1	40	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0	2.7 to 3.6	–	5	500	µA
I_{BHL}	bus hold LOW sustaining current	V_I = 0.8 V; notes 3, 4 and 5	3.0	75	–	–	µA
I_{BHH}	bus hold HIGH sustaining current	V_I = 2.0 V; notes 3, 4 and 5	3.0	–75	–	–	µA
I_{BHLO}	bus hold LOW overdrive current	notes 3, 4 and 6	3.6	500	–	–	µA
I_{BHHO}	bus hold HIGH overdrive current	notes 3, 4 and 6	3.6	–500	–	–	µA

Notes

1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. For bus hold parts the bus hold circuit is switched off when V_I exceeds V_{CC} allowing 5.5 V on the input terminal.
3. Valid for data inputs of bus hold parts (LVCH32-A) only.
4. For data inputs only; control inputs do not have a bus hold circuit.
5. The specified sustaining current at the data input holds the input below the specified V_I level.
6. The specified overdrive current at the data input forces the data input to the opposite logic input level.

AC CHARACTERISTICS

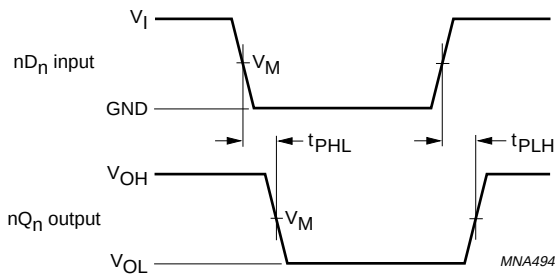
GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} = −40 to +85 °C			UNIT
		WAVEFORMS	V_{CC} (V)	MIN.	TYP.(1)	MAX.	
t_{PHL}/t_{PLH}	propagation delay nD_n to nQ_n	see Figs 4 and 8	2.7	1.5	–	5.7	ns
			3.0 to 3.6	1.5	3.0	4.7	
	propagation delay nLE to nQ_n	see Figs 5 and 8	2.7	1.5	–	5.8	ns
			3.0 to 3.6	1.5	3.4	4.8	
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nQ_n	see Figs 7 and 8	2.7	1.5	–	6.5	ns
			3.0 to 3.6	1.5	3.5	5.5	
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nQ_n	see Figs 7 and 8	2.7	1.5	–	6.4	ns
			3.0 to 3.6	1.5	3.9	5.4	
t_W	nLE pulse width HIGH	see Figs 5 and 8	2.7	3.0	–	–	ns
			3.0 to 3.6	3.0	2.0	–	
t_{su}	set-up time nD_n to nLE	see Figs 6 and 8	2.7	1.7	–	–	ns
			3.0 to 3.6	+1.7	−0.1	–	
t_h	hold time nD_n to nLE	see Figs 6 and 8	2.7	1.2	–	–	ns
			3.0 to 3.6	1.2	0.1	–	

Note

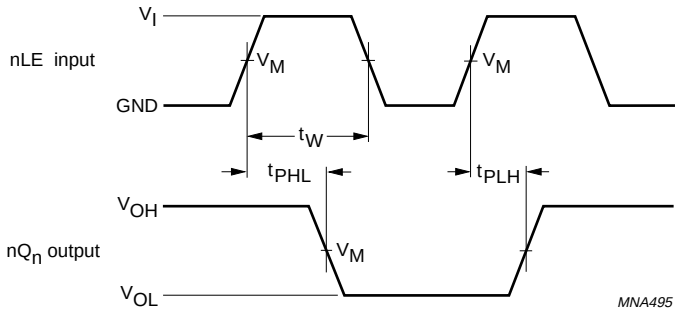
1. All typical values are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.

AC WAVEFORMS



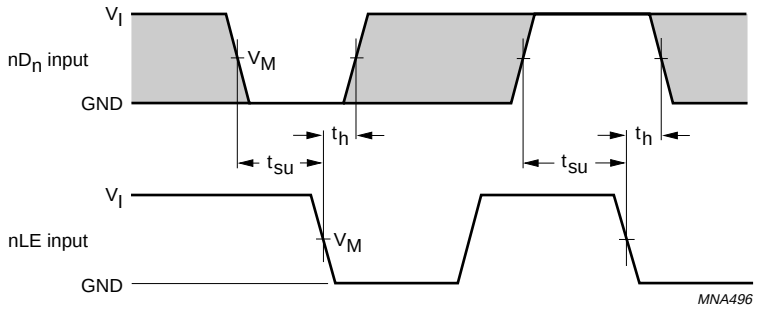
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V;
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.4 Input (nD_n) to output (nQ_n) propagation delay times.



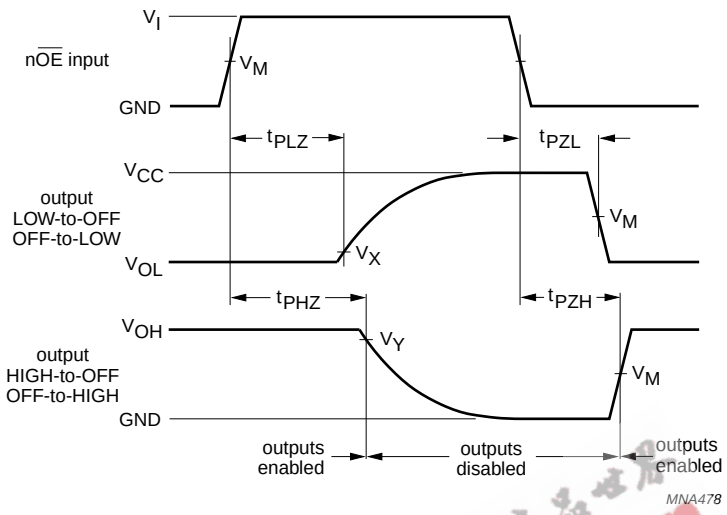
V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V;
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.5 Latch enable inputs (nLE) pulse width and the latch enable input to outputs (nQ_n) propagation delay times.



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V.

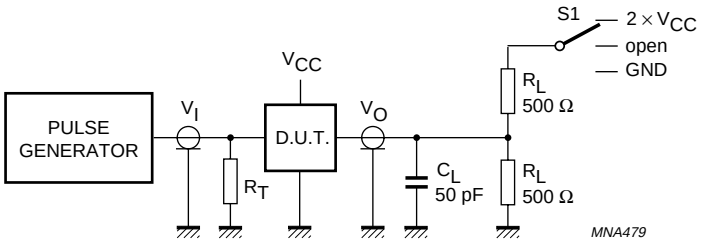
Fig.6 Set-up and hold times for inputs (nD_n) to inputs (nLE).



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V;
$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V;
$V_X = V_{OL}$ + 0.1 V at V_{CC} < 2.7 V;

$V_Y = V_{OH}$ – 0.3 V at $V_{CC} \geq$ 2.7 V;
$V_Y = V_{OH}$ – 0.1 V at V_{CC} < 2.7 V;
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 3-state output enable and disable times.



TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

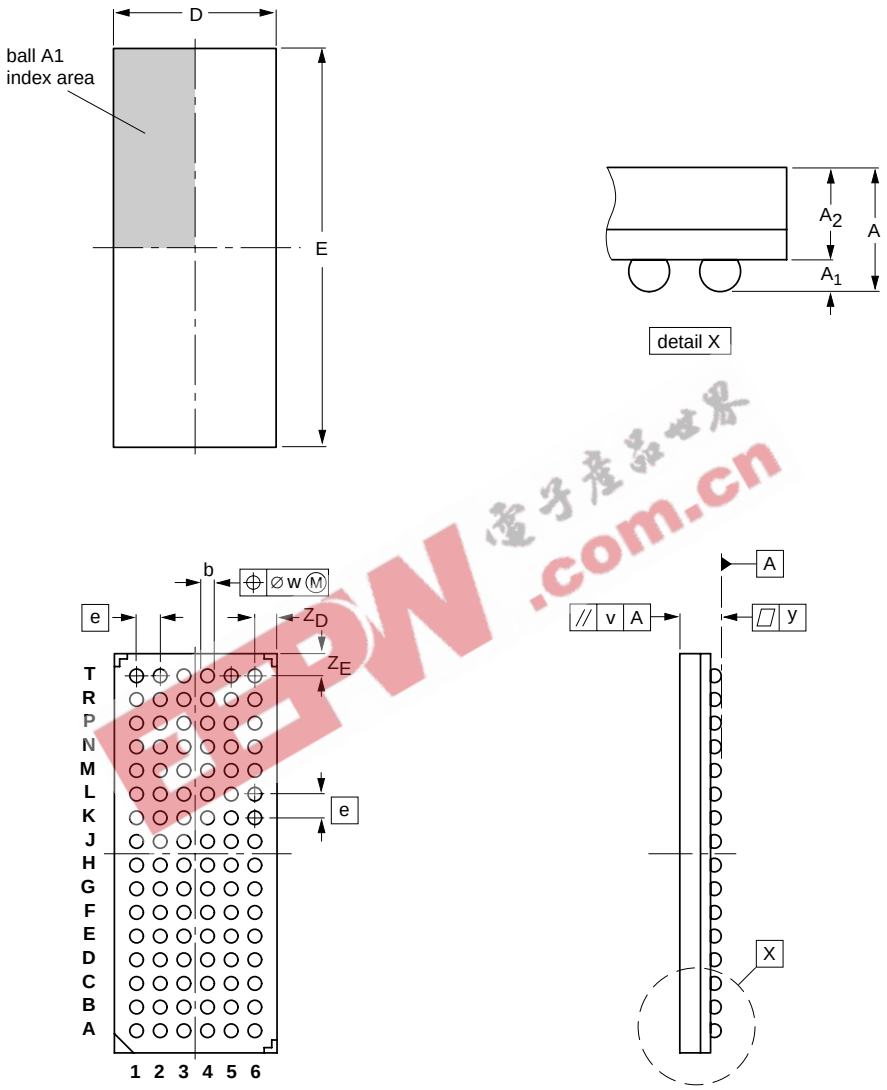
V_{CC}	V_I
<2.7 V	V_{CC}
2.7 to 3.6 V	2.7 V

Definitions for test circuit:
R_L = load resistor.
C_L = load capacitance including jig and probe capacitance.
R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

PACKAGE OUTLINE

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	v	w	y	Z_D	Z_E
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	0.2	0.15	0.1	0.93 0.58	0.93 0.58

0 5 10 mm
scale

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT536-1						~~98-11-25~~ 99-06-03

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

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