FAIRCHILD SEMICONDUCTOR™

November 2001
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# 74ALVC163245
# Low Voltage 16-Bit Dual Supply Translating Transceiver with 3-STATE Outputs

## General Description

The ALVC163245 is a dual supply, 16-bit translating transceiver that is designed for 2 way asynchronous communication between busses at different supply voltages by providing true signal translation. The supply rails consist of $V_{CCA}$, which is a higher potential rail operating at 2.3V to 3.6V and $V_{CCB}$, which is the lower potential rail operating at 1.65V to 2.7V. ($V_{CCB}$ must be less than or equal to $V_{CCA}$ for proper device operation). This dual supply design allows for translation from 1.8V to 2.5V busses to busses at a higher potential, up to 3.3V.

The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable ($\overline{OE}$) input, when HIGH, disables both A and B Ports by placing them in a High-Z condition. The A Port interfaces with the higher voltage bus (2.7V to 3.3V); The B Port interfaces with the lower voltage bus (1.8V to 2.5V). Also the ALVC163245 is designed so that the control pins ($T/\overline{R}_n$, $\overline{OE}_n$) are supplied by $V_{CCB}$.

The 74ALVC163245 is suitable for mixed voltage applications such as notebook computers using a 1.8V CPU and 3.3V peripheral components. It is fabricated with an Advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

## Features

- Bidirectional interface between busses ranging from 1.65V to 3.6V
- Supports Live Insertion and Withdrawal (Note 1)
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16245
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human Body Model >2000V
  - Machine model >200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

**Note 1:** To ensure the high impedance state during power up or power down, $OE_n$ should be tied to $V_{CCB}$ through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver.

## Ordering Code:

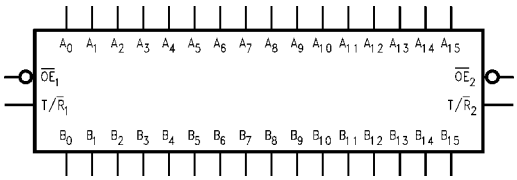
| Order Number | Package Number | Package Description |
|---|---|---|
| 74ALVC163245GX (Note 2) | BGA54A (Preliminary) | 54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [Tape and Reel] |
| 74ALVC163245T (Note 3) | MTD48 | 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

**Note 2:** BGA package available in Tape and Reel only.

**Note 3:** Device also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

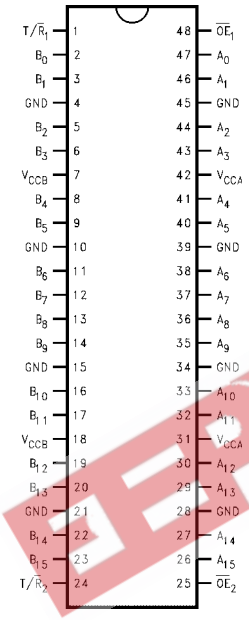
Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

## Logic Diagram

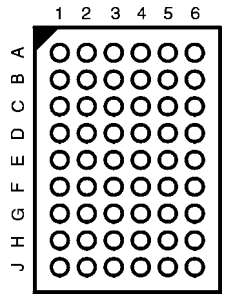



## Connection Diagrams

**Pin Assignment for TSSOP**




**Pin Assignment for FBGA**




**(Top Thru View)**

## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OE}_n$ | Output Enable Input (Active LOW) |
| $T/\overline{R}_n$ | Transmit/Receive Input |
| $A_0$–$A_{15}$ | Side A Inputs or 3-STATE Outputs |
| $B_0$–$B_{15}$ | Side B Inputs or 3-STATE Outputs |
| NC | No Connect |

## FBGA Pin Assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | $B_0$ | NC | $T/\overline{R}_1$ | $\overline{OE}_1$ | NC | $A_0$ |
| **B** | $B_2$ | $B_1$ | NC | NC | $A_1$ | $A_2$ |
| **C** | $B_4$ | $B_3$ | $V_{CCB}$ | $V_{CCA}$ | $A_3$ | $A_4$ |
| **D** | $B_6$ | $B_5$ | GND | GND | $A_5$ | $A_6$ |
| **E** | $B_8$ | $B_7$ | GND | GND | $A_7$ | $A_8$ |
| **F** | $B_{10}$ | $B_9$ | GND | GND | $A_9$ | $A_{10}$ |
| **G** | $B_{12}$ | $B_{11}$ | $V_{CCB}$ | $V_{CCA}$ | $A_{11}$ | $A_{12}$ |
| **H** | $B_{14}$ | $B_{13}$ | NC | NC | $A_{13}$ | $A_{14}$ |
| **J** | $B_{15}$ | NC | $T/\overline{R}_2$ | $\overline{OE}_2$ | NC | $A_{15}$ |

## Truth Tables

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_1$ | $T/\overline{R}_1$ | |
| L | L | Bus $B_0$–$B_7$ Data to Bus $A_0$–$A_7$ |
| L | H | Bus $A_0$–$A_7$ Data to Bus $B_0$–$B_7$ |
| H | X | HIGH Z State on $A_0$–$A_7$, $B_0$–$B_7$ |

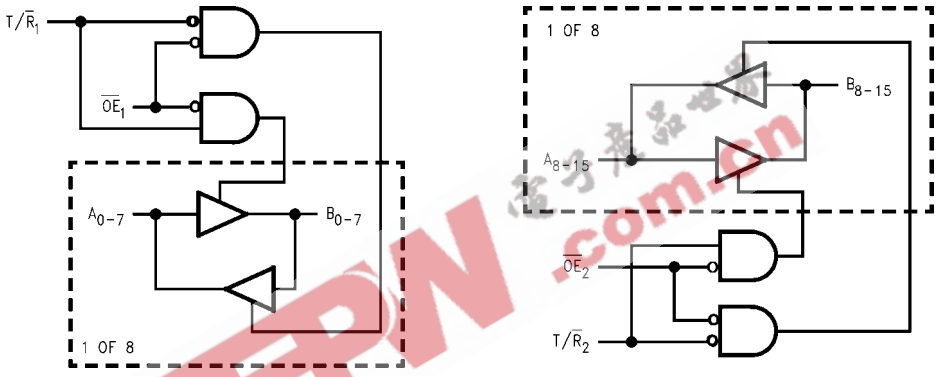
| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_2$ | $T/\overline{R}_2$ | |
| L | L | Bus $B_8$–$B_{15}$ Data to Bus $A_8$–$A_{15}$ |
| L | H | Bus $A_8$–$A_{15}$ Data to Bus $B_8$–$B_{15}$ |
| H | X | HIGH-Z State on $A_8$–$A_{15}$, $B_8$–$B_{15}$ |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

## 74ALVC163245 Translator Power Up Sequence Recommendations

To guard against power up problems, some simple guidelines need to be adhered to. The 74ALVC163245 is designed so that the control pins ($T/\overline{R}_n$, $\overline{OE}_n$) are supplied by $V_{CCB}$. Therefore the first recommendation is to begin by powering up the control side of the device, $V_{CCB}$. The $\overline{OE}_n$ control pins should be ramped with or ahead of $V_{CCB}$, this will guard against bus contentions and oscillations as all A Port and B Port outputs will be disabled. To ensure the high impedance state during power up or power down, $\overline{OE}_n$ should be tied to $V_{CCB}$ through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver. Second, the $T/\overline{R}_n$ control pins should be placed at logic LOW (0V) level, this will ensure that the B-side bus pins are configured as inputs to help guard against bus contention and oscillations. B-side Data Inputs should be driven to a valid logic level (0V or $V_{CCB}$), this will prevent excessive current draw and oscillations. $V_{CCA}$ can then be powered up after $V_{CCB}$, however $V_{CCA}$ must be greater than or equal to $V_{CCB}$ to ensure proper device operation. Upon completion of these steps the device can then be configured for the users desired operation. Following these steps will help to prevent possible damage to the translator device as well as other system components.

## Logic Diagrams




Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 4)

| | |
|---|---|
| Supply Voltage | |
| $V_{CCA}$ | –0.5V to +4.6V |
| $V_{CCB}$ | –0.5V to $V_{CCA}$ |
| DC Input Voltage ($V_I$) | –0.5V to +4.6V |
| DC Output Voltage ($V_{I/O}$) (Note 5) | |
| $A_n$ | –0.5V to $V_{CCA}$ + 0.5V |
| $B_n$ | –0.5V to $V_{CCB}$ + 0.5V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ < 0V | –50 mA |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ < 0V | –50 mA |
| DC Output Source/Sink Current | |
| ($I_{OH}/I_{OL}$) | ±50 mA |
| DC $V_{CC}$ or Ground Current | ±100 mA |
| Supply Pin ($I_{CC}$ or Ground) | |
| Storage Temperature ($T_{STG}$) | –65°C to +150°C |

## Recommended Operating Conditions (Note 6)

| | |
|---|---|
| Power Supply (Note 7) | |
| $V_{CCA}$ | 2.3V to 3.6V |
| $V_{CCB}$ | 1.65V to 2.7V |
| Input Voltage ($V_I$) @ $\overline{OE}$, T/$\overline{R}$ | 0V to $V_{CCB}$ |
| Input/Output Voltage ($V_{I/O}$) | |
| $A_n$ | 0V to $V_{CCA}$ |
| $B_n$ | 0V to $V_{CCB}$ |
| Free Air Operating Temperature ($T_A$ | –40°C to +85°C |
| Minimum Input Edge Rate (Δt/ΔV) | |
| $V_{IN}$ = 0.8V to 2.0V, $V_{CC}$ = 3.0V | 10 ns/V |

**Note 4:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 5:** $I_O$ Absolute Maximum Rating must be observed.

**Note 6:** Unused inputs or I/O pins must be held HIGH or LOW. They may not float.

**Note 7:** Operation requires: $V_{CCB} \le V_{CCA}$

## DC Electrical Characteristics

| Symbol | Parameter | | Conditions | $V_{CCB}$ (V) | $V_{CCA}$ (V) | Min | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IHA}$ | HIGH Level Input Voltage | $A_n$ | | 1.65 - 1.95 | 2.3 - 2.7 | 1.7 | | V |
| | | | | 1.65 - 2.7 | 3.0 - 3.6 | 2.0 | | |
| $V_{IHB}$ | | $B_n$, T/$\overline{R}$, $\overline{OE}$ | | 1.65 - 1.95 | 2.3 - 3.6 | 0.65 x $V_{CCB}$ | | |
| | | | | 2.3 - 2.7 | 3.0 - 3.6 | 1.6 | | |
| $V_{ILA}$ | LOW Level Input Voltage | $A_n$ | | 1.65 - 1.95 | 2.3 - 2.7 | | 0.7 | V |
| | | | | 1.65 - 2.7 | 3.0 - 3.6 | | 0.8 | |
| $V_{ILB}$ | | $B_n$, T/$\overline{R}$, $\overline{OE}$ | | 1.65 - 1.95 | 2.3 - 3.6 | | 0.35 x $V_{CCB}$ | |
| | | | | 2.3 - 2.7 | 3.0 - 3.6 | | 0.7 | |
| $V_{OHA}$ | HIGH Level Output Voltage | | $I_{OH}$ = –100 µA | 1.65 - 2.7 | 2.3 - 3.6 | $V_{CCA}$–0.2 | | V |
| | | | $I_{OH}$ = –12 mA | 1.65 | 2.3 - 2.7 | 1.7 | | |
| | | | $I_{OH}$ = –24 mA | 1.65 - 2.3 | 3.0 - 3.6 | 2 | | |
| $V_{OHB}$ | HIGH Level Output Voltage | | $I_{OH}$ = –100 µA | 1.65 - 2.7 | 2.3 - 3.6 | $V_{CCB}$–0.2 | | V |
| | | | $I_{OH}$ = –4 mA | 1.65 - 1.95 | 2.3 - 3.0 | 1.2 | | |
| | | | $I_{OH}$ = –12 mA | 2.3 - 2.7 | 3.0 | 1.7 | | |
| $V_{OLA}$ | Low Level Output Voltage | | $I_{OL}$ = 100 µA | 1.65 - 2.7 | 2.3 - 3.6 | | 0.2 | V |
| | | | $I_{OL}$ = 12 mA | 1.65 | 2.3 - 2.7 | | 0.7 | |
| | | | $I_{OL}$ = 24 mA | 1.65 - 2.3 | 3.0 - 3.6 | | 0.55 | |
| $V_{OLB}$ | Low Level Output Voltage | | $I_{OL}$ = 100 µA | 1.65 - 2.7 | 2.3 - 3.6 | | 0.2 | V |
| | | | $I_{OL}$ = 4 mA | 1.65 - 1.95 | 2.3 - 3.0 | | 0.45 | |
| | | | $I_{OL}$ = 12 mA | 2.3 -2.7 | 3.0 | | 0.7 | |
| $I_I$ | Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$ | | 0V ≤ $V_I$ ≤ 3.6V | 1.65 - 2.7 | 2.3 - 3.6 | | ±5.0 | µA |
| $I_{OZ}$ | 3-STATE Output Leakage | | 0V ≤ $V_O$ ≤ 3.6V<br>$\overline{OE}$ = $V_{CCB}$<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | 1.65 - 2.7 | 2.3 - 3.6 | | ±10 | µA |
| $I_{OFF}$ | Power Off Leakage Current | | 0≤ ($V_I$, $V_O$) ≤ 3.6V | 0 | 0 | | 10 | µA |
| $I_{CCA}/I_{CCB}$ | Quiescent Supply Current, per supply, $V_{CCA}$ / $V_{CCB}$ | | $A_n$ = $V_{CCA}$ or GND<br>$B_n$, $\overline{OE}$, & T/$\overline{R}$ = $V_{CCB}$ or GND | 1.65 - 2.7 | 2.3 - 3.6 | | 40 | µA |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input, $B_n$, T/$\overline{R}$, $\overline{OE}$ | | $V_I$ = $V_{CCB}$ – 0.6V | 1.65 - 2.2 | 2.3 - 3.6 | | 750 | µA |
| | Increase in $I_{CC}$ per Input, $A_n$ | | $V_I$ = $V_{CCA}$ – 0.6V | 1.65 - 2.2 | 2.3 - 3.6 | | 750 | µA |

## AC Electrical Characteristics

| Symbol | Parameter | | $T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$ | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | $C_L = 50$ pF | | $C_L = 30$ pF | | |
| | | | Min | Max | Min | Max | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay A to B | $V_{CCA} = 3.3 \pm 0.3$, $V_{CCB} = 2.5 \pm 0.2$ | 1.3 | 4.9 | | | ns |
| | | $V_{CCA} = 3.3 \pm 0.3$, $V_{CCB} = 1.8 \pm 0.15$ | 2.0 | 6.7 | 1.5 | 6.2 | |
| | | $V_{CCA} = 2.7$, $V_{CCB} = 1.8 \pm 0.15$ | 2.0 | 6.3 | | | |
| | | $V_{CCA} = 2.5 \pm 0.2$, $V_{CCB} = 1.8 \pm 0.15$ | | | 1.5 | 5.8 | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay B to A | $V_{CCA} = 3.3 \pm 0.3$, $V_{CCB} = 2.5 \pm 0.2$ | 1.1 | 4.5 | | | ns |
| | | $V_{CCA} = 3.3 \pm 0.3$, $V_{CCB} = 1.8 \pm 0.15$ | 1.1 | 5.6 | 0.6 | 5.1 | |
| | | $V_{CCA} = 2.7$, $V_{CCB} = 1.8 \pm 0.15$ | 1.3 | 6.0 | | | |
| | | $V_{CCA} = 2.5 \pm 0.2$, $V_{CCB} = 1.8 \pm 0.15$ | | | 0.8 | 5.5 | |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time OE to B | $V_{CCA} = 3.3 \pm 0.3$, $V_{CCB} = 2.5 \pm 0.2$ | 1.3 | 5.1 | | | ns |
| | | $V_{CCA} = 3.3 \pm 0.3$, $V_{CCB} = 1.8 \pm 0.15$ | 2.0 | 8.7 | 1.5 | 8.2 | |
| | | $V_{CCA} = 2.7$, $V_{CCB} = 1.8 \pm 0.15$ | 2.0 | 8.8 | | | |
| | | $V_{CCA} = 2.5 \pm 0.2$, $V_{CCB} = 1.8 \pm 0.15$ | | | 1.5 | 8.3 | |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time OE to A | $V_{CCA} = 3.3 \pm 0.3$, $V_{CCB} = 2.5 \pm 0.2$ | 1.1 | 4.5 | | | ns |
| | | $V_{CCA} = 3.3 \pm 0.3$, $V_{CCB} = 1.8 \pm 0.15$ | 1.1 | 5.6 | 0.6 | 5.1 | |
| | | $V_{CCA} = 2.7$, $V_{CCB} = 1.8 \pm 0.15$ | 1.3 | 5.8 | | | |
| | | $V_{CCA} = 2.5 \pm 0.2$, $V_{CCB} = 1.8 \pm 0.15$ | | | 0.8 | 5.3 | |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time OE to B | $V_{CCA} = 3.3 \pm 0.3$, $V_{CCB} = 2.5 \pm 0.2$ | 1.3 | 4.9 | | | ns |
| | | $V_{CCA} = 3.3 \pm 0.3$, $V_{CCB} = 1.8 \pm 0.15$ | 1.3 | 5.0 | 0.8 | 4.5 | |
| | | $V_{CCA} = 2.7$, $V_{CCB} = 1.8 \pm 0.15$ | 1.3 | 5.1 | | | |
| | | $V_{CCA} = 2.5 \pm 0.2$, $V_{CCB} = 1.8 \pm 0.15$ | | | 0.8 | 4.6 | |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time OE to A | $V_{CCA} = 3.3 \pm 0.3$, $V_{CCB} = 2.5 \pm 0.2$ | 1.1 | 5.3 | | | ns |
| | | $V_{CCA} = 3.3 \pm 0.3$, $V_{CCB} = 1.8 \pm 0.15$ | 1.1 | 6.1 | 0.6 | 5.6 | |
| | | $V_{CCA} = 2.7$, $V_{CCB} = 1.8 \pm 0.18$ | 1.3 | 5.7 | | | |
| | | $V_{CCA} = 2.5 \pm 0.2$, $V_{CCB} = 1.8 \pm 0.18$ | | | 0.8 | 5.2 | |

## Capacitance

| Symbol | Parameter | | Conditions | $T_A = +25°C$ | | Units |
|---|---|---|---|---|---|---|
| | | | | $V_{CC}$ | Typical | |
| $C_{IN}$ | Input Capacitance | | $V_I = 0V$ or $V_{CC}$ | 3.3 | 5 | pF |
| $C_{OUT}$ | Output Capacitance | | $V_I = 0V$ or $V_{CC}$ | 3.3 | 6 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | Outputs Enabled | f = 10 MHz, $C_L = 50$ pF | 3.3 | 20 | pF |
| | | | | 2.5 | 20 | |

## AC Loading and Waveforms

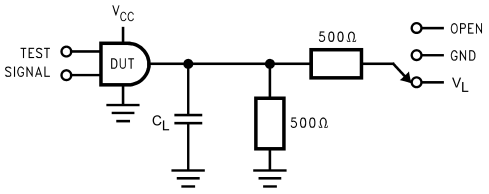



**FIGURE 1. AC Test Circuit**

**TABLE 1. Values for Figure 1**

| TEST | SWITCH |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | $V_L$ |
| $t_{PZH}$, $t_{PHZ}$ | GND |

**TABLE 2. Variable Matrix**
**(Input Characteristics: f = 1MHz; $t_r = t_f$ = 2ns; $Z_0$ = 50Ω)**

| Symbol | $V_{CC}$ | | | |
|---|---|---|---|---|
| | 3.3V ± 0.3V | 2.7V | 2.5V ± 0.2V | 1.8V ± 0.15V |
| $V_{mi}$ | 1.5V | 1.5V | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_{mo}$ | 1.5V | 1.5V | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_X$ | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.15V | $V_{OL}$ + 0.15V |
| $V_Y$ | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.15V | $V_{OH}$ − 0.15V |
| $V_L$ | 6V | 6V | $V_{CC}$*2 | $V_{CC}$*2 |

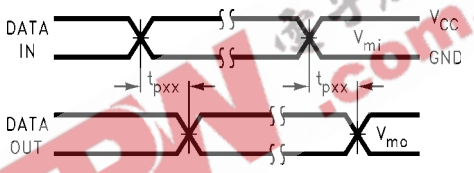



**FIGURE 2. Waveform for Inverting and Non-inverting Functions**
**$t_r = t_f \leq$ 2.0 ns, 10% to 90%**

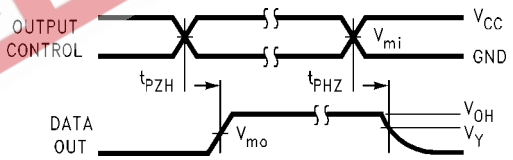



**FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**
**$t_r = t_f \leq$ 2.0 ns, 10% to 90%**

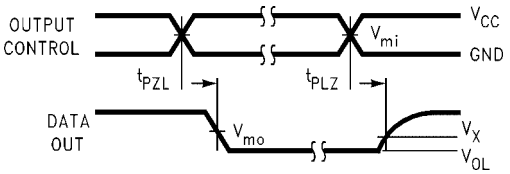
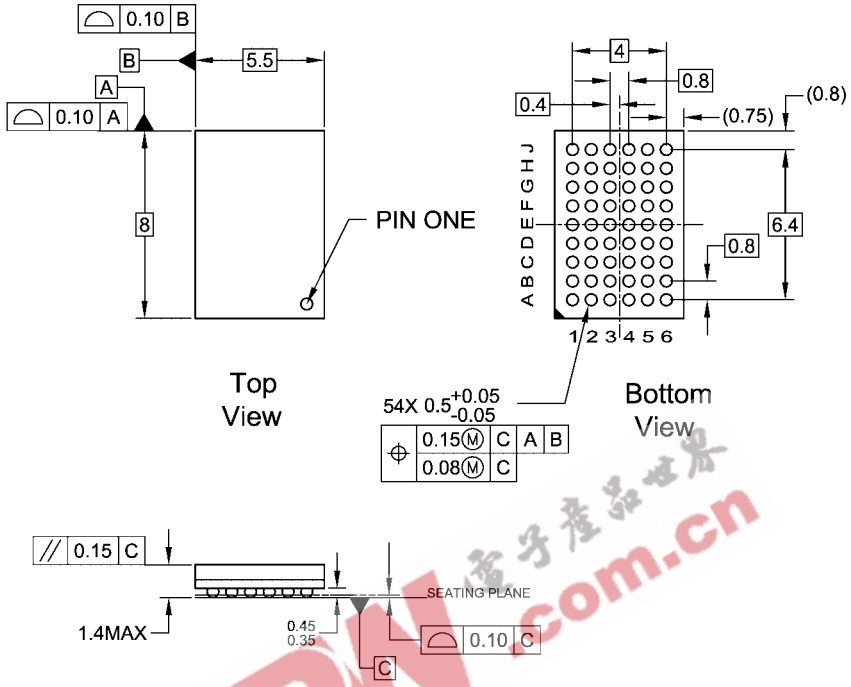



**FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic**
**$t_r = t_f \leq$ 2.0 ns, 10% to 90%**

## Physical Dimensions inches (millimeters) unless otherwise noted



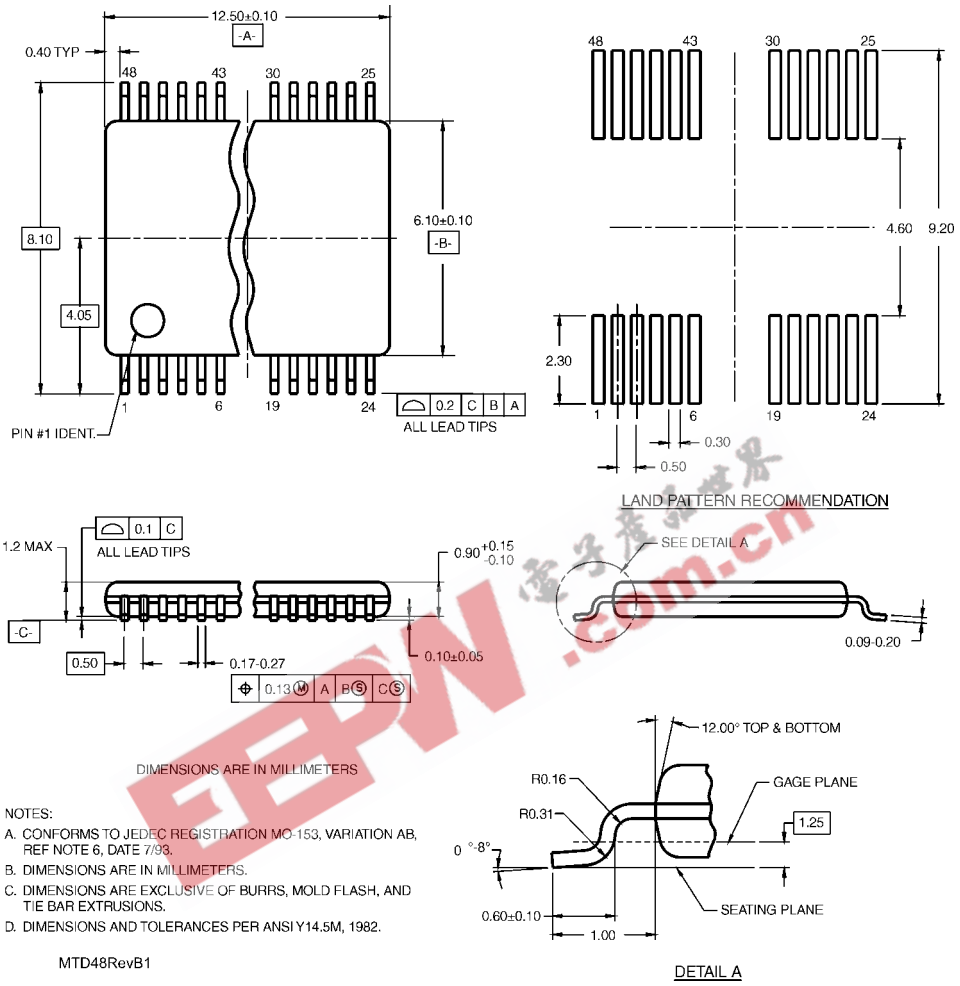

NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide**
**Package Number BGA54A**
**(Preliminary)**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**
**Package Number MTD48**



**LIFE SUPPORT POLICY**

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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