

74F657

Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and 3-STATE Outputs

General Description

The 74F657 contains eight non-inverting buffers with 3-STATE outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24 mA at the A Port and 64 mA at the B Port.

Features

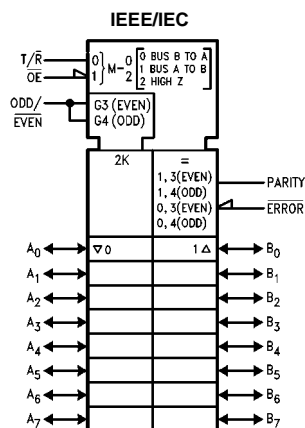
- 300 Mil 24-pin slimline DIP
- Combines 74F245 and 74F280A functions in one package
- 3-STATE outputs
- B Outputs sink 64 mA
- 12 mA source current, B side
- Input diodes for termination effects

Ordering Code:

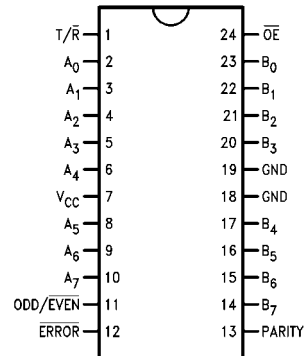
Order Number	Package Number	Package Description
75F657SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F657SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A ₀ -A ₇	Data Inputs/ 3-STATE Outputs	4.5/0.15 150/40 (33.3)	90 μ A/- 90 μ A -3 mA/24 mA (20 mA)
B ₀ -B ₇	Data Inputs/ 3-STATE Outputs	3.5/0.117 600/106.6 (80)	70 μ A/-70 μ A -12 mA/64 mA (48 mA)
$\overline{T/R}$	Transmit/Receive Input	2.0/0.067	40 μ A/-40 μ A
\overline{OE}	Enable Input	2.0/0.067	40 μ A/-40 μ A
PARITY	Parity Input/ 3-STATE Output	3.5/0.117 600/106.6 (80)	70 μ A/-70 μ A -12 mA/64 mA (48 mA)
ODD/ \overline{EVEN}	ODD/ \overline{EVEN} Parity Input	1.0/0.033	20 μ A/-20 μ A
\overline{ERROR}	Error Output	600/106.6 (80)	-12 mA/64 mA (48 mA)

Functional Description

The Transmit/Receive ($\overline{T/R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from the A Port to the B Port; Receive (active LOW) enables data from the B Port to the A Port.

The Output Enable (\overline{OE}) input disables the parity and \overline{ERROR} outputs and both the A and B Ports by placing them in a HIGH-Z condition when the Output Enable input is HIGH.

When transmitting ($\overline{T/R}$ HIGH), the parity generator detects whether an even or odd number of bits on the A Port are HIGH and compares these with the condition of the parity

select (ODD/ \overline{EVEN}). If the Parity Select is HIGH and an even number of A inputs are HIGH, the Parity output is HIGH.

In receiving mode ($\overline{T/R}$ LOW), the parity select and number of HIGH inputs on port B are compared to the condition of the Parity input. If an even number of bits on the B Port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, then \overline{ERROR} will be HIGH to indicate no error. If an odd number of bits on the B Port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, the \overline{ERROR} will be LOW indicating an error.

Function Table

Number of Inputs that are HIGH	Inputs			Input/Output	Outputs	
	\overline{OE}	$\overline{T/R}$	ODD/ \overline{EVEN}	Parity	\overline{ERROR}	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Immaterial	H	X	X	Z	Z	Z

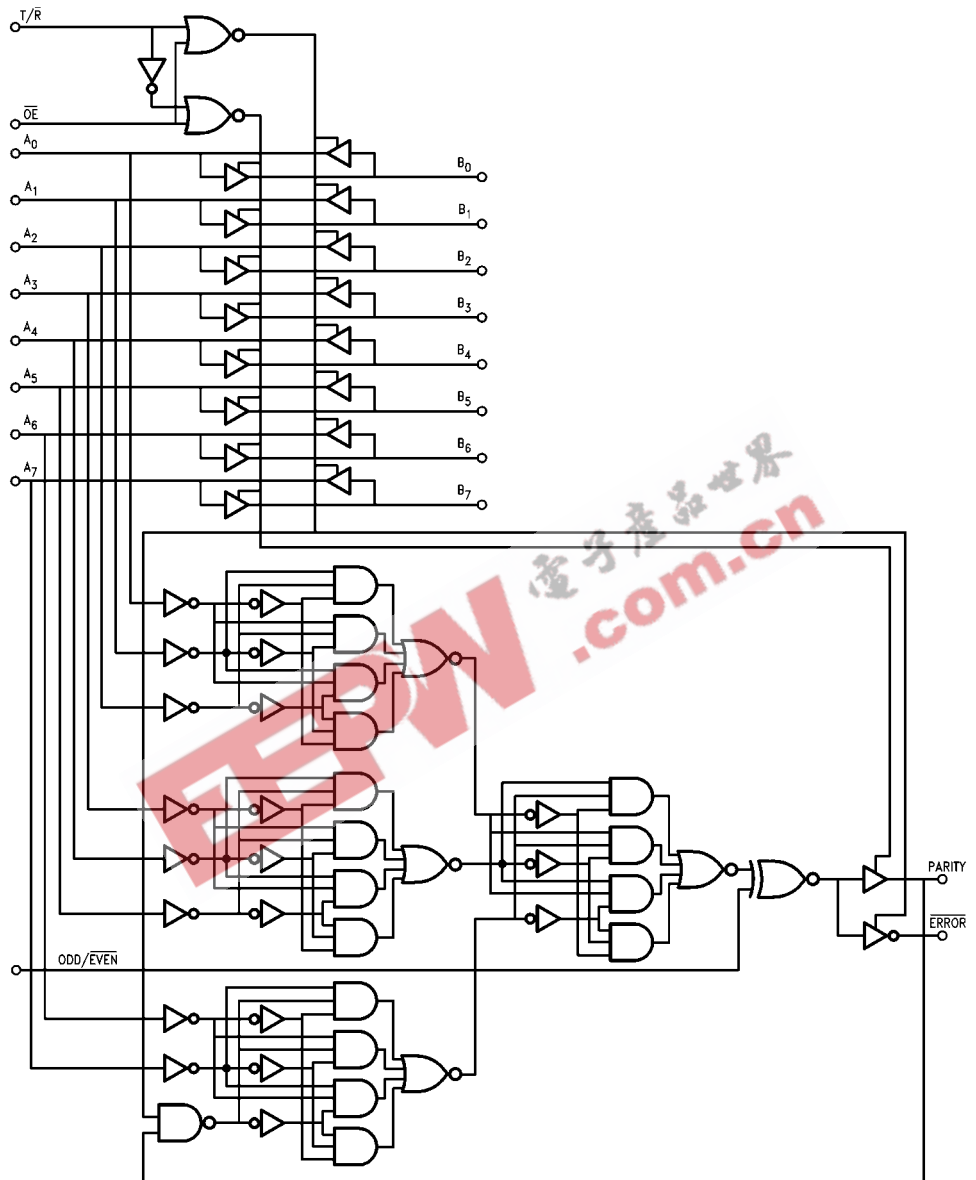
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Function Table

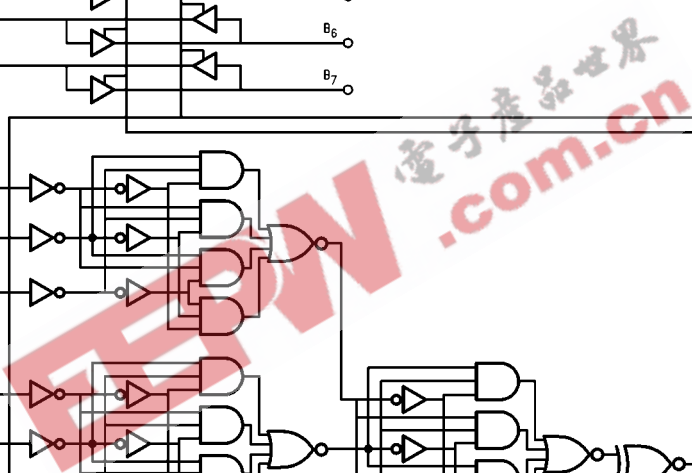
Inputs		Outputs
\overline{OE}	$\overline{T/R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Block Diagram



2 GROUND PINS
1 V_{CC} PIN



Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions	
Storage Temperature	-65°C to +150°C	Free Air Ambient Temperature	0°C to +70°C
Ambient Temperature under Bias	-55°C to +125°C	Supply Voltage	+4.5V to +5.5V
Junction Temperature under Bias	-55°C to +150°C		
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V		
Input Voltage (Note 2)	-0.5V to +7.0V		
Input Current (Note 2)	-30 mA to +5.0 mA		
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)			
Standard Output	-0.5V to V _{CC}		
3-STATE Output	-0.5V to +5.5V		
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)		

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

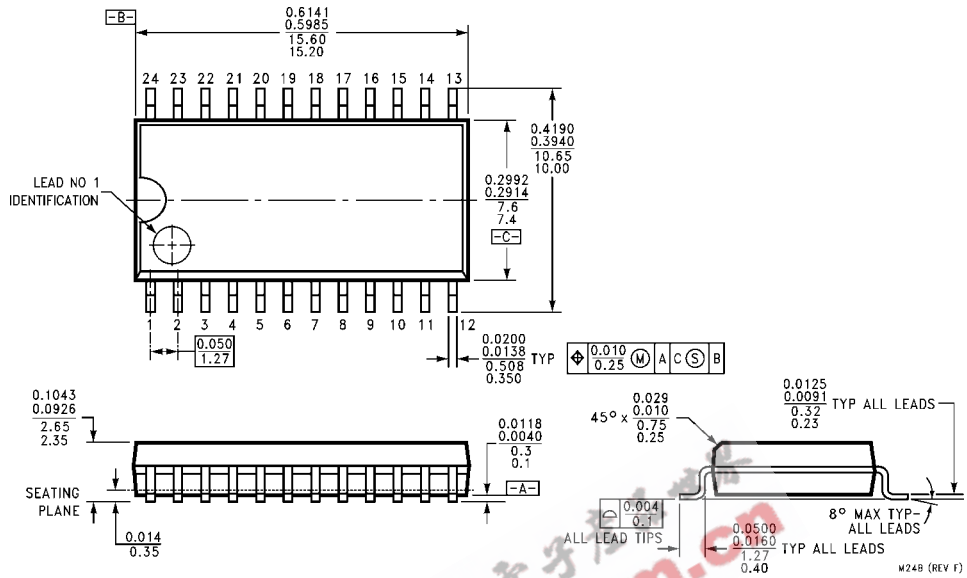
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC}	2.5			Min	I _{OH} = -1 mA (A _n)
		10% V _{CC}	2.4		I _{OH} = -3 mA (A _n , B _n , Parity, <u>ERROR</u>)		
		10% V _{CC}	2.0		I _{OH} = -15 mA (B _n , Parity, <u>ERROR</u>)		
		5% V _{CC}	2.7		I _{OH} = -1 mA (A _n)		
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 24 mA (A _n)
		10% V _{CC}		0.55	I _{OL} = 64 mA (B _n , Parity, <u>ERROR</u>)		
I _{IH}	Input HIGH Current			20	μA	Max	V _{IN} = 2.7V (ODD/ <u>EVEN</u>)
				40	V _{IN} = 2.7V (T/ <u>R</u> , <u>OE</u>)		
I _{BVI}	Input HIGH Current Breakdown Test			100	μA	V _{CC} = 0	V _{IN} = 7.0V (T/ <u>R</u> , <u>OE</u> , ODD/ <u>EVEN</u>)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			1.0 2.0	mA	Max	V _{IN} = 5.5V (Parity, B _n) V _{IN} = 5.5V (A _n)
I _{IL}	Input LOW Current			-20 -40	μA	Max	V _{IN} = 0.5V (ODD/ <u>EVEN</u>) V _{IN} = 0.5V (T/ <u>R</u> , <u>OE</u>)
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V (<u>ERROR</u>)
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V (<u>ERROR</u>)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{I/O} = 2.7V (B _n , Parity)
				90	V _{I/O} = 2.7V (A _n)		
I _{IL} + I _{OZL}	Output Leakage Current			-70	μA	Max	V _{I/O} = 0.5V (B _n , Parity)
				-90	V _{I/O} = 0.5V (A _n)		
I _{OS}	Output Short-Circuit Current			-60 -150	mA	Max	V _{OUT} = 0V (A _n)
				-100 -225	V _{OUT} = 0V (B _n , Parity, <u>ERROR</u>)		
I _{CEX}	Output HIGH Leakage Current			250	μA	Max	V _{OUT} = V _{CC} (<u>ERROR</u>)
				1.0	mA	Max	V _{OUT} = V _{CC} (B _n , Parity)
				2.0	mA	Max	V _{OUT} = V _{CC} (A _n)
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V (A _n , B _n , Parity, <u>ERROR</u>)
I _{CCH}	Power Supply Current		101	125	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		112	150	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		109	145	mA	Max	V _O = HIGH Z

AC Electrical Characteristics									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	2.5	4.5	8.0	2.5	9.5	2.5	9.0	ns
t_{PHL}	A_n to B_n , B_n to A_n	3.0	4.9	7.5	3.0	8.5	3.0	8.0	
t_{PLH}	Propagation Delay	6.5	10.1	14.0	5.5	18.0	6.0	16.0	ns
t_{PHL}	A_n to Parity	7.0	10.9	15.0	5.5	20.5	6.0	16.5	
t_{PLH}	Propagation Delay	4.5	7.8	11.0	4.0	14.0	4.0	13.0	ns
t_{PHL}	ODD/EVEN to PARITY	4.5	8.8	12.0	4.5	16.5	4.5	13.5	
t_{PLH}	Propagation Delay	4.5	7.5	11.0	4.0	14.0	4.0	13.0	ns
t_{PHL}	ODD/EVEN to ERROR	4.5	8.2	12.0	4.5	16.5	4.5	13.5	
t_{PLH}	Propagation Delay	8.0	14.0	20.5	7.5	27.0	7.5	23.0	ns
t_{PHL}	B_n to ERROR	8.0	15.0	21.5	7.5	28.5	7.5	23.5	
t_{PLH}	Propagation Delay	7.0	10.8	15.5	6.0	20.0	6.0	17.0	ns
t_{PHL}	PARITY to ERROR	7.5	11.8	16.5	6.5	22.0	7.5	18.5	
t_{PZH}	Output Enable Time	3.0	5.0	8.0	2.5	11.0	2.5	9.5	ns
t_{PZL}	\overline{OE} to A_n/B_n	4.0	6.5	10.0	3.5	13.5	3.5	11.0	
t_{PHZ}	Output Disable Time	1.0	4.5	8.0	1.0	9.5	1.0	9.0	ns
t_{PLZ}	\overline{OE} to A_n/B_n	1.0	4.9	7.5	1.0	8.5	1.0	8.0	
t_{PZH}	Output Enable Time	3.0	5.0	8.0	2.5	11.0	2.5	9.5	ns
t_{PZL}	\overline{OE} to ERROR (Note 3)	4.0	7.7	10.0	3.5	13.5	3.5	11.0	
t_{PHZ}	Output Disable Time	1.0	4.5	8.0	1.0	9.5	1.0	9.0	ns
t_{PLZ}	\overline{OE} to ERROR	1.0	4.9	7.5	1.0	8.5	1.0	8.0	
t_{PZH}	Output Enable Time	3.0	5.0	8.0	2.5	11.0	2.5	9.5	ns
t_{PZL}	\overline{OE} to PARITY	4.0	7.7	10.0	3.5	13.5	3.5	11.0	
t_{PHZ}	Output Disable Time	1.0	4.6	8.0	1.0	9.5	1.0	9.0	ns
t_{PLZ}	\overline{OE} to PARITY	1.0	5.1	7.5	1.0	8.5	1.0	8.0	

Note 3: These delay times reflect the 3-STATE recovery time only and not the signal time through the buffers or the parity check circuitry. To assure VALID information at the ERROR pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the ERROR output after the ERROR pin has been enabled (Output Enable times). VALID data at the ERROR pin \geq (A to PARITY) + (Output Enable Time).

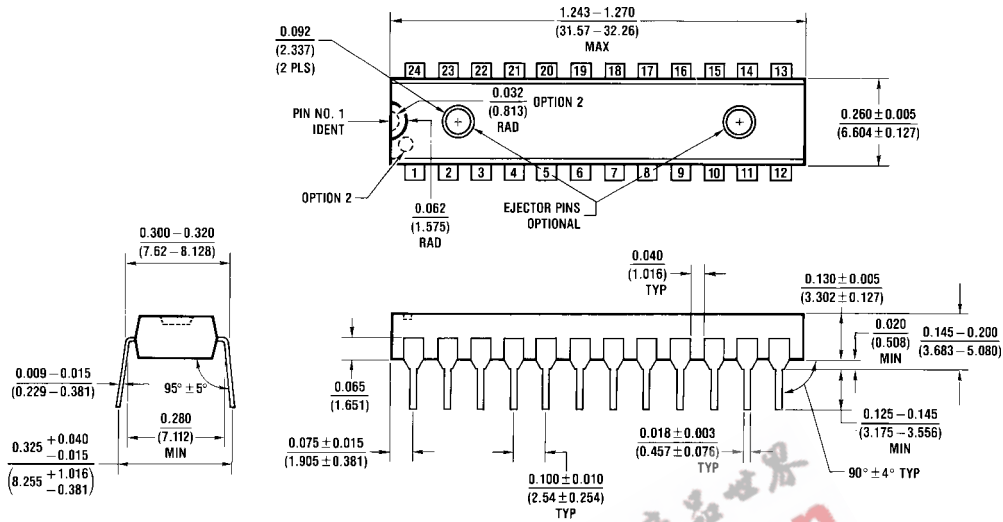
74F657

Physical Dimensions inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide Package Number N24C

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