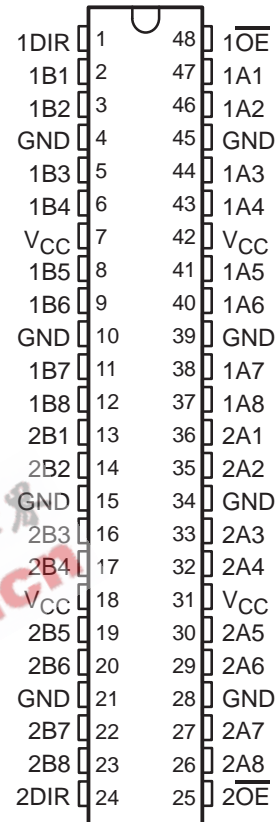


# SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS2600 – JUNE 1993 – REVISED SEPTEMBER 2003

- Members of the Texas Instruments Widebus™ Family
- A-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce) <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

SN54LVTH162245 . . . WD PACKAGE  
SN74LVTH162245 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description/ordering information

The 'LVTH162245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LVTH162245DL	LVTH162245
		Tape and reel	SN74LVTH162245DLR	
	TSSOP – DGG	Tape and reel	SN74LVTH162245DGGR	LVTH162245
	VFBGA – GQL	Tape and reel	SN74LVTH162245KR	LL2245
VFBGA – ZQL (Pb-free)	74LVTH162245ZQLR			
–55°C to 125°C	CFP – WD	Tube	SNJ54LVTH162245WD	SNJ54LVTH162245WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## description/ordering information (continued)

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

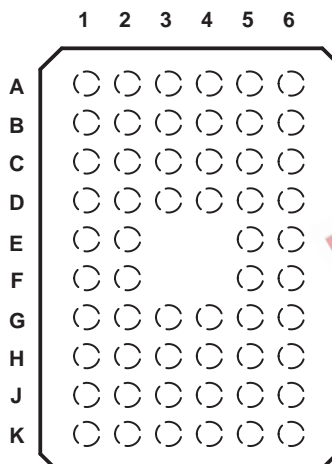
The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22- $\Omega$  series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

### GQL OR ZQL PACKAGE (TOP VIEW)



### terminal assignments

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	$\overline{1OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	$V_{CC}$	$V_{CC}$	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	$V_{CC}$	$V_{CC}$	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	$\overline{2OE}$

NC – No internal connection

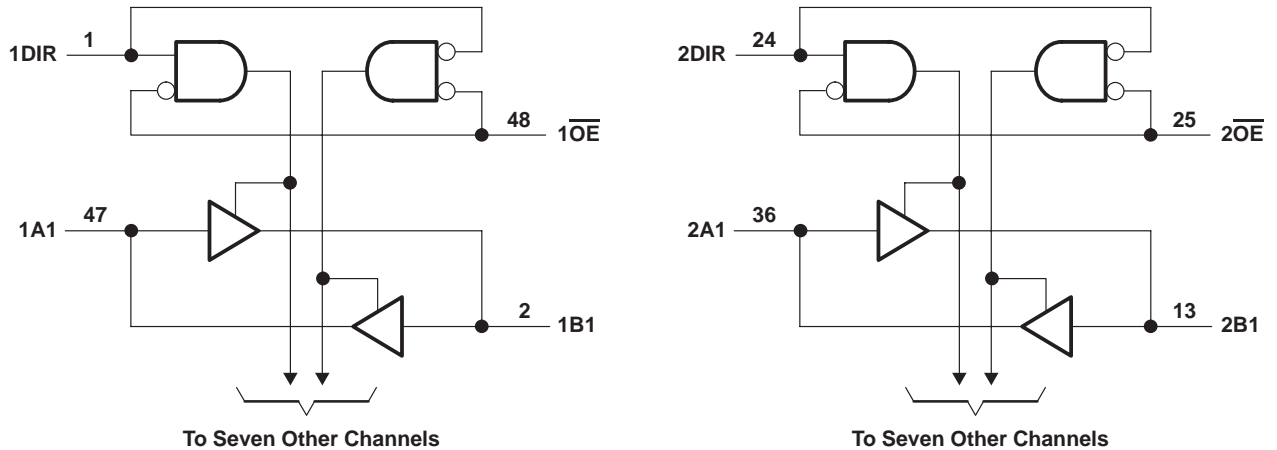
### FUNCTION TABLE (each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

# SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



Pin numbers shown are for the DGG, DL, and WD packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$ : SN54LVTH162245 (B port) .....	96 mA
SN74LVTH162245 (B port) .....	128 mA
A port .....	30 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH162245 (B port) .....	48 mA
SN74LVTH162245 (B port) .....	64 mA
A port .....	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package .....	70°C/W
DL package .....	63°C/W
GQL/ZQL package .....	42°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
3. The package thermal impedance is calculated in accordance with JESD 51-7.

**SN54LVTH162245, SN74LVTH162245**  
**3.3-V ABT 16-BIT BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 4)**

		SN54LVTH162245		SN74LVTH162245		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2.7	3.6	2.7	3.6	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage		5.5		5.5	V
I <sub>OH</sub>	High-level output current	A port	-12	-12		mA
		B port	-24	-32		
I <sub>OL</sub>	Low-level output current	A port	12	12		mA
		B port	48	64		
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate	200		200		μs/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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# SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54LVTH162245			SN74LVTH162245			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$	A port	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$	$V_{CC}-0.2$		V	
		$V_{CC} = 3\text{ V}$ , $I_{OH} = -12\text{ mA}$		2	2			
	B port	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$	$V_{CC}-0.2$			
		$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$		2.4	2.4			
		$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2				
$I_{OH} = -32\text{ mA}$			2					
$V_{OL}$	A port	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ , $I_{OL} = 100\text{ }\mu\text{A}$			0.2	0.2		
		$V_{CC} = 3\text{ V}$ , $I_{OL} = 12\text{ mA}$			0.8	0.8		
	B port	$V_{CC} = 2.7\text{ V}$		$I_{OL} = 100\text{ }\mu\text{A}$	0.2	0.2		
				$I_{OL} = 24\text{ mA}$	0.5	0.5		
		$V_{CC} = 3\text{ V}$		$I_{OL} = 16\text{ mA}$	0.4	0.4		
				$I_{OL} = 32\text{ mA}$	0.5	0.5		
				$I_{OL} = 48\text{ mA}$	0.55	0.55		
			$I_{OL} = 64\text{ mA}$		0.55			
$I_I$	Control inputs	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$		$\pm 1$	$\pm 1$			
		$V_{CC} = 0\text{ or }3.6\text{ V}$ , $V_I = 5.5\text{ V}$		10	10			
	A or B ports‡	$V_{CC} = 3.6\text{ V}$		$V_I = 5.5\text{ V}$	20	20		
				$V_I = V_{CC}$	5	5		
				$V_I = 0$	-10	-10		
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				$\pm 100$			
$I_I(\text{hold})$	A or B ports	$V_{CC} = 3\text{ V}$ , $V_I = 0.8\text{ V}$		75	75			
		$V_{CC} = 3\text{ V}$ , $V_I = 2\text{ V}$		-75	-75			
		$V_{CC} = 3.6\text{ V}^{\S}$ , $V_I = 0\text{ to }3.6\text{ V}$			500 -750			
$I_{OZPU}$	$V_{CC} = 0\text{ to }1.5\text{ V}$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $\overline{OE} = \text{don't care}$			$\pm 100^*$	$\pm 100$			
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to }0$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $\overline{OE} = \text{don't care}$			$\pm 100^*$	$\pm 100$			
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$		Outputs high	0.19	0.19			
			Outputs low	5	5			
			Outputs disabled	0.19	0.19			
$\Delta I_{CC}^{\parallel}$	$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$			0.3	0.2			
$C_i$	$V_I = 3\text{ V or }0$			4	4			
$C_{io}$	$V_O = 3\text{ V or }0$			10	10			

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Unused pins at  $V_{CC}\text{ or GND}$ .

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}\text{ or GND}$ .

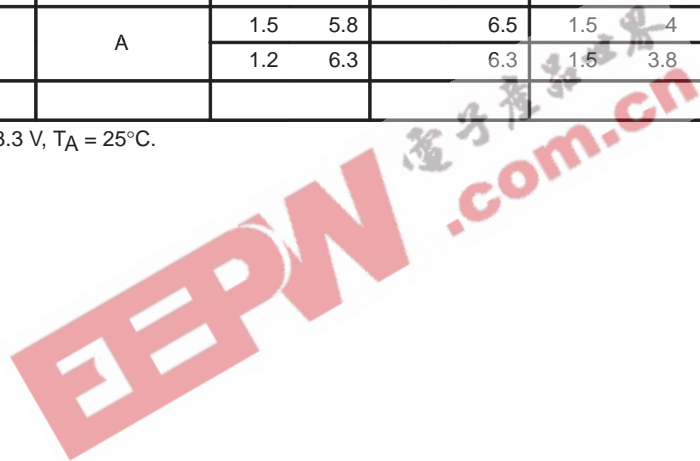
**SN54LVTH162245, SN74LVTH162245**  
**3.3-V ABT 16-BIT BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

SCBS2600 – JUNE 1993 – REVISED SEPTEMBER 2003

switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$   
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162245				SN74LVTH162245				UNIT	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
$t_{PLH}$	A	B	1	3.5	4		1	2.3	3.3	3.7		ns
$t_{PHL}$			1	3.5	3.9		1	2.2	3.3	3.5		
$t_{PLH}$	B	A	1	4.3	5.3		1	2.8	4	4.6		ns
$t_{PHL}$			1	4.2	4.5		1	2.5	3.4	3.6		
$t_{PZH}$	$\overline{OE}$	B	1	4.8	5.9		1	2.8	4.6	5.4		ns
$t_{PZL}$			1	4.8	5.5		1	3	4.6	5.2		
$t_{PZH}$	$\overline{OE}$	A	1	5.5	7.2		1	3.3	5.3	6.3		ns
$t_{PZL}$			1	5.4	6.4		1	3.3	5.1	5.8		
$t_{PHZ}$	$\overline{OE}$	B	1.5	5.5	5.8		1.5	3.8	5.2	5.5		ns
$t_{PLZ}$			1.5	5.5	5.8		1.5	3.5	5.1	5.4		
$t_{PHZ}$	$\overline{OE}$	A	1.5	5.8	6.5		1.5	4	5.6	5.9		ns
$t_{PLZ}$			1.2	6.3	6.3		1.5	3.8	5.5	5.5		
$t_{sk(o)}$								0.5			ns	

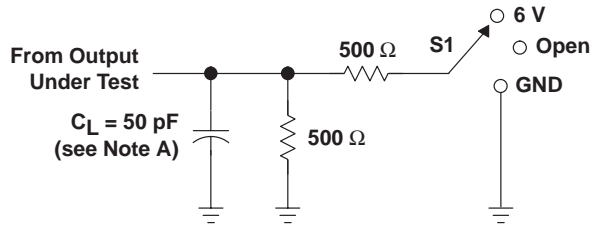
† All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .



# SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

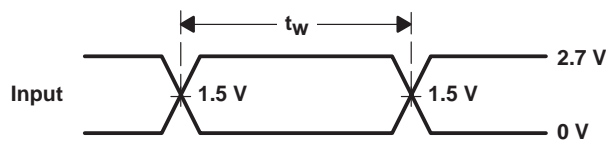
SCBS2600 – JUNE 1993 – REVISED SEPTEMBER 2003

## PARAMETER MEASUREMENT INFORMATION

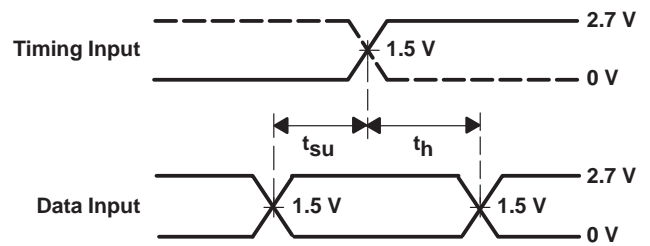


LOAD CIRCUIT

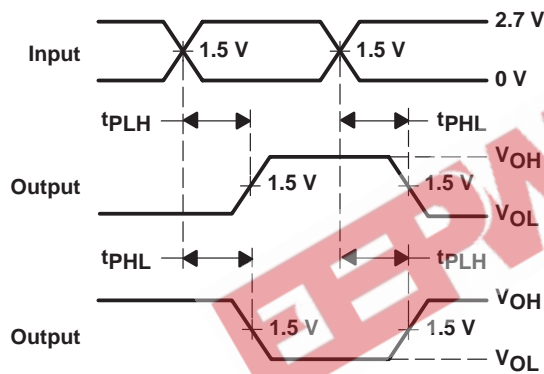
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



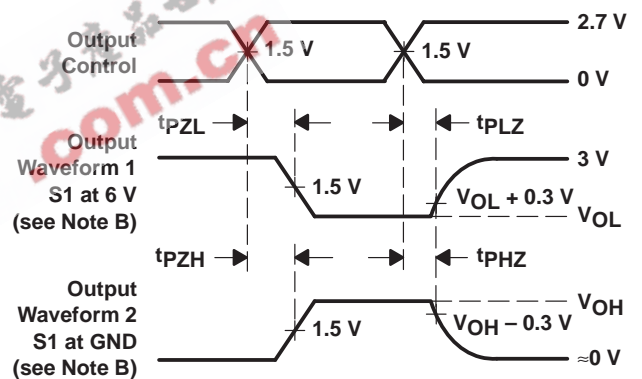
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9678001QXA	ACTIVE	CFP	WD	48	1	TBD	Call TI	Level-NC-NC-NC
5962-9678001VXA	ACTIVE	CFP	WD	48	1	TBD	Call TI	Level-NC-NC-NC
74LVTH162245DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVTH162245DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVTH162245GRDR	ACTIVE	LFBGA	GRD	54	1000	TBD	SNPB	Level-1-240C-UNLIM
74LVTH162245GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVTH162245ZQLR	ACTIVE	VFBGA	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
74LVTH162245ZRDR	ACTIVE	LFBGA	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74LVTH162245DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH162245DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH162245DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH162245DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH162245KR	ACTIVE	VFBGA	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SNJ54LVTH162245WD	ACTIVE	CFP	WD	48	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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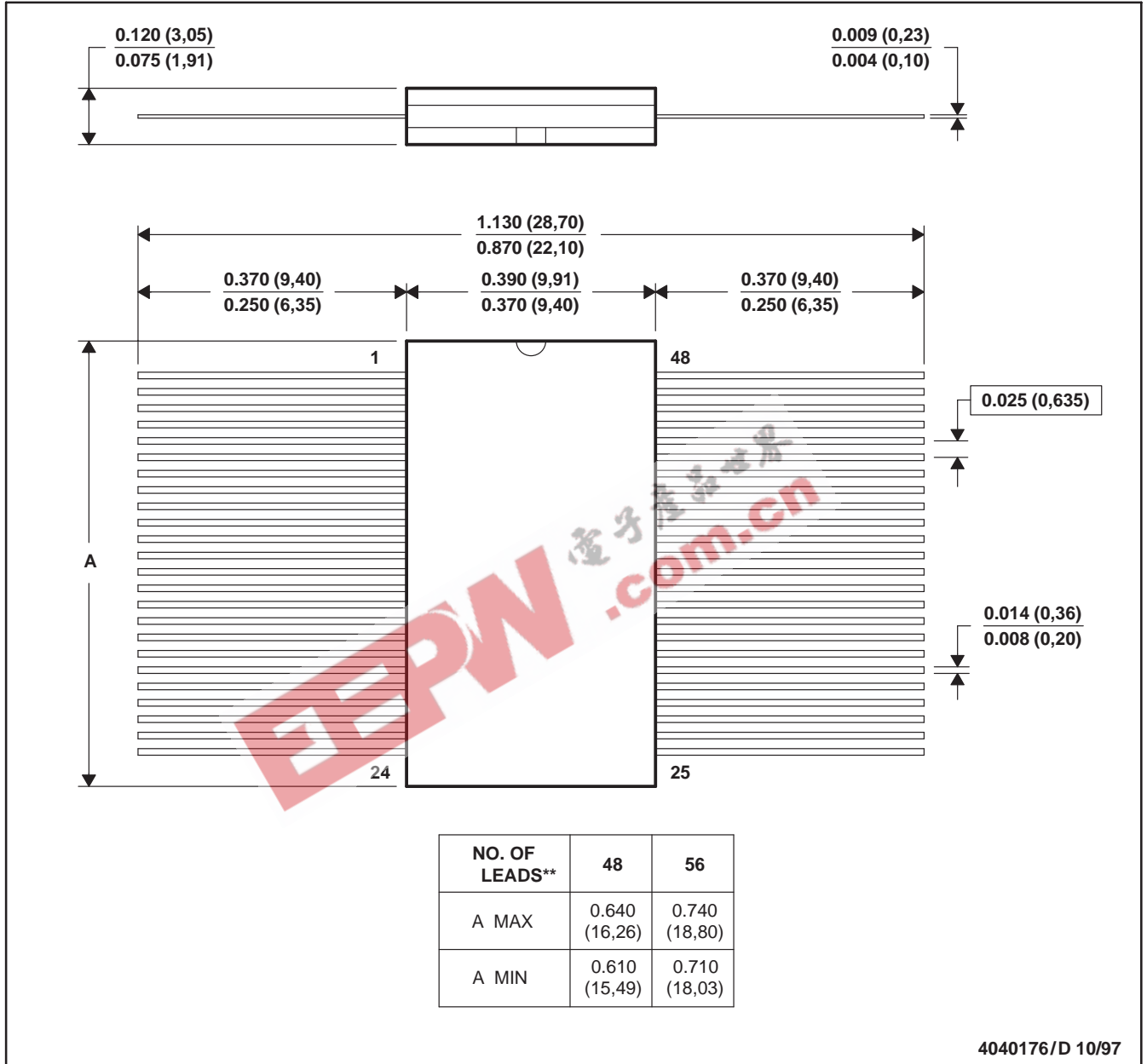
# MECHANICAL DATA

MCFP010B – JANUARY 1995 – REVISED NOVEMBER 1997

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN

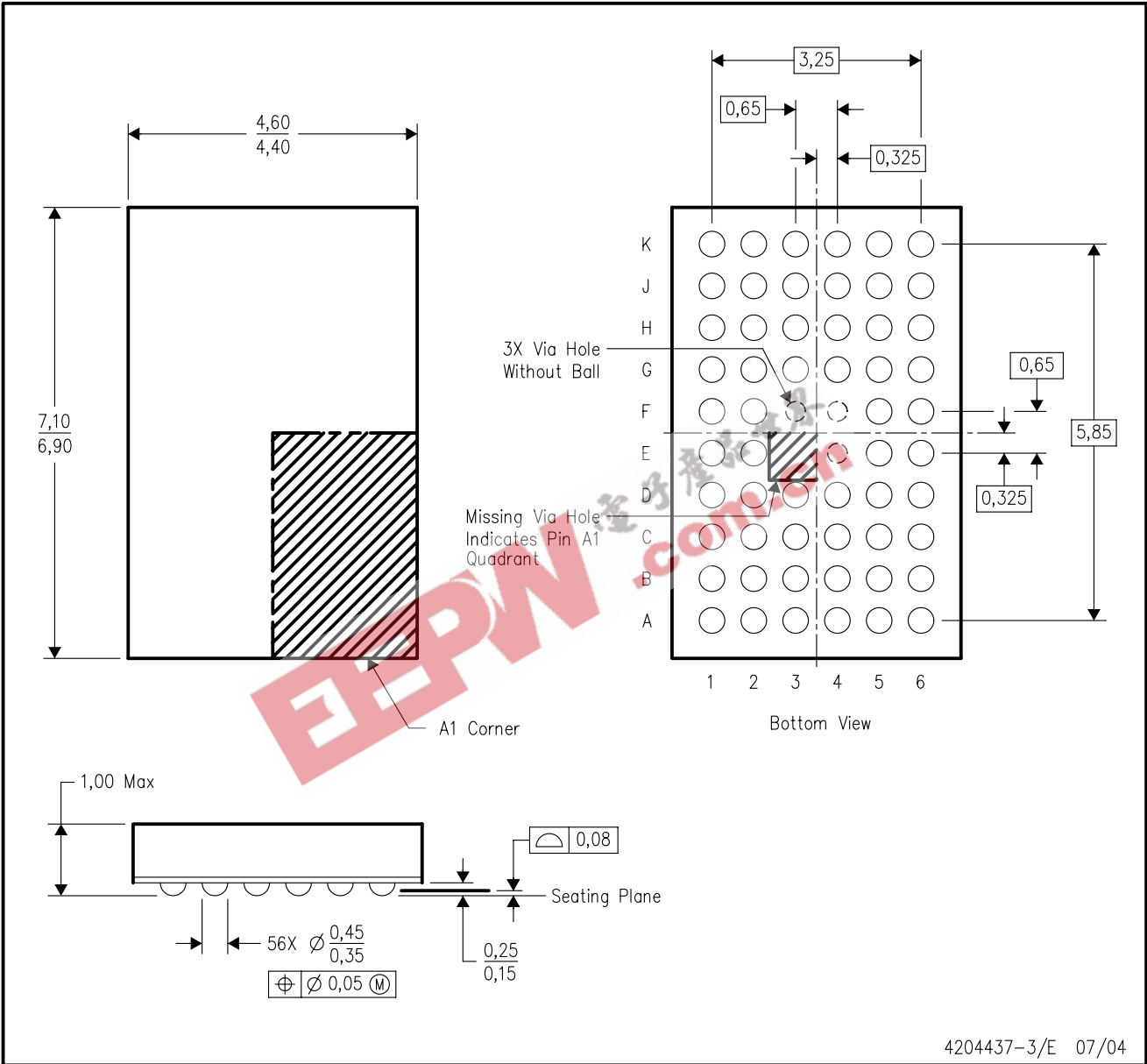


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

MECHANICAL DATA

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



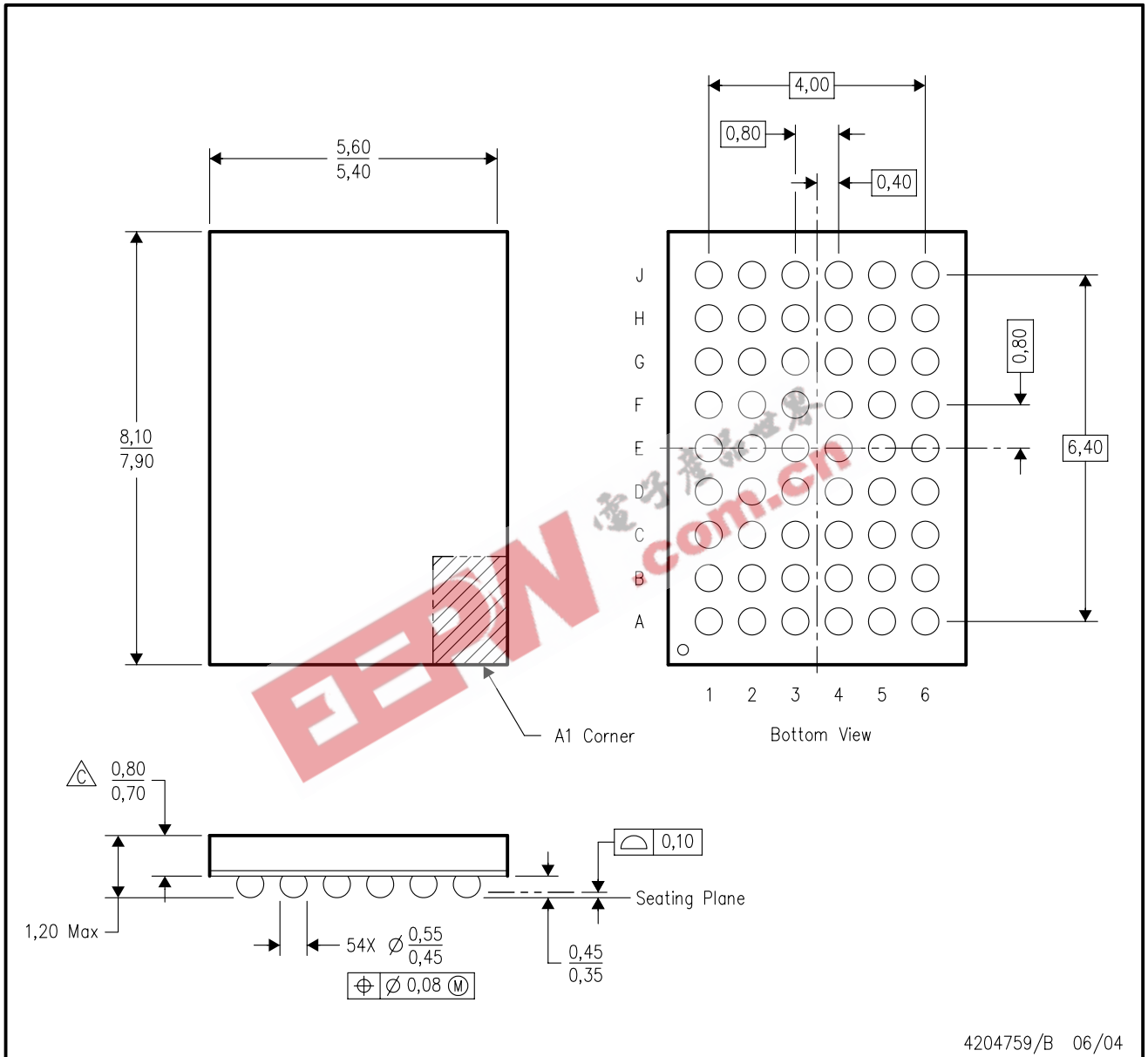
4204437-3/E 07/04

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BA.
  - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

# MECHANICAL DATA

GRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY

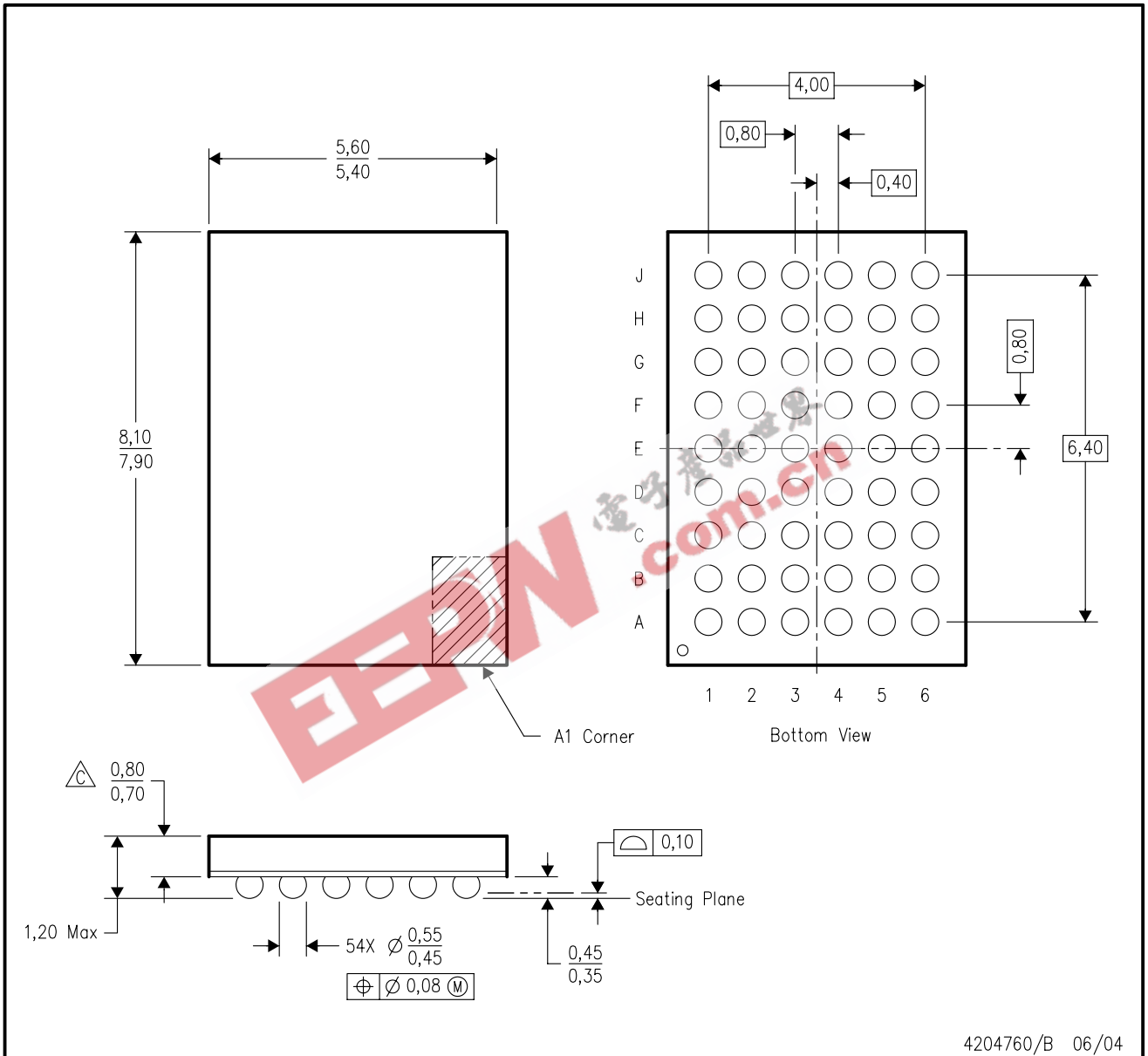


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MO-205 variation DD.
  - D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

# MECHANICAL DATA

ZRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY

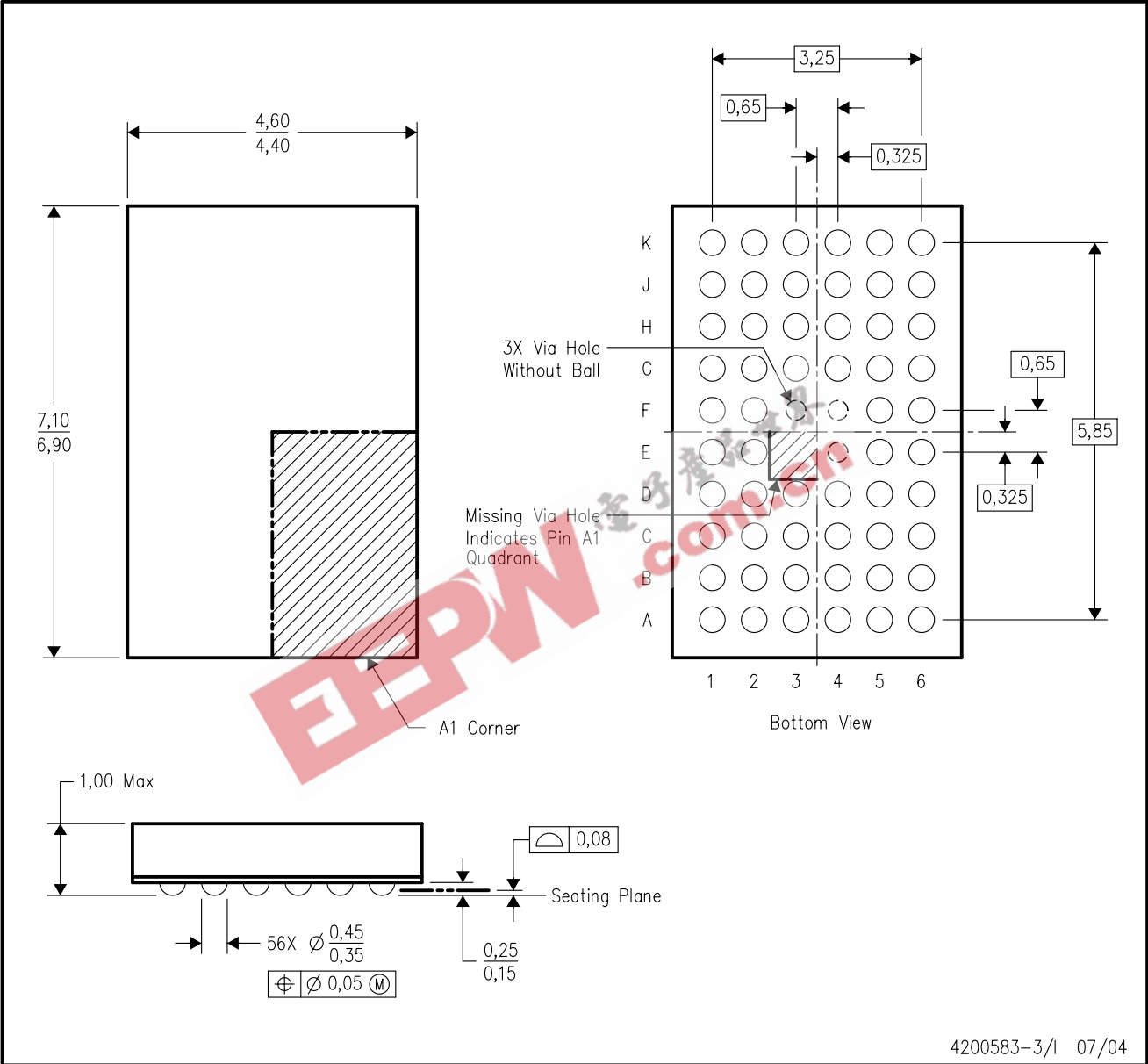


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation DD.
  - D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

MECHANICAL DATA

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



4200583-3/1 07/04

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BA.
  - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

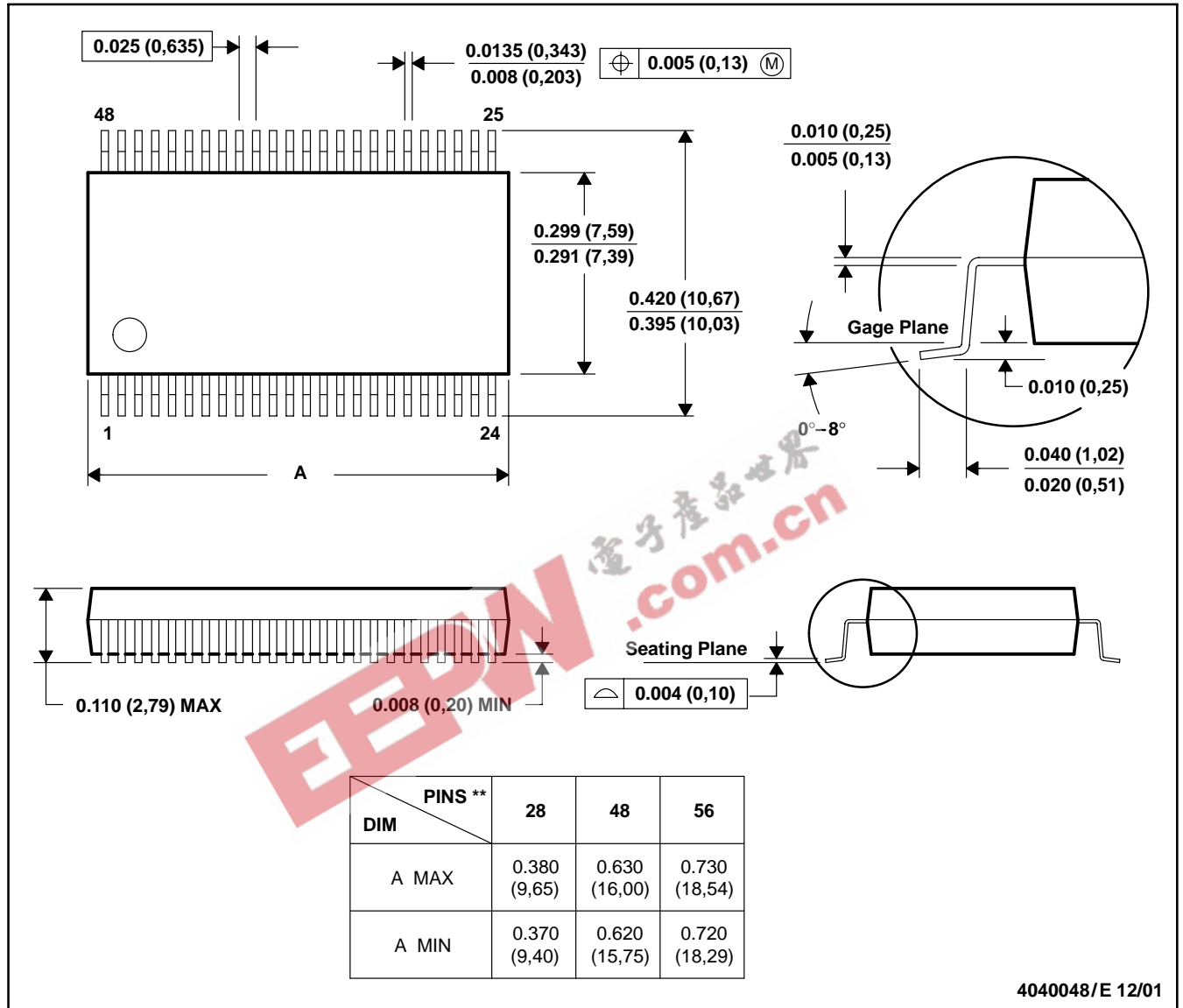
# MECHANICAL DATA

MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

## DL (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

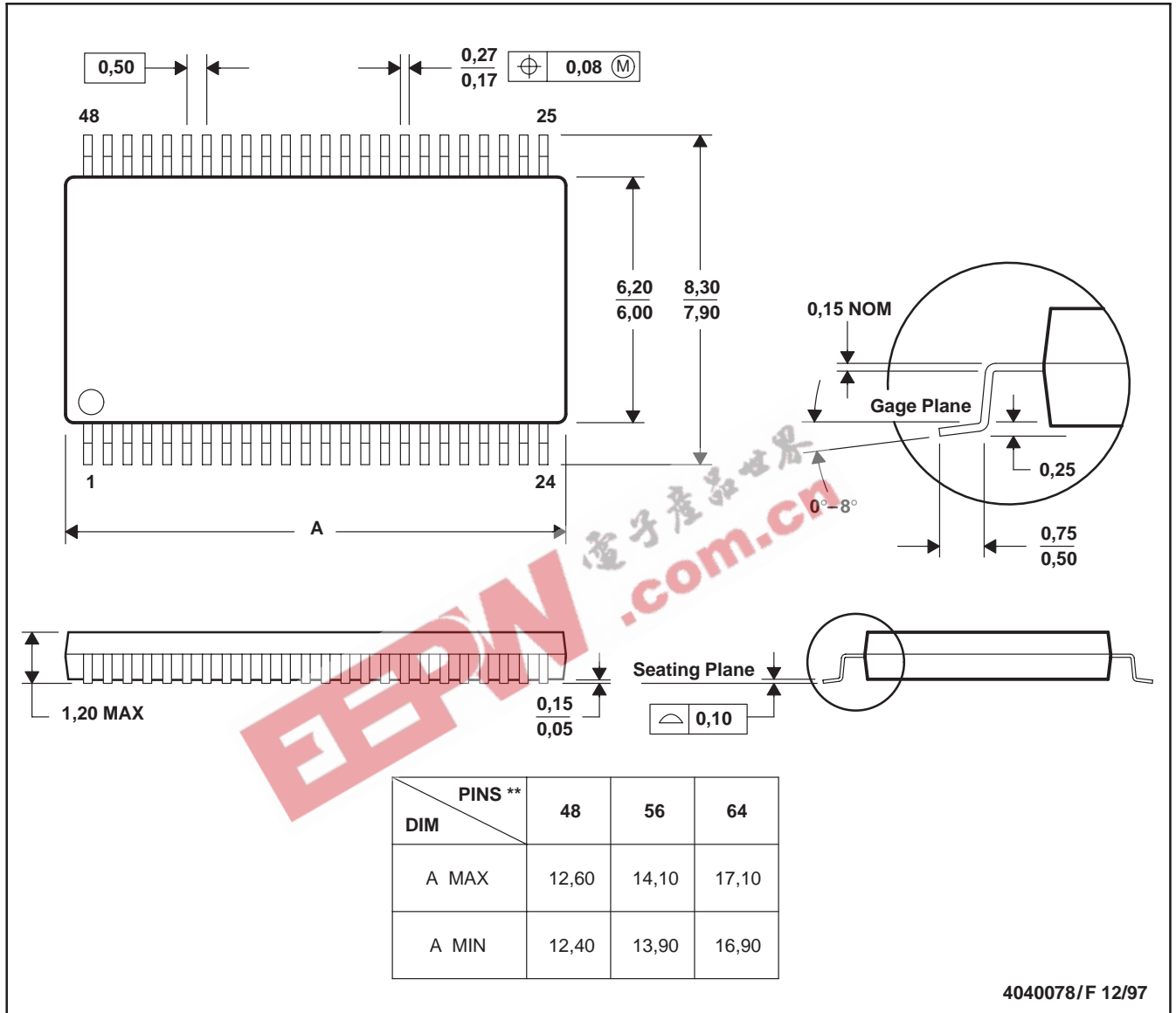
# MECHANICAL DATA

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



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