

## Octal D-type transparent latch (3-State)

## 74ABT573A

## FEATURES

- 74ABT573A is flow-through pinout version of 74ABT373
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State output buffers
- Common output enable
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset

## DESCRIPTION

The 74ABT573A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT573A device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ( $\overline{OE}$ ) control gates. The 74ABT573A is functionally identical to the 74ABT373 but has a flow-through pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ( $\overline{OE}$ ) controls all eight 3-State buffers independent of the latch operation.

When  $\overline{OE}$  is Low, the latched or transparent data appears at the outputs. When  $\overline{OE}$  is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

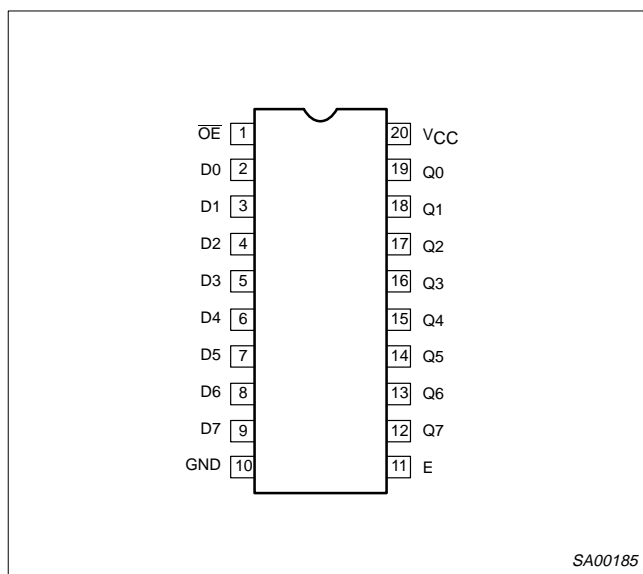
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay Dn to Qn	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	2.8 3.3	ns
$C_{IN}$	Input capacitance	$V_I = 0\text{V}$ or $V_{CC}$	3	pF
$C_{OUT}$	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or $V_{CC}$	6	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	100	$\mu\text{A}$

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74ABT573A N	74ABT573A N	SOT146-1
20-Pin plastic SO	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74ABT573A D	74ABT573A D	SOT163-1
20-Pin Plastic SSOP Type II	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74ABT573A DB	74ABT573A DB	SOT339-1
20-Pin Plastic TSSOP Type I	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74ABT573A PW	74ABT573APW DH	SOT360-1

## PIN CONFIGURATION



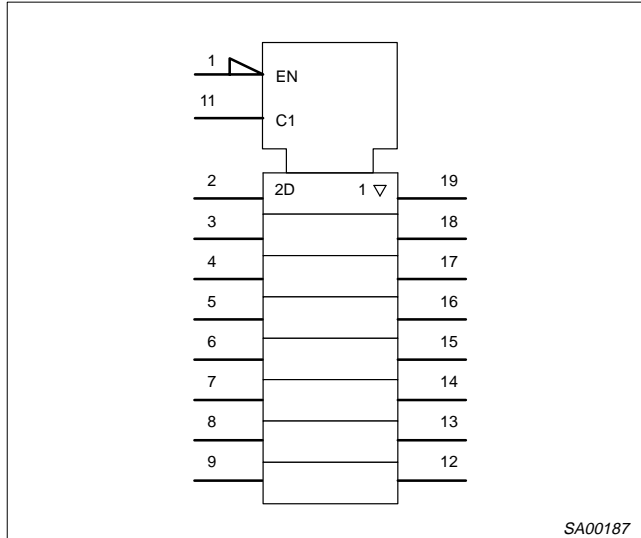
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	E	Enable input (active-High)
10	GND	Ground (0V)
20	$V_{CC}$	Positive supply voltage

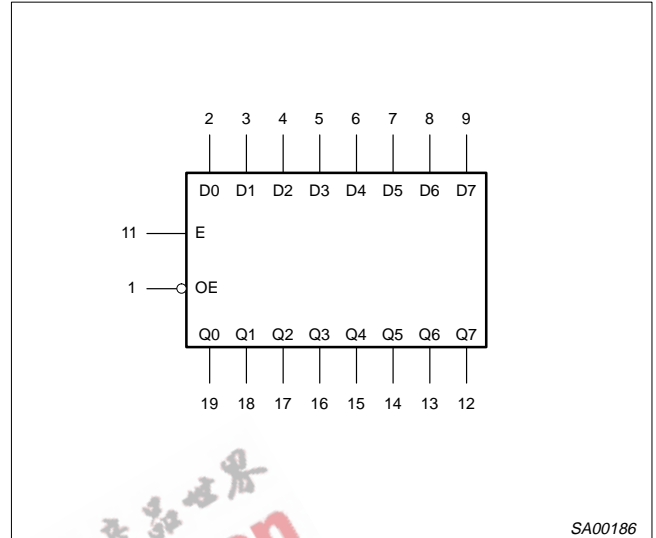
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## LOGIC SYMBOL (IEEE/IEC)



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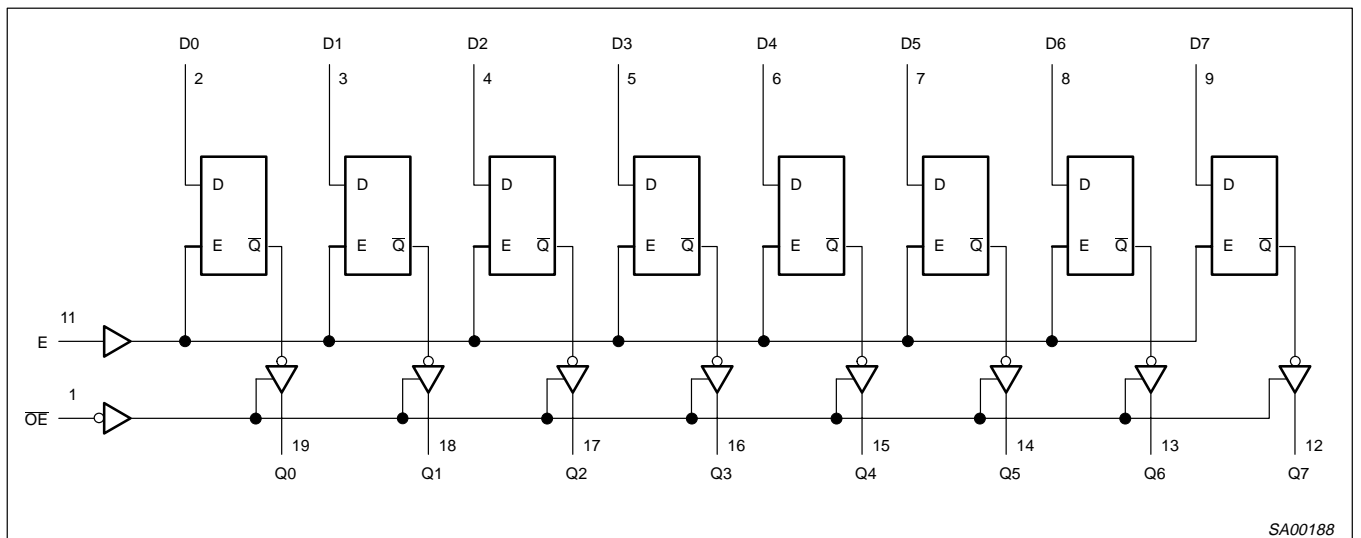


## FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS Q0 – Q7	OPERATING MODE
OE	E	Dn			
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

- H = High voltage level
- h = High voltage level one set-up time prior to the High-to-Low E transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the High-to-Low E transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- ↓ = High-to-Low E transition

## LOGIC DIAGRAM



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**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$I_{IK}$	DC input diode current	$V_I < 0$	-18	mA
$V_I$	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$	-50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	output in Off or High state	-0.5 to +5.5	V
$I_{OUT}$	DC output current	output in Low state	128	mA
$T_{stg}$	Storage temperature range		-65 to 150	°C

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Low-level input voltage		0.8	V
$I_{OH}$	High-level output current		-32	mA
$I_{OL}$	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = -18mA		-0.9	-1.2		-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.5	2.9		2.5		V
		V <sub>CC</sub> = 5.0V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	3.0	3.4		3.0		V
		V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -32mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.0	2.4		2.0		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 64mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		0.42	0.55		0.55	V
V <sub>RST</sub>	Power-up output low voltage <sup>3</sup>	V <sub>CC</sub> = 5.5V; I <sub>O</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>		0.13	0.55		0.55	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V		±0.01	±1.0		±1.0	μA
I <sub>OFF</sub>	Power-off leakage current	V <sub>CC</sub> = 0.0V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5V		±5.0	±100		±100	μA
I <sub>PU/</sub> I <sub>PD</sub>	Power-up/down 3-State output current <sup>4</sup>	V <sub>CC</sub> = 2.0V; V <sub>O</sub> = 0.5V; V <sub>OE</sub> = Don't Care; V <sub>I</sub> = GND or V <sub>CC</sub>		±5.0	±50		±50	μA
I <sub>OZH</sub>	3-State output High current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.7V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		5.0	50		50	μA
I <sub>OZL</sub>	3-State output Low current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		-5.0	-50		-50	μA
I <sub>CEX</sub>	Output High leakage current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>		5.0	50		50	μA
I <sub>O</sub>	Output current <sup>1</sup>	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V	-40		-180	-40	-180	mA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub>		100	250		250	μA
I <sub>CCL</sub>		V <sub>CC</sub> = 5.5V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub>		24	30		30	mA
I <sub>CCZ</sub>		V <sub>CC</sub> = 5.5V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>		100	250		250	μA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 5.5V; one input at 3.4V, other inputs at V <sub>CC</sub> or GND		0.5	1.5		1.5	mA

## NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V<sub>CC</sub> between 0V and 2.1V with a transition time of up to 10msec. For V<sub>CC</sub> = 2.1V to V<sub>CC</sub> = 5V ± 10%, a transition time of up to 100μsec is permitted.

## AC CHARACTERISTICS

GND = 0V, t<sub>R</sub> = t<sub>F</sub> = 2.5ns, C<sub>L</sub> = 50pF, R<sub>L</sub> = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V			T <sub>amb</sub> = -40 to +85°C V <sub>CC</sub> = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dn to Qn	2	1.5 2.2	2.8 3.3	4.0 4.8	1.5 2.2	4.5 5.3	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay E to Qn	1	1.2 1.8	2.5 3.0	4.0 4.4	1.2 1.8	4.5 4.7	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to High and Low level	4 5	1.2 2.7	3.0 3.8	4.5 5.3	1.2 2.7	5.2 5.7	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from High and Low level	4 5	1.5 1.2	2.8 2.2	4.1 3.4	1.5 1.2	4.5 3.8	ns

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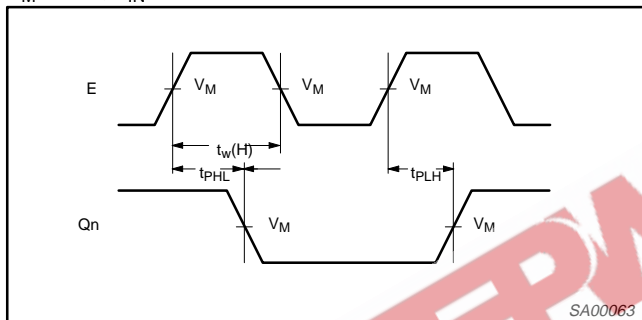
## AC SETUP REQUIREMENTS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$

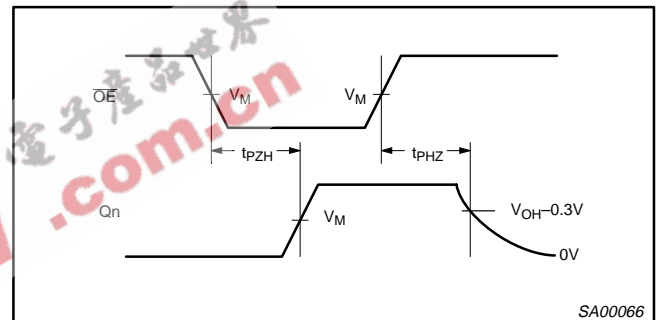
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			Min	Typ	Min	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low Dn to E	3	1.0 1.0	0.3 0.2	1.0 1.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low Dn to E	3	1.0 1.0	-0.1 -0.2	1.0 1.0	ns
$t_w(\text{H})$	E pulse width High	1	2.0	0.7	2.0	ns

## AC WAVEFORMS

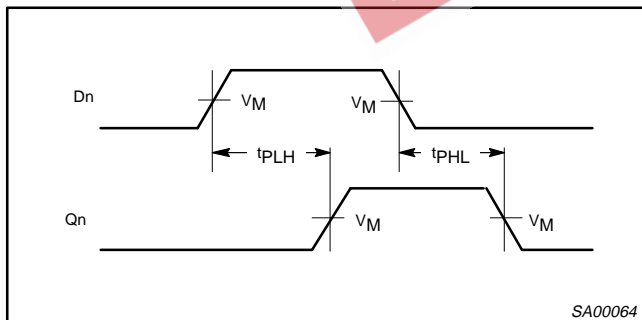
$V_M = 1.5\text{V}$ ,  $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



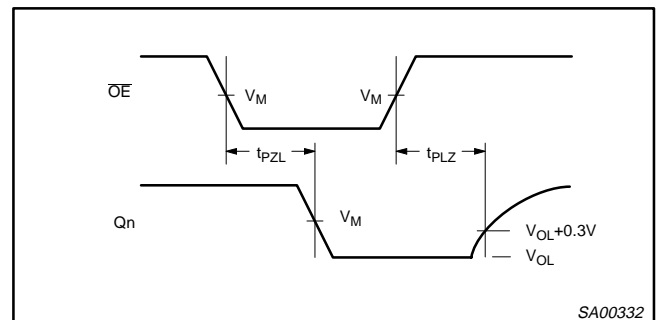
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



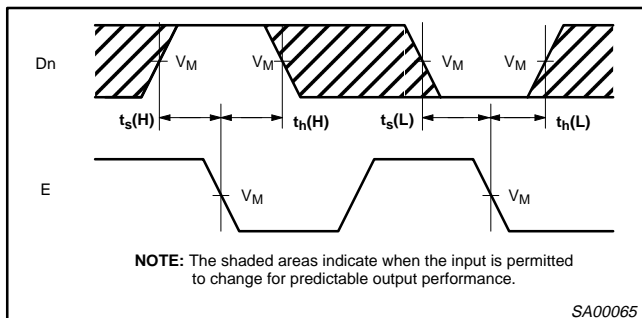
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Propagation Delay for Data to Outputs



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 3. Data Setup and Hold Times

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## TEST CIRCUIT AND WAVEFORM

**Test Circuit for 3-State Outputs**

**Input Pulse Definition**

$V_M = 1.5V$

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_R$	$t_F$
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012