

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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## 74HC/HCT368

Hex buffer/line driver; 3-state;  
inverting

Product specification  
File under Integrated Circuits, IC06

December 1990

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## 74HC/HCT368

## FEATURES

- Inverting outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT368 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT368 are hex inverting buffer/line drivers with 3-state outputs. The 3-state outputs ( $\overline{nY}$ ) are controlled by the output enable inputs ( $1\overline{OE}$ ,  $2\overline{OE}$ ).

A HIGH on  $\overline{nOE}$  causes the outputs to assume a high impedance OFF-state.

The "368" is identical to the "367" but has inverting outputs.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to $\overline{nY}$	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	9	11	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz  
 f<sub>o</sub> = output frequency in MHz  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in V
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

## ORDERING INFORMATION

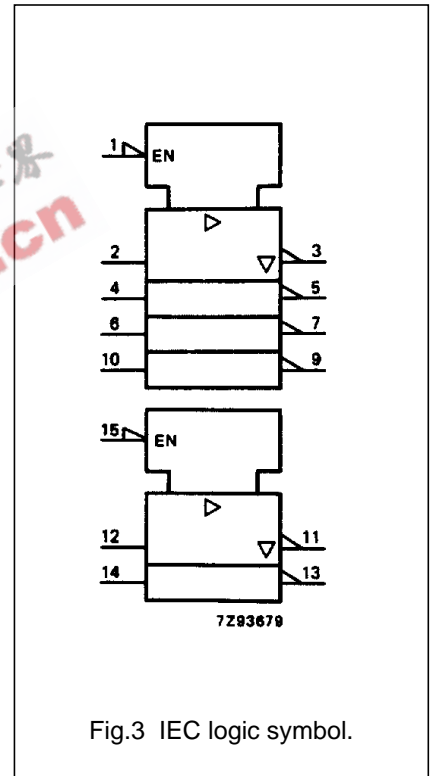
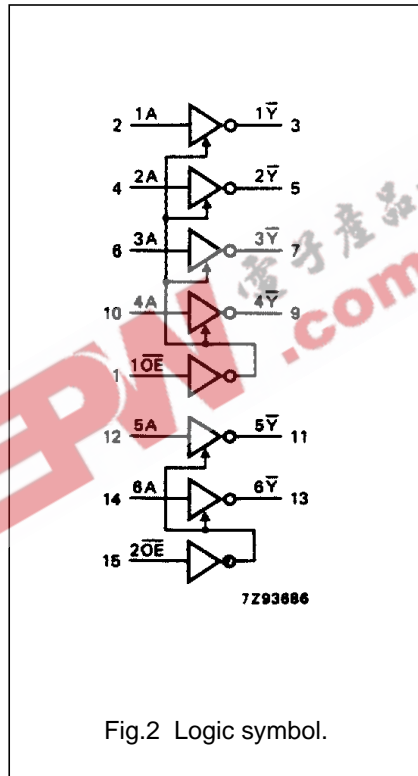
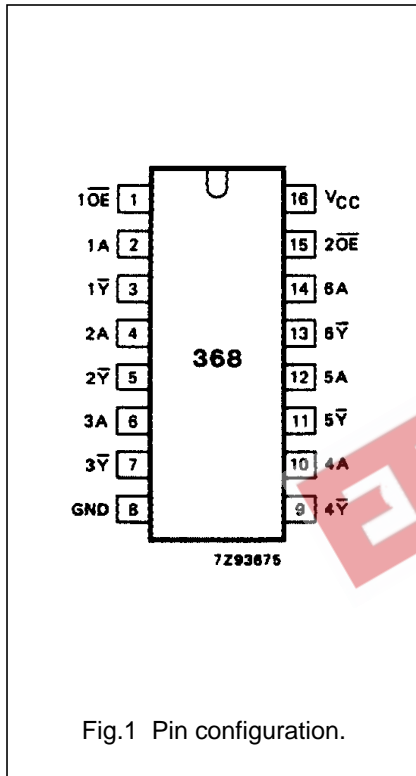
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{1OE}, \overline{2OE}$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	$1\overline{Y}$ to $6\overline{Y}$	data outputs
8	GND	ground (0 V)
16	V <sub>CC</sub>	positive supply voltage



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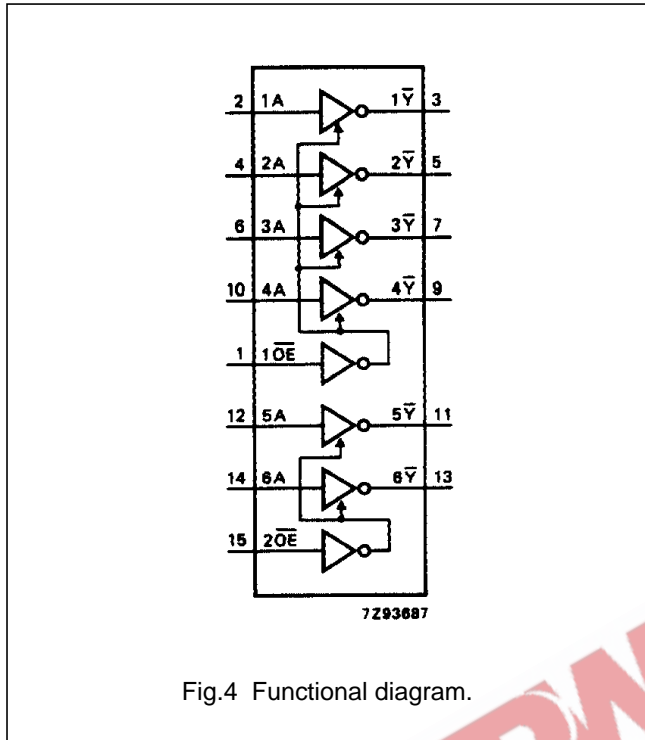


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nA	$n\overline{Y}$
L	L	H
L	H	L
H	X	Z

Note

1. H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 Z = high impedance OFF-state

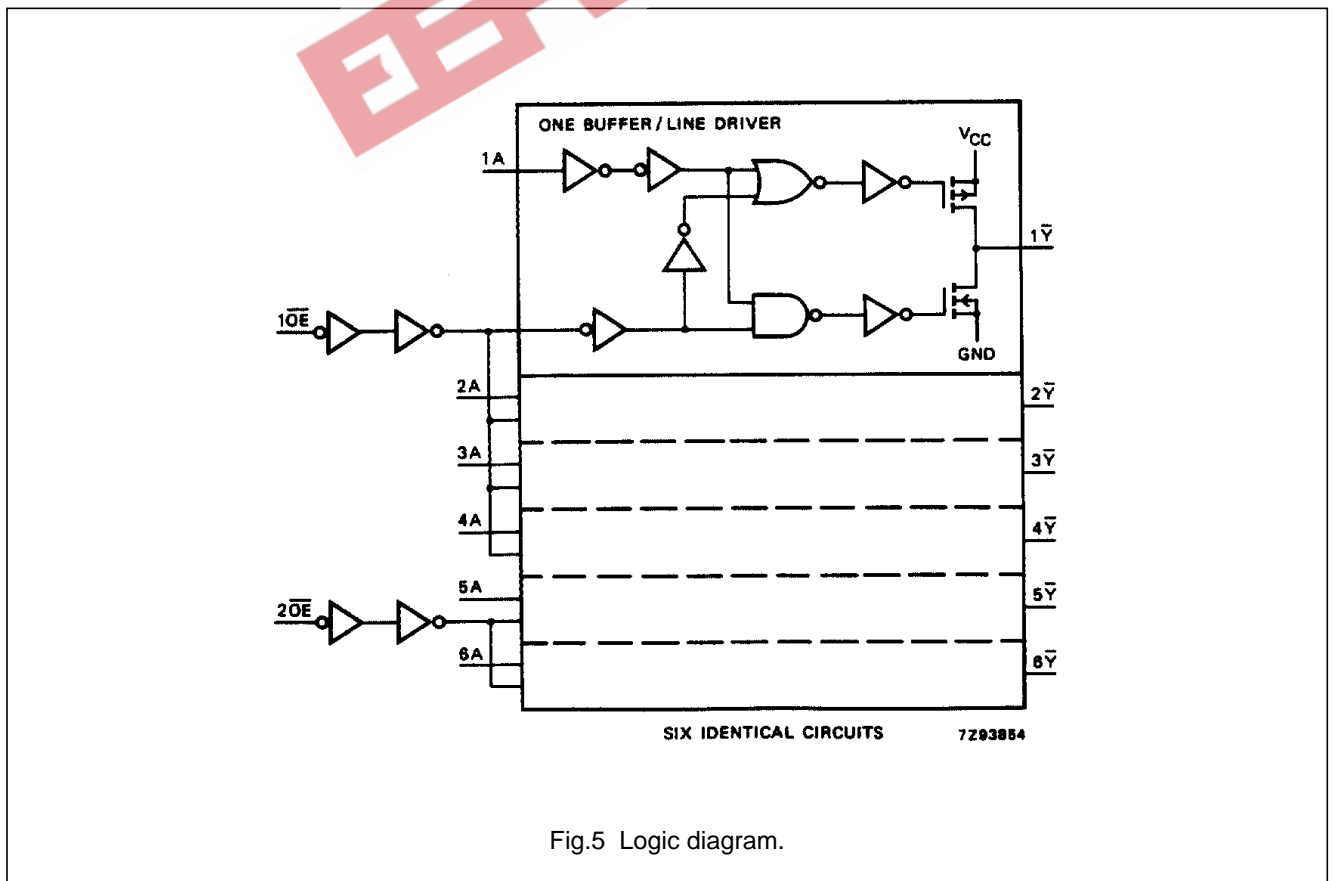


Fig.5 Logic diagram.

## Hex buffer/line driver; 3-state; inverting

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to n $\bar{Y}$		30 11 9	95 19 16		120 24 20	145 29 25	ns	2.0 4.5 6.0	Fig.6	
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time n $\bar{OE}$ to n $\bar{Y}$		41 15 12	150 30 26		190 38 33	225 45 38	ns	2.0 4.5 6.0	Fig.7	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time n $\bar{OE}$ to n $\bar{Y}$		55 20 16	150 30 26		190 38 33	225 45 38	ns	2.0 4.5 6.0	Fig.7	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13	90 18 15	ns	2.0 4.5 6.0	Fig.6	

## Hex buffer/line driver; 3-state; inverting

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{1OE}$	1.00
$\overline{2OE}$	0.90
nA	1.00

**AC CHARACTERISTICS FOR 74HCT**

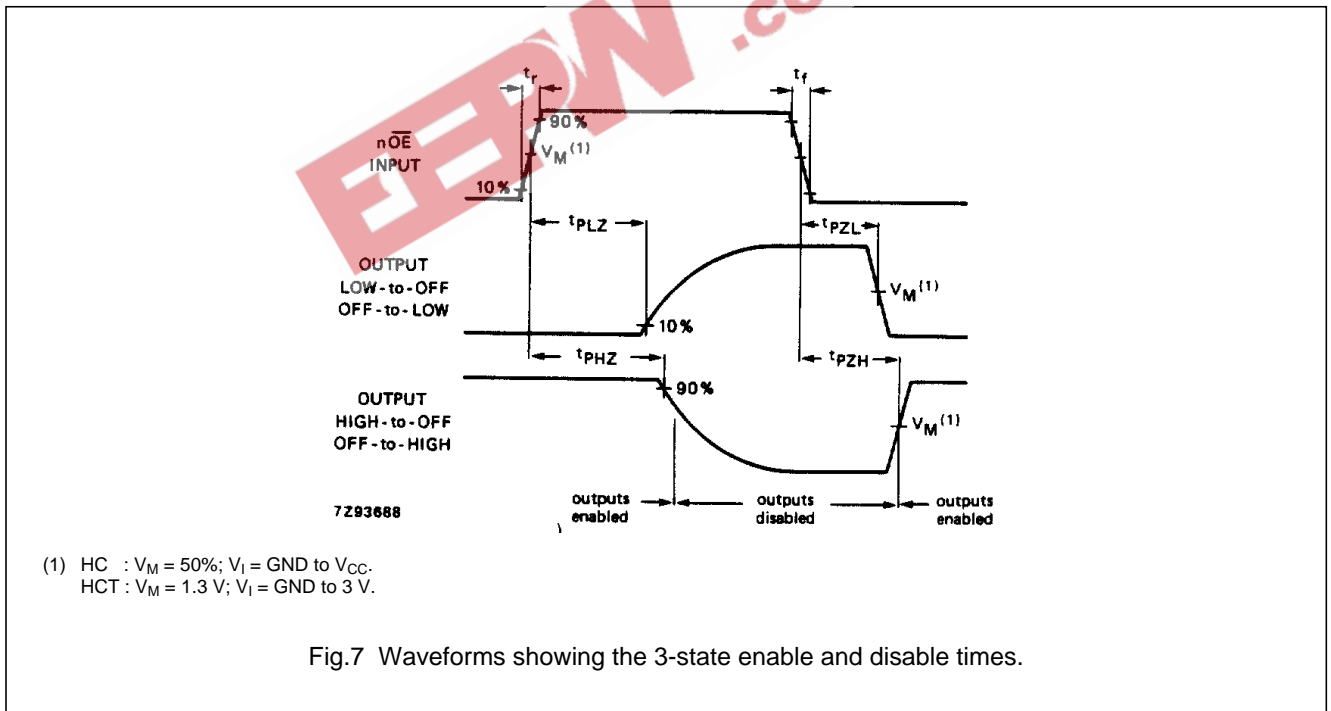
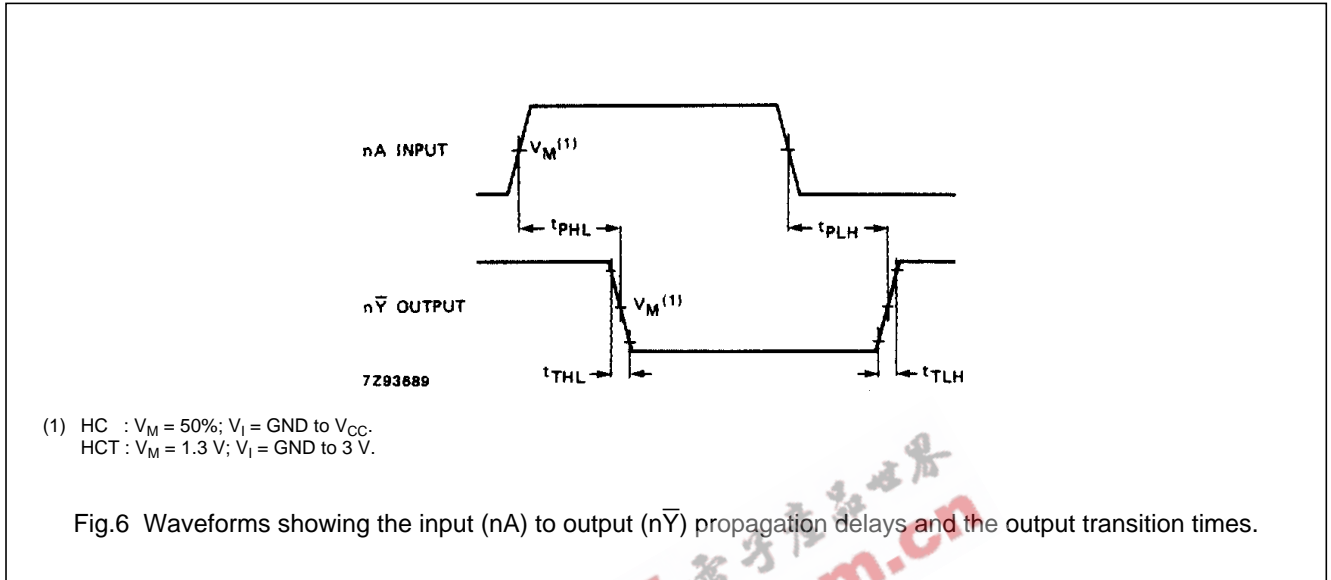
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to n $\overline{Y}$		13	24		30		36	ns	4.5	Fig.6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time n $\overline{OE}$ to n $\overline{Y}$		17	35		44		53	ns	4.5	Fig.7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time n $\overline{OE}$ to n $\overline{Y}$		20	35		44		53	ns	4.5	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.6

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".