74LVTH32245

3.3 V 32-bit bus transceiver; 3-state

Rev. 01 — 23 January 2008

Product data sheet

1. General description

The 74LVTH32245 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V. The 74LVTH32245 is a 32-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features four output enable ($n\overline{OE}$) inputs for easy cascading and four send/receive (nDIR) inputs for direction control. Pin $n\overline{OE}$ controls the outputs so that the buses are effectively isolated. Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features

- 32-bit bidirectional bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
 - ♦ JESD78 Class II level A exceeds 500 mA
- **ESD** protection:
 - ♦ HBM JESD22-A114E exceeds 2000 V
 - ♦ MM JESD22-A115-A exceeds 200 V

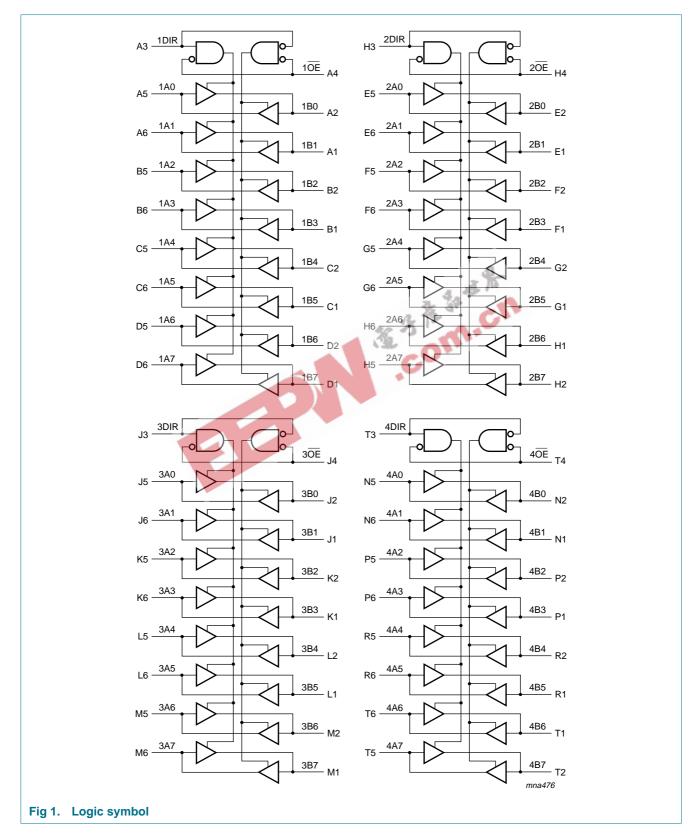
3. Ordering information

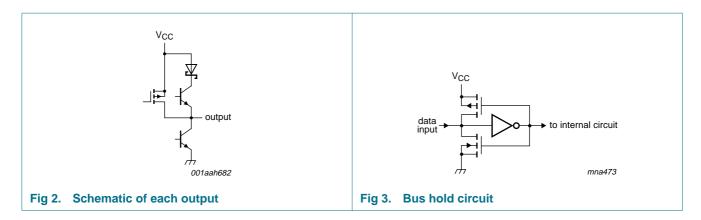
Table 1. Ordering information

Type number	Package						
	Temperature range	Name	Description	Version			
74LVTH32245EC	–40 °C to +85 °C	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body $13.5 \times 5.5 \times 1.05 \text{ mm}$	SOT536-1			



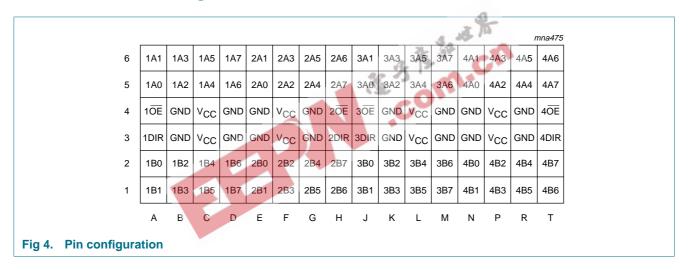
4. Functional diagram





5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Ball	Description
nDIR (n = 1 to 4)	A3, H3, J3, T3	direction control
$n\overline{OE}$ (n = 1 to 4)	A4, H4, J4, T4	output enable input (active LOW)
1A[0:7]	A5, A6, B5, B6, C5, C6, D5, D6	input or output
1B[0:7]	A2, A1, B2, B1, C2, C1, D2, D1	input or output
2A[0:7]	E5, E6, F5, F6, G5, G6, H6, H5	input or output
2B[0:7]	E2, E1, F2, F1, G2, G1, H1, H2	input or output
3A[0:7]	J5, J6, K5, K6, L5, L6, M5, M6	input or output
3B[0:7]	J2, J1, K2, K1, L2, L1, M2, M1	input or output
4A[0:7]	N5, N6, P5, P6, R5, R6, T6, T5	input or output

Pin description ... continued Table 2.

Symbol	Ball	Description
4B[0:7]	N2, N1, P2, P1, R2, R1, T1, T2	input or output
GND	B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, R4	ground (0 V)
V _{CC}	C3, C4, F3, F4, L3, L4, P3, P4	supply voltage

Functional description

Table 3. Function selection[1]

Input nOE nDIR		Input/output			
nOE	nDIR	nAn	nBn		
L	L	nAn = nBn	inputs		
L	Н	inputs	nBn = nAn		
Н	X	Z	Z		

 ^[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state
 7. Limiting values

Table 4. **Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)[1][2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
VI	input voltage		<u>[3]</u> −0.5	+7.0	V
Vo	output voltage	output in OFF or HIGH-state	<u>[3]</u> −0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	– 50	-	mA
I _{OK}	output clamping current	V _O < 0 V	–50	-	mA
I _O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		-	150	°C

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond indicated under Section 8 "Recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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Recommended operating conditions

Recommended operating conditions Table 5.

0	5	0		-		11
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_{I}	input voltage		0	-	5.5	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle \leq 50 %; $f \geq 1 \text{ kHz}$	-	-	64	mA
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V
P _{tot}	total power dissipation		<u>[1]</u> _	-	1000	mW

^[1] Above 70 $^{\circ}$ C the value of P_{tot} derates linearly with 1.8 mW/K.

Table 6. Static characteristics At recommended operating conditions; voltages are referenced to GND (ground = 0 V). Symbol Parameter Conditions Min Typ Max Unit $\Gamma_{amb} = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C}_{\boxed{1}}$									
Symbol	Parameter	Conditions	Min	Тур	Max	Unit			
T _{amb} = -	40 °C to +85 °C[1]								
V_{IK}	input clamping voltage	$V_{CC} = 2.7 \text{ V; } I_{IK} = -18 \text{ mA}$	-1.2	-0.85	-	V			
V_{IH}	HIGH-level input voltage		2.0	-	-	V			
V_{IL}	LOW-level input voltage		-	-	8.0	V			
V_{OH}	HIGH-level output voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V; } I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$	V_{CC}	-	V			
		$V_{CC} = 2.7 \text{ V}; I_{OH} = -8 \text{ mA}$	2.4	2.5	-	V			
		$V_{CC} = 3.0 \text{ V}; I_{OH} = -32 \text{ mA}$	2.0	2.3	-	V			
V _{OL}	LOW-level output voltage	$V_{CC} = 2.7 \text{ V}; I_{OL} = 100 \mu\text{A}$	-	0.07	0.2	V			
		$V_{CC} = 2.7 \text{ V}; I_{OL} = 24 \text{ mA}$	-	0.3	0.5	V			
		$V_{CC} = 3.0 \text{ V}; I_{OL} = 16 \text{ mA}$	-	0.25	0.4	V			
		$V_{CC} = 3.0 \text{ V}; I_{OL} = 32 \text{ mA}$	-	0.3	0.5	V			
		$V_{CC} = 3.0 \text{ V}; I_{OL} = 64 \text{ mA}$	-	0.4	0.55	V			
l _l	input leakage current	control pins							
		$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or GND}$	-	0.1	±1	μΑ			
		$V_{CC} = 0 \text{ V or } 3.6 \text{ V; } V_{I} = 5.5 \text{ V}$	-	0.1	10	μΑ			
		input/output data pins; V _{CC} = 3.6 V	[2]						
		V _I = 5.5 V	-	0.1	20	μΑ			
		$V_I = V_{CC}$	-	0.5	10	μΑ			
		V _I = 0 V	-5	-0.1	-	μΑ			
l _{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}$; $V_I \text{ or } V_O = 0 \text{ V to } 4.5 \text{ V}$	-	0.1	±100	μΑ			
I _{LO}	output leakage current	output HIGH; $V_O = 5.5 \text{ V}$; $V_{CC} = 3.0 \text{ V}$	-	75	125	μΑ			
I _{O(pu/pd)}	power-up/power-down output current	$V_{CC} \le 1.2 \text{ V}; V_O = 0.5 \text{ V to } V_{CC};$ $V_I = \text{GND or } V_{CC}; n\overline{OE} = \text{don't care}$	[4] -	40	±100	μΑ			

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

	, ,		,			
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I_{BHL}	bus hold LOW current	$V_{CC} = 3 \text{ V}; V_{I} = 0.8 \text{ V}$	75	135	-	μΑ
I _{BHH}	bus hold HIGH current	$V_{CC} = 3 \text{ V}; V_{I} = 2.0 \text{ V}$	-	-135	-75	μΑ
I _{BHLO}	bus hold LOW overdrive current	$V_{CC} = 0 \text{ V to } 3.6 \text{ V}; V_{I} = 3.6 \text{ V}$	[3] 500	-	-	μΑ
I _{внно}	bus hold HIGH overdrive current	$V_{CC} = 0 \text{ V to } 3.6 \text{ V}; V_{I} = 3.6 \text{ V}$	[3] _	-	-500	μΑ
I _{CC}	supply current	$V_{CC} = 3.6 \text{ V}$; $V_I = \text{GND or } V_{CC}$; $I_O = 0 \text{ A}$				
		outputs HIGH	-	0.14	0.24	mA
		outputs LOW	-	8.4	12	mA
		outputs disabled	<u>[5]</u> _	0.14	0.24	mA
Δl _{CC}	additional supply current	per input pin; V_{CC} = 3 V to 3.6 V; one input at V_{CC} – 0.6 V; other inputs at V_{CC} or GND	<u>[6]</u> -	0.1	0.2	mA
Cı	input capacitance	control pins; $V_O = 0 \text{ V or } 3.0 \text{ V}$	-4_	3	-	pF
C _{I/O}	input/output capacitance	input/output data pins; outputs disabled; V_{CC} = 3.6 V; I_{O} = 0 A; V_{I} = GND or V_{CC}	CN	9	-	pF

^[1] All typical values are at $V_{CC} = 3.3 \text{ V}$ and $T_{amb} = 25 ^{\circ}\text{C}$ unless otherwise specified.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for load circuit see <u>Figure 7</u>.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$T_{amb} = -4$	0 °C to +85 °C					
t _{PLH}	LOW to HIGH propagation delay	nAn to nBn or nBn to nAn; see Figure 5				
		$V_{CC} = 2.7 \text{ V}$	-	-	3.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	1.9	3.3	ns
t _{PHL}	HIGH to LOW propagation delay	nAn to nBn or nBn to nAn; see Figure 5				
		$V_{CC} = 2.7 \text{ V}$	-	-	3.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	1.7	3.3	ns
t_{PZH}	OFF-state to HIGH propagation	nOE to nAn or nBn; see Figure 6				
	delay	$V_{CC} = 2.7 \text{ V}$	-	-	5.3	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.8	4.5	ns

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^[2] Unused pins at V_{CC} or GND.

^[3] This is the bus-hold overdrive current required to force the input to the opposite logic state.

This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V \pm 0.3 V a transition time of 100 μ s is permitted. This parameter is valid for T_{amb} = 25 °C only.

^[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

^[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

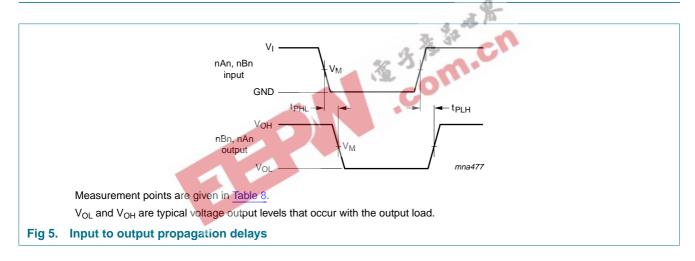
 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for load circuit see Figure 7.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{PZL}	OFF-state to LOW propagation	nOE to nAn or nBn; see Figure 6				
	delay	$V_{CC} = 2.7 \text{ V}$	-	-	5.1	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.8	4.1	ns
t _{PHZ}	HIGH to OFF-state propagation delay	nOE to nAn or nBn; see Figure 6				
		$V_{CC} = 2.7 \text{ V}$	-	-	5.7	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	3.2	5.1	ns
t_{PLZ}	LOW to OFF-state propagation delay	nOE to nAn or nBn; see Figure 6				
		$V_{CC} = 2.7 \text{ V}$	-	-	4.6	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	3.0	4.6	ns

^[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Waveforms



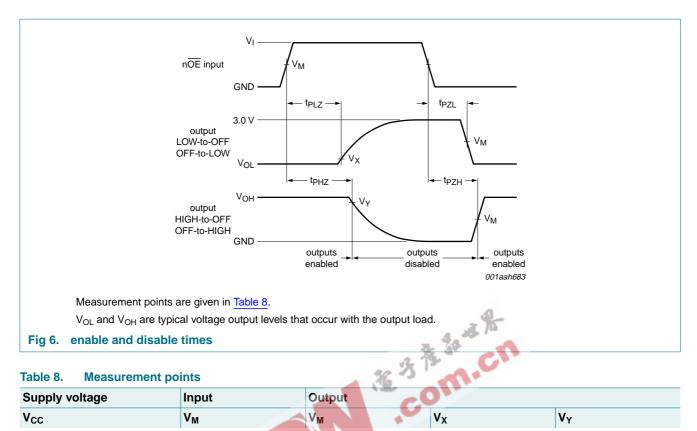


Table 8. **Measurement points**

Supply voltage	Input	Output		
V _{CC}	V _M	V _M	V_X	V _Y
2.7 V to 3.6 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} – 0.3 V

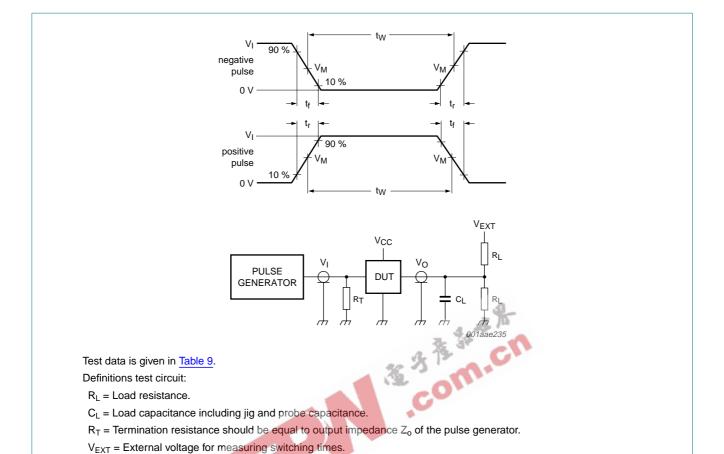


Fig 7. Load circuitry for switching times

Test data

Table 9.

Input			Load			V _{EXT}		
V _I	f _i	t _W	t _r , t _f	R _L	CL	t _{PHZ} , t _{PZH}	t _{PLZ} , t _{PZL}	t _{PLH} , t _{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500Ω	50 pF	GND	6 V	open

12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1

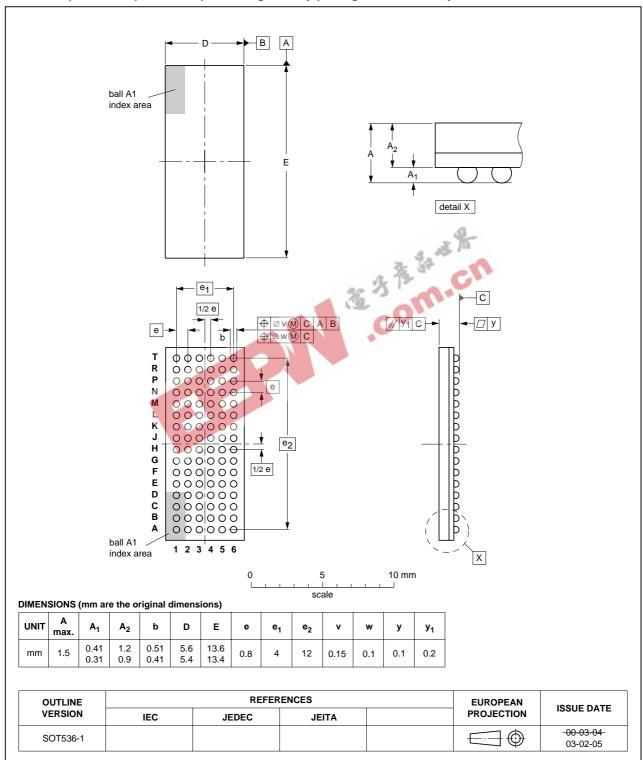


Fig 8. Package outline SOT536-1 (LFBGA96)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

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Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVTH32245_1	20080123	Product data sheet		-
			om.cn	



15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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