

74VCX16500

Low Voltage 18-Bit Universal Bus Transceivers with 3.6V Tolerant Inputs and Outputs

General Description

The VCX16500 is an 18-bit universal bus transceiver which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of CLKAB. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in a high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active HIGH and OEBA is active LOW).

The VCX16500 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The 74VCX16500 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD} (A to B, B to A)
 - 2.9 ns max for 3.0V to 3.6V V_{CC}
 - 3.5 ns max for 2.3V to 2.7V V_{CC}
 - 7.0 ns max for 1.65V to 1.95V V_{CC}
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
 - ±24 mA @ 3.0V V_{CC}
 - ±18 mA @ 2.3V V_{CC}
 - ±6 mA @ 1.65V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model >200V

Note 1: To ensure the high-impedance state during power up or power down, OEBA should be tied to V_{CC} through a pull-up resistor and OEAB should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

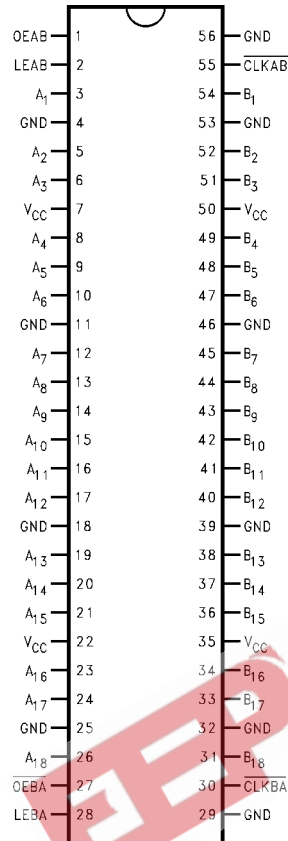
Ordering Code:

Order Number	Package Number	Package Description
74VCX16500MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

74VCX16500 Low Voltage 18-Bit Universal Bus Transceivers with 3.6V Tolerant Inputs and Outputs

Connection Diagram



Pin Descriptions

Pin Names	Description
OEAB	Output Enable Input for A to B Direction (Active HIGH)
$\overline{\text{OEBA}}$	Output Enable Input for B to A Direction (Active LOW)
LEAB, LEBA	Latch Enable Inputs
$\overline{\text{CLKAB}}$, CLKBA	Clock Inputs
A ₁ –A ₁₈	Side A Inputs or 3-STATE Outputs
B ₁ –B ₁₈	Side B Inputs or 3-STATE Outputs

Function Table (Note 2)

Inputs				Outputs
OEAB	LEAB	CLKAB	A _n	B _n
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B ₀ (Note 3)
H	L	L	X	B ₀ (Note 4)

H = HIGH Voltage Level

L = LOW Voltage Level

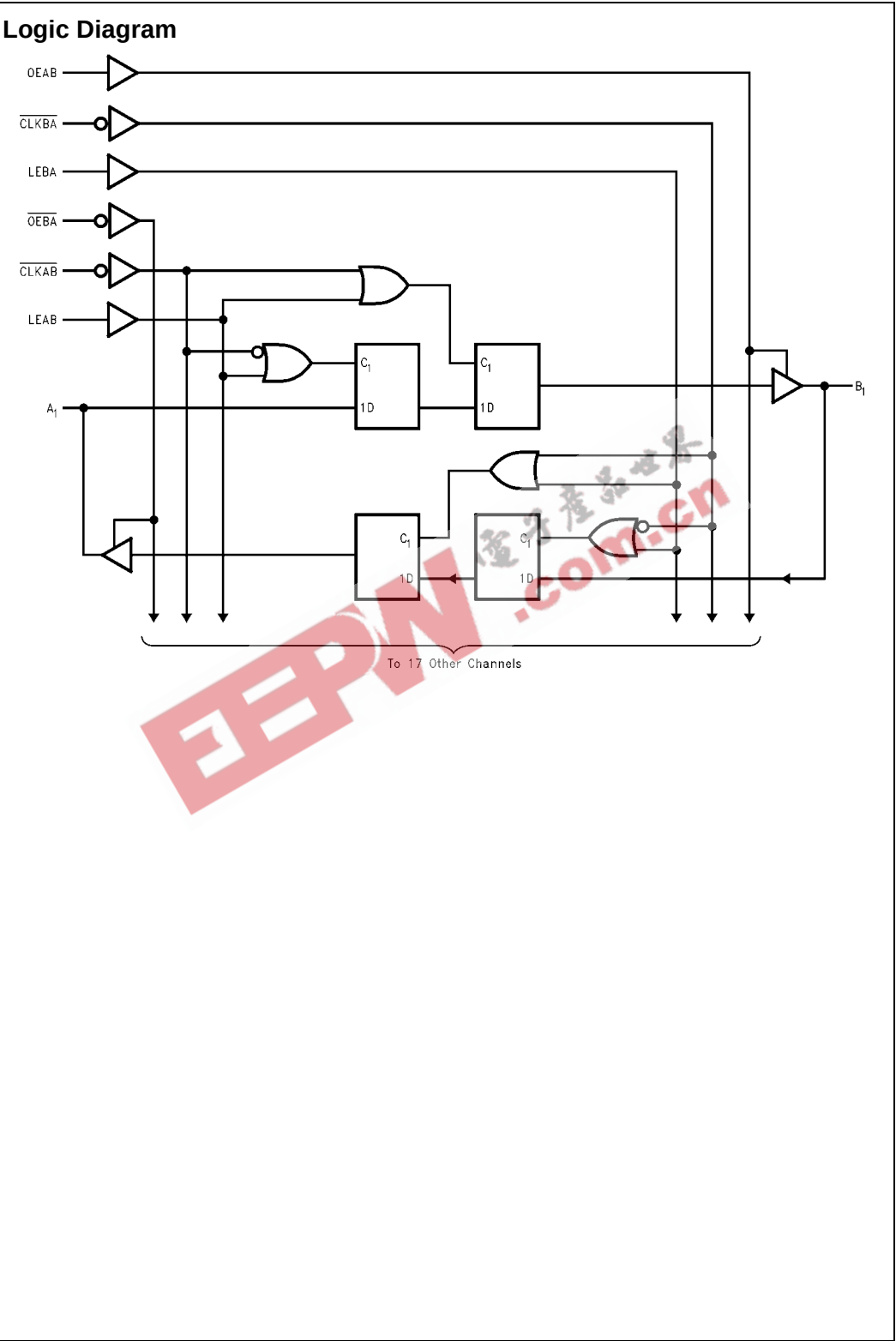
X = Immaterial (HIGH or LOW, inputs may not float)

Z = High Impedance

Note 2: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA and CLKBA. OEBA is active LOW.

Note 3: Output level before the indicated steady-state input conditions were established.

Note 4: Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.



Absolute Maximum Ratings (Note 5)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATE	-0.5V to +4.6V
Outputs Active (Note 6)	-0.5 to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or Ground Current per	
Supply Pin (I_{CC} or Ground)	± 100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 7)

Power Supply	
Operating	1.65V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	-0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
$V_{CC} = 3.0V$ to 3.6V	± 24 mA
$V_{CC} = 2.3V$ to 2.7V	± 18 mA
$V_{CC} = 1.65V$ to 2.3V	± 6 mA
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 5: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: Floating or unused pin (inputs or I/O's) must be held HIGH or LOW.

DC Electrical Characteristics (2.7V < V_{CC} ≤ 3.6V)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7-3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7-3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$	2.7-3.6 2.7 3.0 3.0	$V_{CC} - 0.2$ 2.2 2.4 2.2		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 18 \text{ mA}$ $I_{OL} = 24 \text{ mA}$	2.7-3.6 2.7 3.0 3.0		0.2 0.4 0.4 0.55	V
I_I	Input Leakage Current	$0V \leq V_I \leq 3.6V$	2.7-3.6		± 5.0	μA
I_{OZ}	3-STATE Output Leakage	$0V \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or V_{IL}	2.7-3.6		± 10	μA
I_{OFF}	Power Off Leakage Current	$0V \leq (V_I, V_O) \leq 3.6V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND $V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 8)	2.7-3.6 2.7-3.6		20 ± 20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7-3.6		750	μA

Note 8: Outputs disabled or 3-STATE only.

DC Electrical Characteristics (2.3V ≤ V _{CC} ≤ 2.7V)						
Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		2.3–2.7	1.6		V
V _{IL}	LOW Level Input Voltage		2.3–2.7		0.7	V
V _{OH}	HIGH Level Output Voltage	I _{OH} = –100 μA I _{OH} = –6 mA I _{OH} = –12 mA I _{OH} = –18 mA	2.3–2.7 2.3 2.3 2.3	V _{CC} – 0.2 2.0 1.8 1.7		V
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA I _{OL} = 12 mA I _{OL} = 18 mA	2.3–2.7 2.3 2.3		0.2 0.4 0.6	V
I _I	Input Leakage Current	0 ≤ V _I ≤ 3.6V	2.3–2.7		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	2.3–2.7		±10	μA
I _{OFF}	Power Off Leakage Current	0 ≤ (V _I , V _O) ≤ 3.6V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND V _{CC} ≤ (V _I , V _O) ≤ 3.6V (Note 9)	2.3–2.7 2.3–2.7		20 ±20	μA
Note 9: Outputs disabled or 3-STATE only.						
DC Electrical Characteristics (1.65V ≤ V _{CC} < 2.3V)						
Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		1.65 - 2.3	0.65 × V _{CC}		V
V _{IL}	LOW Level Input Voltage		1.65 - 2.3		0.35 × V _{CC}	V
V _{OH}	HIGH Level Output Voltage	I _{OH} = –100 μA I _{OH} = –6 mA	1.65 - 2.3 1.65	V _{CC} – 0.2 1.25		V
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA I _{OL} = 6 mA	1.65 - 2.3 1.65		0.2 0.3	V
I _I	Input Leakage Current	0 ≤ V _I ≤ 3.6V	1.65 - 2.3		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	1.65 - 2.3		±10	μA
I _{OFF}	Power Off Leakage Current	0 ≤ (V _I , V _O) ≤ 3.6V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND V _{CC} ≤ (V _I , V _O) ≤ 3.6V (Note 10)	1.65 - 2.3 1.65 - 2.3		20 ±20	μA
Note 10: Outputs disabled or 3-STATE only.						

AC Electrical Characteristics (Note 11)

Symbol	Parameter	T _A = -40°C to +85°C, C _L = 30 pF, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.5 ± 0.2V		V _{CC} = 1.8 ± 0.15V		
		Min	Max	Min	Max	Min	Max	
t _{MAX}	Maximum Clock Frequency	250		200		100		MHz
t _{PHL}	Propagation Delay							
t _{PLH}	Bus to Bus	0.6	2.9	0.8	3.5	1.5	7.0	ns
t _{PHL}	Propagation Delay							
t _{PLH}	Clock to Bus	0.6	4.2	0.8	5.3	1.5	9.8	ns
t _{PHL}	Propagation Delay							
t _{PLH}	LE to Bus	0.6	3.8	0.8	4.9	1.5	9.8	ns
t _{PZL}	Output Enable Time							
t _{PZH}		0.6	3.8	0.8	4.9	1.5	9.8	ns
t _{PLZ}	Output Disable Time							
t _{PHZ}		0.6	3.7	0.8	4.2	1.5	7.6	ns
t _S	Setup Time	1.5		1.5		2.5		ns
t _H	Hold Time	1.0		1.0		1.0		ns
t _W	Pulse Width	1.5		1.5		4.0		ns
t _{OSHL}	Output to Output							
t _{OSLH}	Skew (Note 12)		0.5		0.5		0.75	ns

Note 11: For $C_L = 50\text{pF}$, add approximately 300ps to the AC maximum specification.

Note 12: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25^{\circ}\text{C}$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8 2.5 3.3	0.25 0.6 0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8 2.5 3.3	-0.25 -0.6 -0.8	V
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8 2.5 3.3	1.5 1.9 2.2	V

Capacitance

Symbol	Parameter	Conditions	$T_A = +25^{\circ}\text{C}$	Units
C_{IN}	Input Capacitance	$V_I = 0V$ or V_{CC} $V_{CC} = 1.8V, 2.5V, \text{ or } 3.3V,$	6	pF
$C_{I/O}$	Output Capacitance	$V_I = 0V$, or V_{CC} ; $V_{CC} = 1.8V, 2.5V \text{ or } 3.3V$	7	pF
C_{PD}	Power Dissipation Capacitance	$V_I = 0V$ or V_{CC} , $f = 10 \text{ MHz}$ $V_{CC} = 1.8V, 2.5V \text{ or } 3.3V$	20	pF

AC Loading and Waveforms

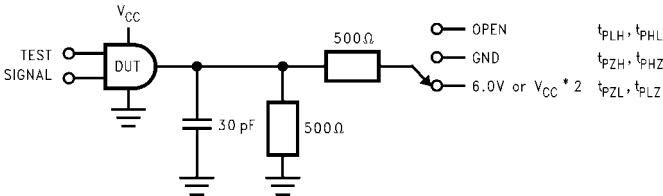


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V; 1.8 \pm 0.15V$
t_{PZH}, t_{PHZ}	GND

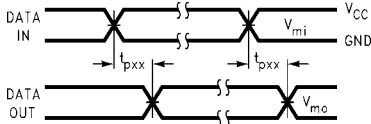


FIGURE 2. Waveform for Inverting and Non-inverting Functions

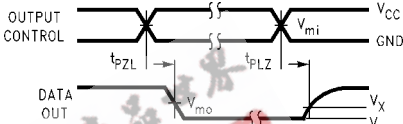


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

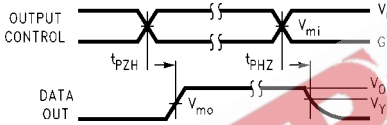


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

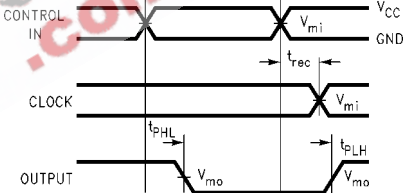


FIGURE 5. Propagation Delay, Pulse Width and t_{rec} Waveforms

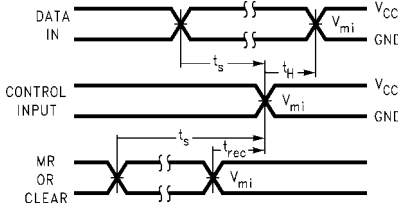


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8 \pm 0.15V$
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

The drawing shows a 28-pin DIP package. The top view (left) indicates a width of 14.0 ± 0.1 mm and a body width of 6.1 ± 0.1 mm. Pin 1 is at the bottom left. Dimensions for the lead height are 8.1 mm and 4.05 mm. The side view (right) shows a total height of 9.2 mm (typical) and a body height of 5.6 mm (typical). Symmetry lines (SYMM) are shown for both views. A detail box for the lead profile shows dimensions 0.2 , 0.3 , and 0.5 mm, with a note "ALL LEAD TIPS".

Technical drawing of a lead wire assembly, showing side and end views with dimensions and callouts.

Side View Dimensions:

- Lead tip diameter: $\triangle 0.1 \text{ C}$
- Lead tip length: ALL LEAD TIPS
- Lead wire diameter: $\phi 0.13 \text{ (M) A B (S) C (S)}$
- Lead wire length: $0.17 - 0.27 \text{ TYP}$
- Lead wire diameter tolerance: $\pm 0.10 \pm 0.05 \text{ TYP}$
- Lead wire diameter tolerance: $0.09 - 0.20 \text{ TYP}$
- Lead wire diameter tolerance: $0.10 \pm 0.05 \text{ TYP}$
- Lead wire diameter tolerance: $1.1' \text{ MAX}$
- Lead wire diameter tolerance: (0.90)
- Lead wire diameter tolerance: 0.5 TYP
- Lead wire diameter tolerance: $-C-$

End View Dimensions:

- Lead tip diameter: $\triangle 0.1 \text{ C}$
- Lead tip length: ALL LEAD TIPS
- Lead wire diameter: $\phi 0.13 \text{ (M) A B (S) C (S)}$
- Lead wire length: $0.17 - 0.27 \text{ TYP}$
- Lead wire diameter tolerance: $\pm 0.10 \pm 0.05 \text{ TYP}$
- Lead wire diameter tolerance: $0.09 - 0.20 \text{ TYP}$
- Lead wire diameter tolerance: $0.10 \pm 0.05 \text{ TYP}$
- Lead wire diameter tolerance: $1.1' \text{ MAX}$
- Lead wire diameter tolerance: (0.90)
- Lead wire diameter tolerance: 0.5 TYP
- Lead wire diameter tolerance: $-C-$

Callouts:

- SEE DETAIL A
- GAGE PLANE
- SEATING PLANE
- 0.25
- $0.60^{+0.15}_{-0.10}$
- $0^\circ - 8^\circ$

**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56**

LIFE SUPPORT POLICY

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

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