



74LVX16245

16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS, 5V TOLERANT INPUTS

- HIGH SPEED: $t_{PD} = 5.3 \text{ ns}$ (TYP.) at $V_{CC} = 3V$
- 5V TOLERANT INPUT
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- INPUT VOLTAGE LEVEL: $V_{IL} = 0.8$, $V_{IH} = 2V$ AT $V_{CC} = 3V$
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(\text{OPR}) = 2V$ to $3.6V$ (1.2V Data Retention)
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: $V_{OLP} = 0.3V$ (TYP.) AT $V_{CC} = 3V$

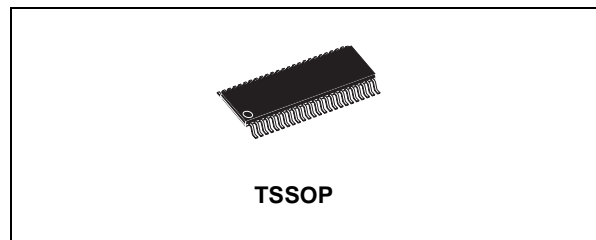
DESCRIPTION

The 74LVX16245 is an advanced high-speed CMOS 16-BIT BUS TRANSCEIVER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

This IC is intended for two-way asynchronous communication between data busses; the direction of data transmission is determined by DIR input. The enable input \overline{G} can be used to disable the device so that the busses are effectively isolated.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

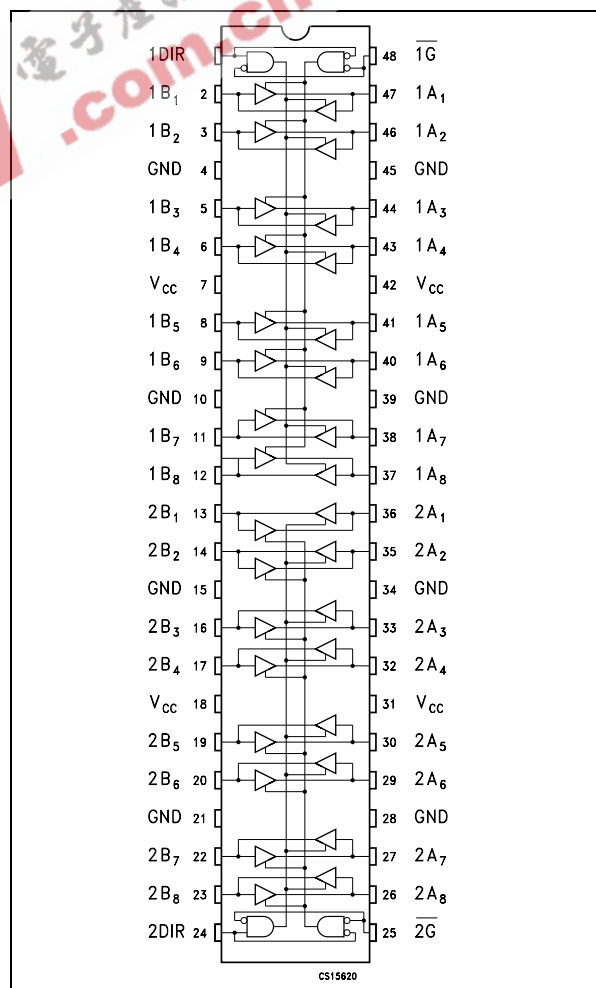
All floating bus terminals during High Z State must be held HIGH or LOW.



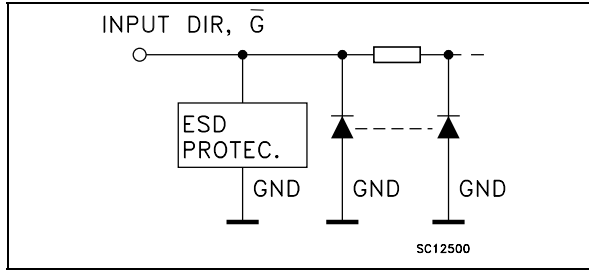
ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74LVX16245TTR

PIN CONNECTION



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

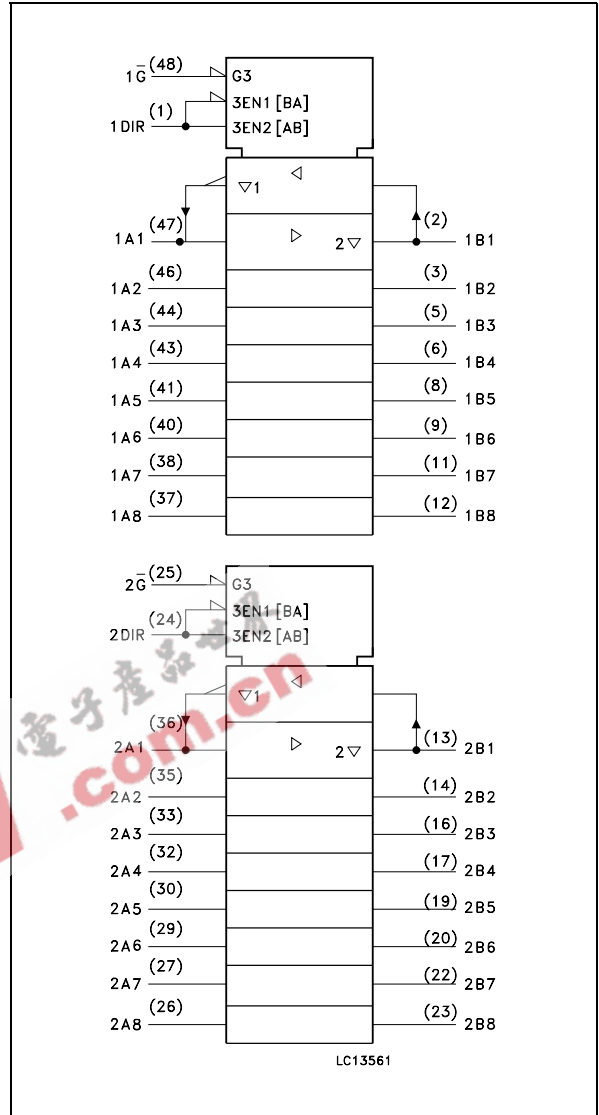
PIN No	SYMBOL	NAME AND FUNCTION
1	1DIR	Directional Control
2, 3, 5, 6, 8, 9, 11, 12	1B1 to 1B8	Data Inputs/Outputs
13, 14, 16, 17, 19, 20, 22, 23	2B1 to 2B8	Data Inputs/Outputs
24	2DIR	Directional Control
25	2G	Output Enable Input
36, 35, 33, 32, 30, 29, 27, 26	2A1 to 2A8	Data Inputs/Outputs
47, 46, 44, 43, 41, 40, 38, 38	1A1 to 1A8	Data Inputs/Outputs
48	1G	Output Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS		FUNCTION		OUTPUT
G-bar	DIR	A BUS	B BUS	Y _n
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	Z	Z	Z

X : Don't Care
Z : High Impedance

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage (DIR, G)	-0.5 to +7.0	V
$V_{I/O}$	Bus I/O Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 75	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage (DIR, G)	0 to 5.5	V
$V_{I/O}$	Bus I/O Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2) ($V_{CC} = 3.0$)	0 to 100	ns/V

1) Truth Table guaranteed: 1.2 to 3.6V

1) V_{IN} from 0.8 to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0		2.0			2.0		2.0		
		3.6		2.4			2.4		2.4		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0				0.8		0.8		0.8	
		3.6				0.8		0.8		0.8	
V _{OH}	High Level Output Voltage	2.0	I _O =-50 μA	1.9	2.0		1.9		1.9		V
		3.0	I _O =-50 μA	2.9	3.0		2.9		2.9		
		3.0	I _O =-4 mA	2.58	4.5		2.48		2.4		
V _{OL}	Low Level Output Voltage	2.0	I _O =50 μA		0.0	0.1		0.1			V
		3.0	I _O =50 μA		0.0	0.1		0.1			
		3.0	I _O =4 mA			0.36		0.44		0.55	
I _{oz}	High Impedance Output Leakage Current	5.5	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.25		±2.5		±2.5	μA
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			±0.1		±1		±1	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40		40	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)	C _L (pF)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation Delay Time	2.7	15		5.7	9.0	1.0	10.5	1.0	10.5	ns
		2.7	50		8.0	12.3	1.0	14.0	1.0	14.0	
		3.3 ^(*)	15		5.3	8.4	1.0	10.0	1.0	10.0	
		3.3 ^(*)	50		7.8	11.9	1.0	13.5	1.0	13.5	
t _{PZL} t _{PZH}	Output Disable Time	2.7	15	R _L = 1KΩ	7.0	11.0	1.0	13.5	1.0	13.5	ns
		2.7	50	R _L = 1KΩ	9.6	15.1	1.0	16.5	1.0	16.5	
		3.3 ^(*)	15	R _L = 1KΩ	6.6	10.6	1.0	12.5	1.0	12.5	
		3.3 ^(*)	50	R _L = 1KΩ	9.1	14.1	1.0	16.0	1.0	16.0	
t _{PLZ} t _{PHZ}	Output Enable Time	2.7	50	R _L = 1KΩ	10.8	15.0	1.0	16.5	1.0	16.5	ns
		3.3 ^(*)	50	R _L = 1KΩ	10.3	14.0	1.0	16.0	1.0	16.0	
t _{OSLH} t _{OSHL}	Output to Output Skew time (note 1)	3.3 ^(*)	50			1.5		1.5		1.5	ns
		3.3 ^(*)	50			1.0		1.0		1.0	

(*) Voltage range is 3.3V ± 0.3V

Note 1: Parameter guaranteed by design. t_{soLH} = |t_{PLHm} - t_{PLHn}|, t_{soHL} = |t_{PHLm} - t_{PHLn}|

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
				T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance		4	10		10		10	pF		
C _{I/O}	Output Capacitance		8						pF		
C _{PD}	Power Dissipation Capacitance (note 1)		21						pF		

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per circuit)

DYNAMIC SWITCHING CHARACTERISTICS

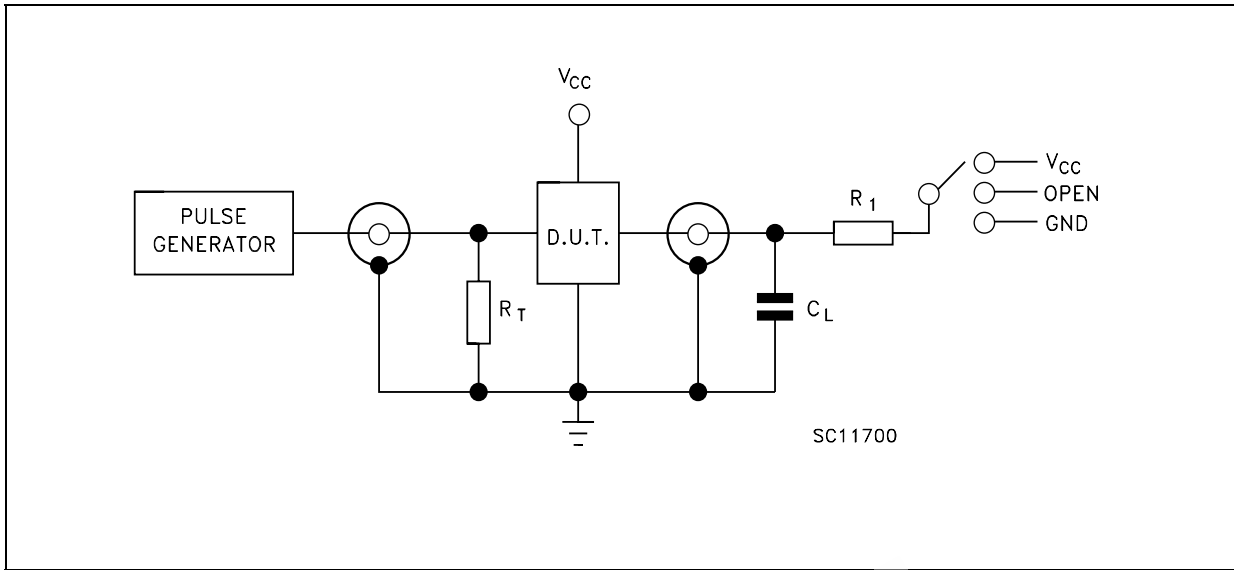
Symbol	Parameter	Test Condition		Value						Unit		
				V _{CC} (V)	T _A = 25°C			-40 to 85°C			-55 to 125°C	
					Min.	Typ.	Max.	Min.	Max.		Min.	Max.
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C _L = 50 pF		0.3	0.8					V	
V _{OLV}				-0.8	-0.3							
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3		2.0						V		
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					V	

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

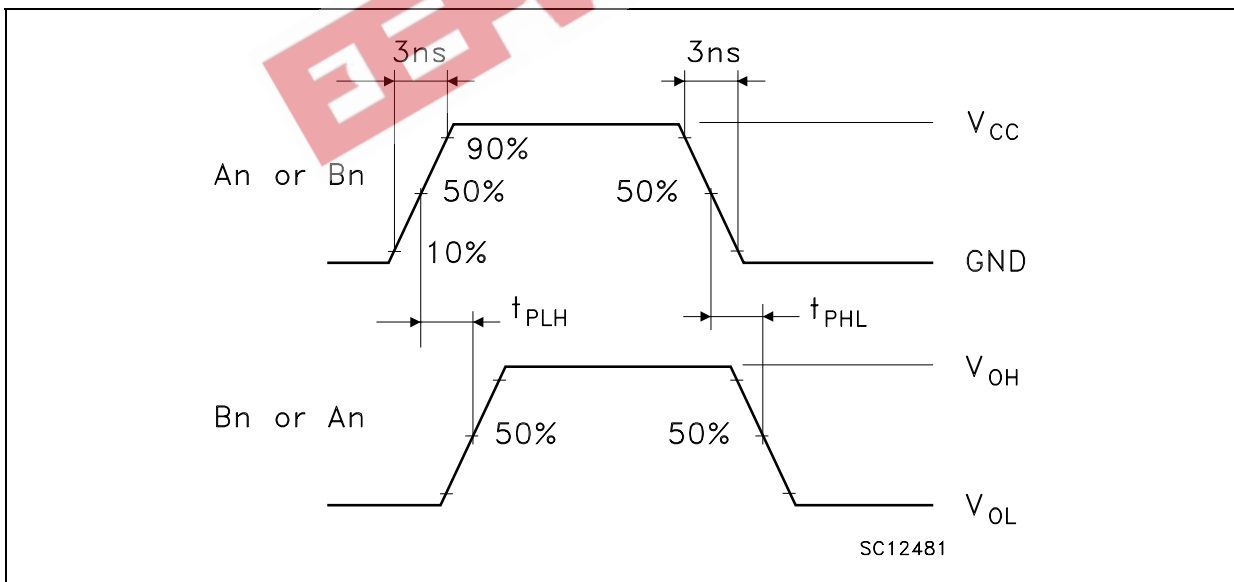
TEST CIRCUIT



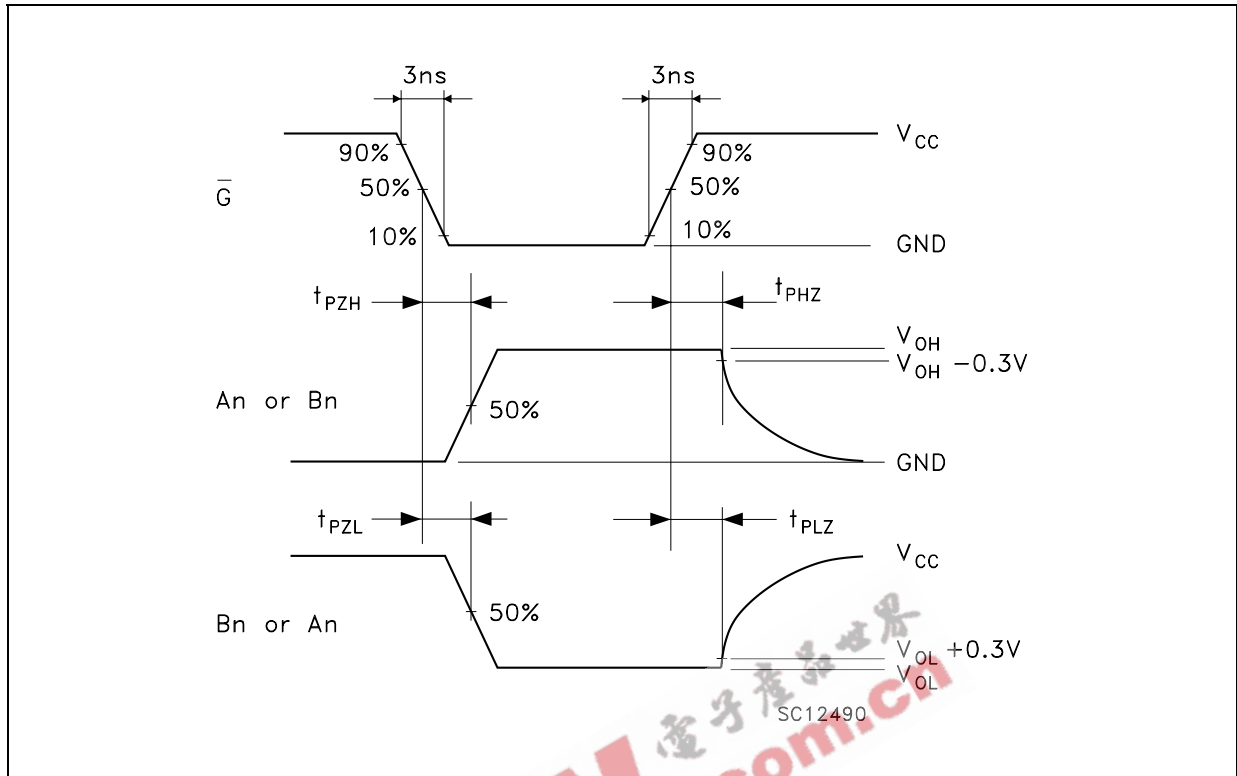
TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	V_{CC}
t_{PZH} , t_{PHZ}	GND

$C_L = 15/50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = R_1 = 1\text{K}\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)

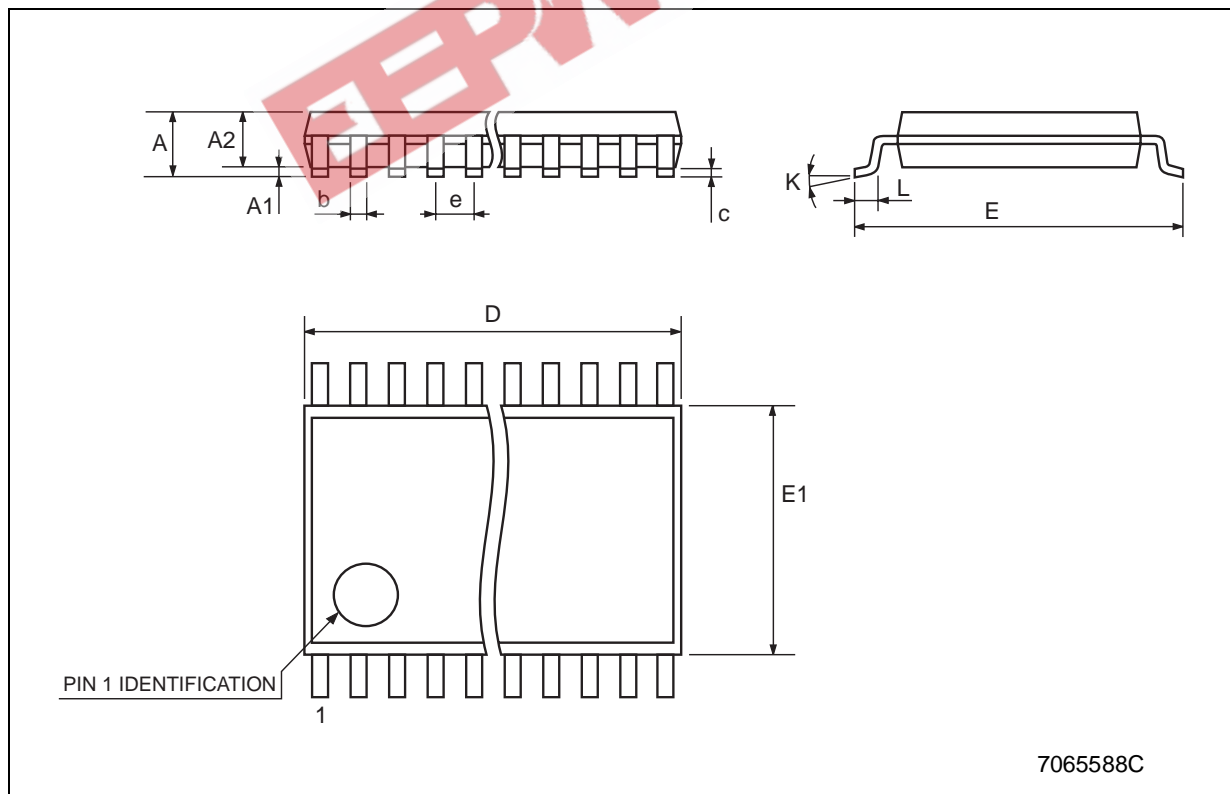


WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



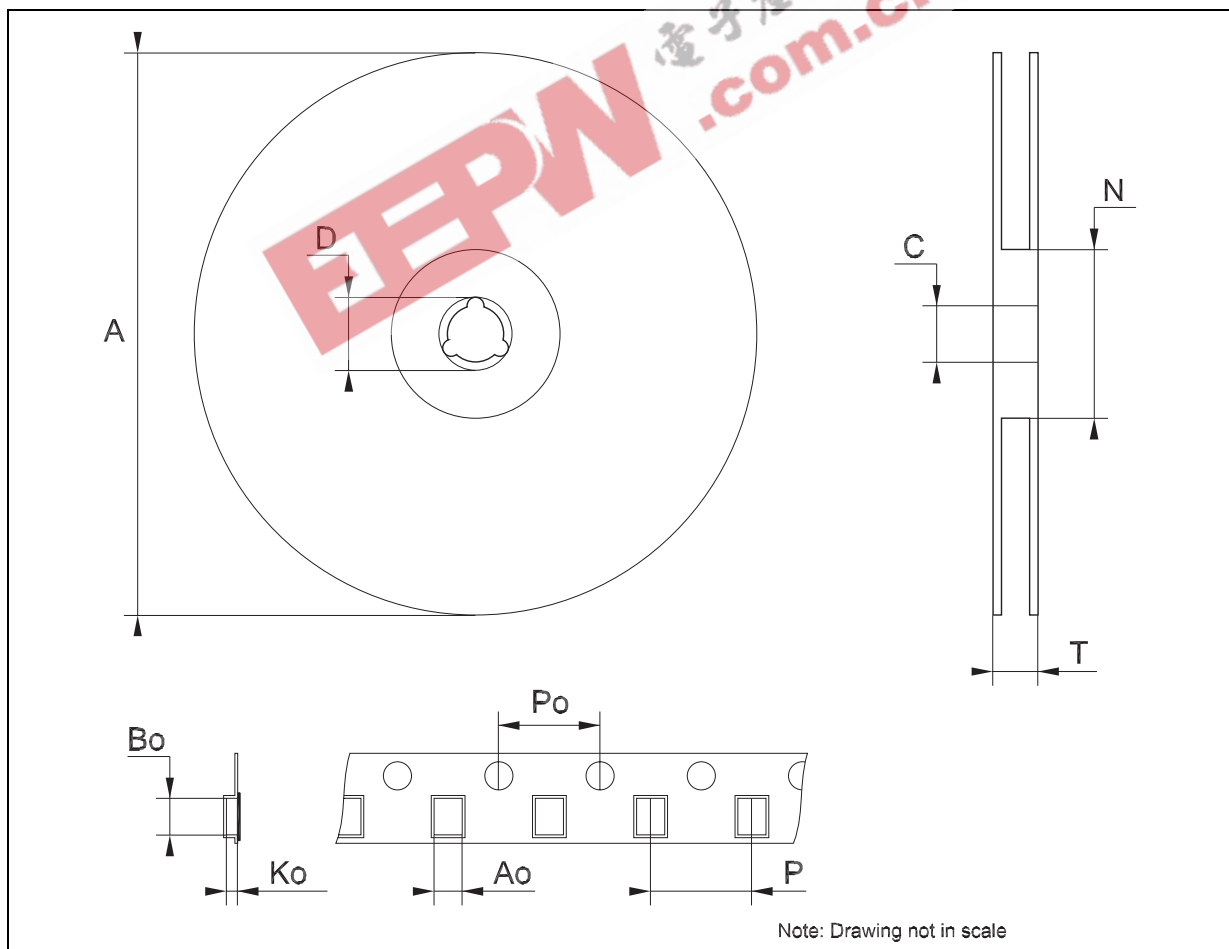
TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



Tape & Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



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