

# 74ABT544

Octal latched transceiver with dual enable; inverting; 3-state

Rev. 03 — 20 April 2005

Product data sheet

## 1. General description

The 74ABT544 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT544 octal latched transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable ( $\overline{LEAB}$  and  $\overline{LEBA}$ ) and output enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64 mA.

The 74ABT544 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B enable ( $\overline{EAB}$ ) input and the A-to-B latch enable ( $\overline{LEAB}$ ) input are LOW, the A-to-B path is transparent. A subsequent LOW-to-HIGH transition of the  $\overline{LEAB}$  signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With  $\overline{EAB}$  and  $\overline{OEAB}$  both LOW, the 3-state B output buffers are active and invert the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the  $\overline{EBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$  inputs.

## 2. Features

- Combines 74ABT640 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64 mA and -32 mA
- Live insertion and extraction permitted
- Power-up 3-state
- Power-up reset
- Latch-up protection:
  - ◆ JESD78: exceeds 500 mA
- ESD protection:
  - ◆ MIL STD 883 method 3015: exceeds 2000 V
  - ◆ Machine model: exceeds 200 V

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### 3. Quick reference data

**Table 1: Quick reference data**

$T_{amb} = 25\text{ }^\circ\text{C}$ ;  $GND = 0\text{ V}$ .

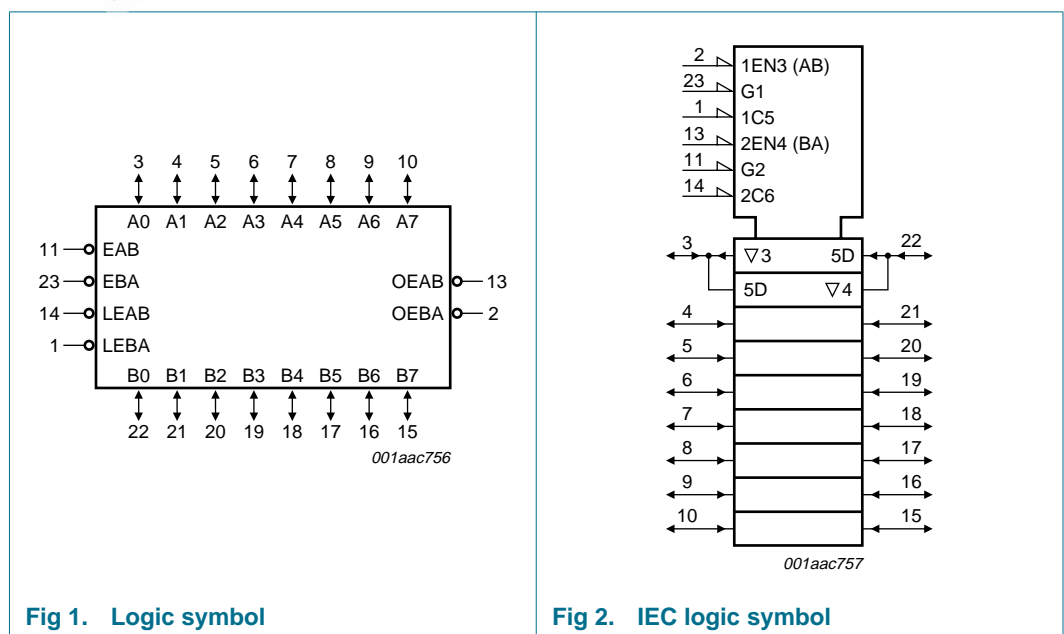
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PLH}$	propagation delay An to Bn or Bn to An	$C_L = 50\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-	3.0	-	ns
$t_{PHL}$	propagation delay An to Bn or Bn to An	$C_L = 50\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-	3.6	-	ns
$C_I$	input capacitance	$V_I = 0\text{ V}$ or $V_{CC}$	-	4	-	pF
$C_{I/O}$	I/O capacitance	outputs disabled; $V_O = 0\text{ V}$ or $V_{CC}$	-	7	-	pF
$I_{CC}$	quiescent supply current	outputs 3-state; $V_{CC} = 5.5\text{ V}$	-	110	-	$\mu\text{A}$

### 4. Ordering information

**Table 2: Ordering information**

Type number	Package			Version
	Temperature range	Name	Description	
74ABT544D	-40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74ABT544N	-40 °C to +85 °C	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222-1
74ABT544DB	-40 °C to +85 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74ABT544PW	-40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

### 5. Functional diagram



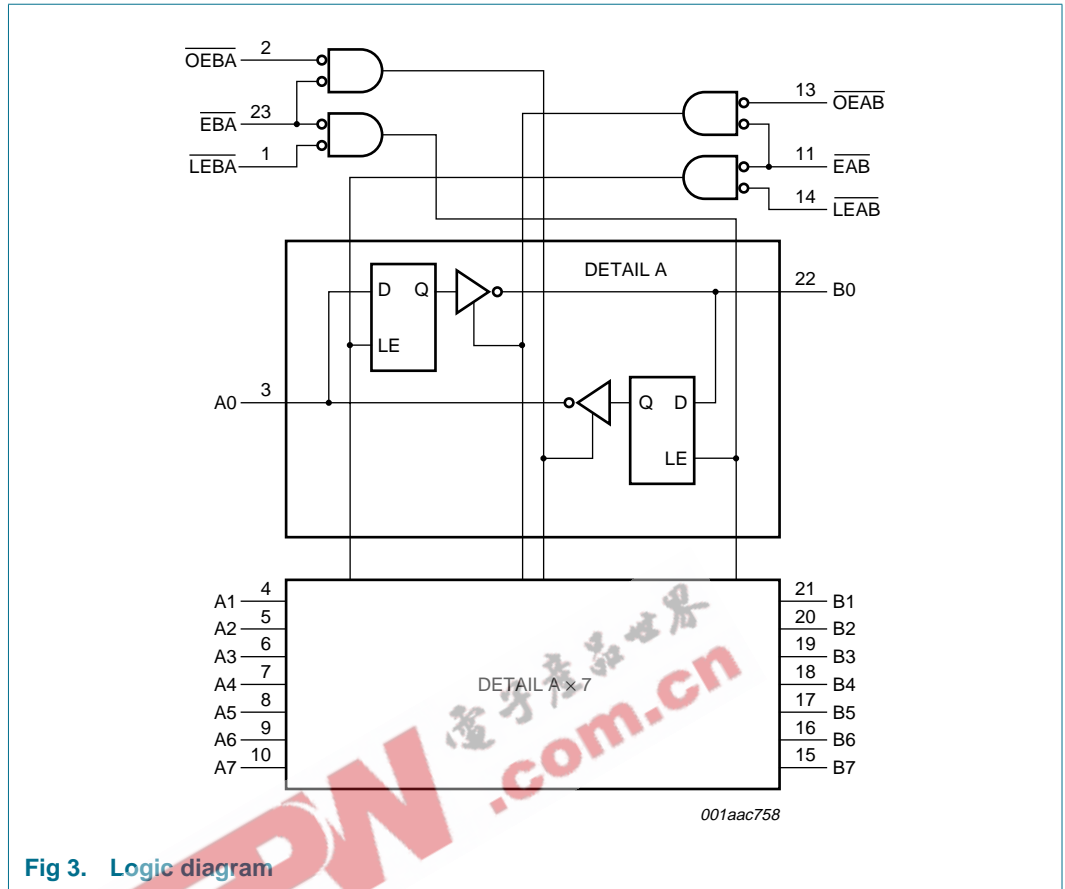


Fig 3. Logic diagram

## 6. Pinning information

### 6.1 Pinning

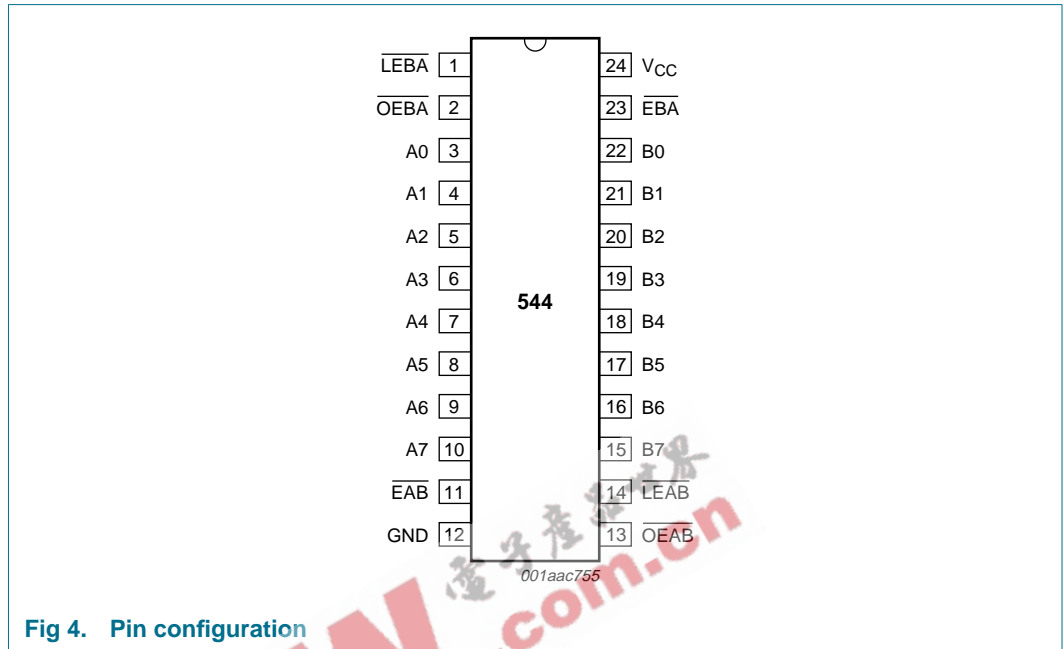


Fig 4. Pin configuration

### 6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
$\overline{\text{LEBA}}$	1	B-to-A latch enable input (active LOW)
$\overline{\text{OEBA}}$	2	B-to-A output enable input (active LOW)
A0	3	port A, 3-state output 0
A1	4	port A, 3-state output 1
A2	5	port A, 3-state output 2
A3	6	port A, 3-state output 3
A4	7	port A, 3-state output 4
A5	8	port A, 3-state output 5
A6	9	port A, 3-state output 6
A7	10	port A, 3-state output 7
$\overline{\text{EAB}}$	11	A-to-B enable input (active LOW)
GND	12	ground (0 V)
$\overline{\text{OEAB}}$	13	A-to-B output enable input (active LOW)
$\overline{\text{LEAB}}$	14	A-to-B latch enable input (active LOW)
B7	15	port B, 3-state output 7
B6	16	port B, 3-state output 6
B5	17	port B, 3-state output 5
B4	18	port B, 3-state output 4

Table 3: Pin description ...continued

Symbol	Pin	Description
B3	19	port B, 3-state output 3
B2	20	port B, 3-state output 2
B1	21	port B, 3-state output 1
B0	22	port B, 3-state output 0
$\overline{\text{EBA}}$	23	B-to-A enable input (active LOW)
$V_{\text{CC}}$	24	supply voltage

## 7. Functional description

### 7.1 Function table

Table 4: Function table [1]

Status	Control			Input	Output
	$\text{OE}_{\text{xx}}$	$\overline{\text{E}}_{\text{xx}}$	$\overline{\text{LE}}_{\text{xx}}$	An or Bn	An or Bn
Disabled	H	X	X	X	Z
	X	H	X	X	Z
Disabled + latch	L	$\uparrow$	L	h	Z
				I	Z
Latch + display	L	L	$\uparrow$	h	L
				I	H
Transparent	L	L	L	H	L
				L	H
Hold	L	L	H	X	NC

- [1] H = HIGH voltage level;  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
L = LOW voltage level;  
I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
X = don't care;  
 $\uparrow$  = LOW-to-HIGH clock transition;  
NC = no change;  
Z = high-impedance OFF-state.

## 8. Limiting values

**Table 5: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		[1] -1.2	+7.0	V
$V_O$	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+5.5	V
$I_{IK}$	input diode current	$V_I < 0$ V	-	-18	mA
$I_{OK}$	output diode current	$V_O < 0$ V	-	-50	mA
$I_O$	output current	output in LOW-state	-	128	mA
$T_j$	junction temperature		[2] -	150	°C
$T_{stg}$	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 9. Recommended operating conditions

**Table 6: Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level Input voltage		-	-	0.8	V
$I_{OH}$	HIGH-level output current		-	-	-32	mA
$I_{OL}$	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise or fall rate		0	-	10	ns/V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C

## 10. Static characteristics

**Table 7: Static characteristics**
*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>T<sub>amb</sub> = 25 °C</b>							
V <sub>IK</sub>	input diode voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-	-0.9	-1.2	V	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>					
		I <sub>OH</sub> = -3 mA	2.5	3.2	-	V	
		I <sub>OH</sub> = -32 mA	2.0	2.3	-	V	
		V <sub>CC</sub> = 5.0 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>					
	I <sub>OH</sub> = -3 mA	3.0	3.7	-	V		
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 4.5 V; I <sub>OL</sub> = 64 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	-	0.42	0.55	V	
V <sub>RST</sub>	restart LOW-level output voltage	V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 1 mA; V <sub>I</sub> = GND or V <sub>CC</sub>	[1]	-	0.13	0.55 V	
I <sub>LI</sub>	input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V					
			control pins	-	±0.01	±1.0	µA
			data pins	-	±5	±100	µA
I <sub>OFF</sub>	power-down leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V	-	±5.0	±100	µA	
I <sub>PU</sub> , I <sub>PD</sub>	power-up or power-down 3-state output current	V <sub>CC</sub> = 2.1 V; V <sub>O</sub> = 0.5 V; V <sub>I</sub> = GND or V <sub>CC</sub> ; V <sub>OExx</sub> = don't care	[2]	-	±5.0	±50 µA	
I <sub>OZ</sub>	3-state output current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>					
			output HIGH-state at V <sub>O</sub> = 2.7 V	-	5.0	50	µA
			output LOW-state at V <sub>O</sub> = 0.5 V	-	-5.0	-50	µA
I <sub>CEX</sub>	output HIGH-state leakage current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	5.0	50	µA	
I <sub>O</sub>	output current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 2.5 V	[3]	-50	-65	-180 mA	
I <sub>CC</sub>	quiescent supply current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>					
			outputs HIGH-state	-	110	250	µA
			outputs LOW-state	-	20	30	mA
			outputs 3-state	-	110	250	µA
ΔI <sub>CC</sub>	additional supply current per input pin	V <sub>CC</sub> = 5.5 V; one input at 3.4 V and other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	[4]	-	0.3	1.5 mA	
C <sub>I</sub>	input capacitance	V <sub>I</sub> = 0 V or V <sub>CC</sub>	-	4	-	pF	
C <sub>I/O</sub>	I/O capacitance	outputs disabled; V <sub>O</sub> = 0 V or V <sub>CC</sub>	-	7	-	pF	
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>							
V <sub>IK</sub>	input diode voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-	-	-1.2	V	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>					
		I <sub>OH</sub> = -3 mA	2.5	-	-	V	
		I <sub>OH</sub> = -32 mA	2.0	-	-	V	
		V <sub>CC</sub> = 5.0 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>					
	I <sub>OH</sub> = -3 mA	3.0	-	-	V		
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 4.5 V; I <sub>OL</sub> = 64 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	-	-	0.55	V	
V <sub>RST</sub>	restart LOW-level output voltage	V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 1 mA; V <sub>I</sub> = GND or V <sub>CC</sub>	[1]	-	0.55	V	

**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$I_{LI}$	input leakage current	$V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } 5.5 \text{ V}$					
	control pins		-	-	$\pm 1.0$	$\mu\text{A}$	
	data pins		-	-	$\pm 100$	$\mu\text{A}$	
$I_{OFF}$	power-down leakage current	$V_{CC} = 0 \text{ V}; V_I \text{ or } V_O \leq 4.5 \text{ V}$	-	-	$\pm 100$	$\mu\text{A}$	
$I_{PU}, I_{PD}$	power-up or power-down 3-state output current	$V_{CC} = 2.1 \text{ V}; V_O = 0.5 \text{ V}; V_I = \text{GND or } V_{CC}; V_{OExx} = \text{don't care}$	[2]	-	$\pm 50$	$\mu\text{A}$	
$I_{OZ}$	3-state output current	$V_{CC} = 5.5 \text{ V}; V_I = V_{IL} \text{ or } V_{IH}$					
		output HIGH-state at $V_O = 2.7 \text{ V}$	-	-	50	$\mu\text{A}$	
		output LOW-state at $V_O = 0.5 \text{ V}$	-	-	-50	$\mu\text{A}$	
$I_{CEX}$	output HIGH-state leakage current	$V_{CC} = 5.5 \text{ V}; V_O = 5.5 \text{ V}; V_I = \text{GND or } V_{CC}$	-	-	50	$\mu\text{A}$	
$I_O$	output current	$V_{CC} = 5.5 \text{ V}; V_O = 2.5 \text{ V}$	[3]	-50	-	-180	mA
$I_{CC}$	quiescent supply current	$V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } V_{CC}$					
		outputs HIGH-state	-	-	250	$\mu\text{A}$	
		outputs LOW-state	-	-	30	mA	
		outputs 3-state	-	-	250	$\mu\text{A}$	
$\Delta I_{CC}$	additional supply current per input pin	$V_{CC} = 5.5 \text{ V}; \text{one input at } 3.4 \text{ V and other inputs at } V_{CC} \text{ or GND}; V_{CC} = 5.5 \text{ V}$	[4]	-	-	1.5	mA

[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

[2] This parameter is valid for any  $V_{CC}$  between 0 V and 2.1 V, with a transition time of up to 10 ms. From  $V_{CC} = 2.1 \text{ V}$  to  $V_{CC} = 5 \text{ V} \pm 10 \%$  a transition time of up to 100  $\mu\text{s}$  is permitted.

[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[4] This is the increase in supply current for each input at 3.4 V.

## 11. Dynamic characteristics

**Table 8: Dynamic characteristics** $GND = 0 \text{ V}$ ; for test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25 \text{ }^\circ\text{C}; V_{CC} = 5.0 \text{ V}</math></b>						
$t_{PLH}$	propagation delay					
	An to Bn, Bn to An	see <a href="#">Figure 5</a>	1.7	3.0	3.8	ns
	$\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	see <a href="#">Figure 5</a> and <a href="#">6</a>	2.1	3.5	4.2	ns
$t_{PHL}$	propagation delay					
	An to Bn, Bn to An	see <a href="#">Figure 5</a>	2.4	3.6	4.5	ns
	$\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	see <a href="#">Figure 5</a> and <a href="#">6</a>	3.0	4.4	5.3	ns
$t_{PZH}$	output enable time to HIGH-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see <a href="#">Figure 7</a>	1.8	3.0	3.9	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see <a href="#">Figure 7</a>	1.9	3.4	4.1	ns
$t_{PZL}$	output enable time to LOW-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see <a href="#">Figure 8</a>	2.9	4.2	5.2	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see <a href="#">Figure 8</a>	3.1	4.6	5.5	ns



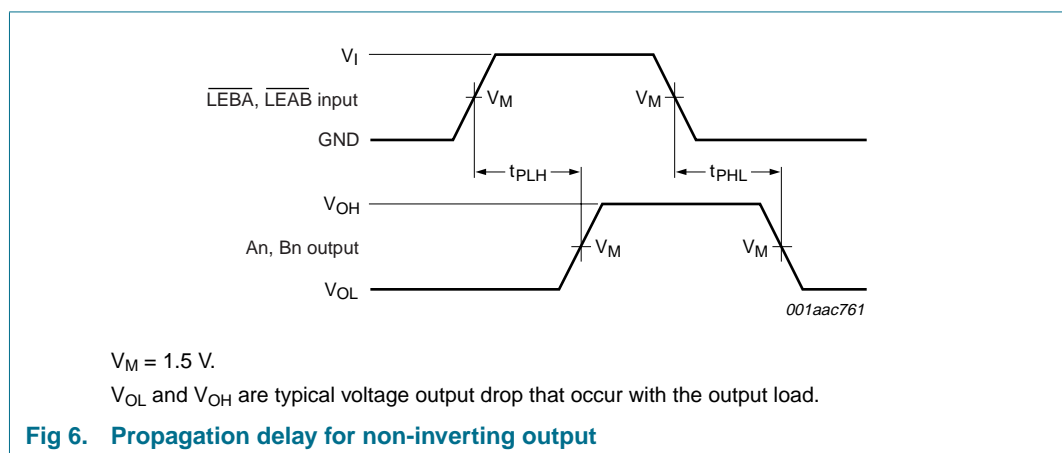
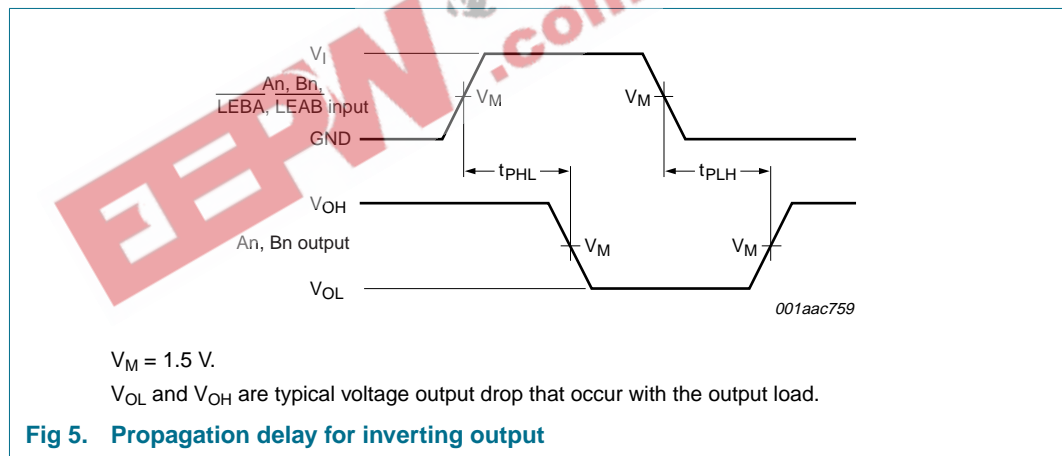
**Table 8: Dynamic characteristics ...continued**  
*GND = 0 V; for test circuit see Figure 10.*

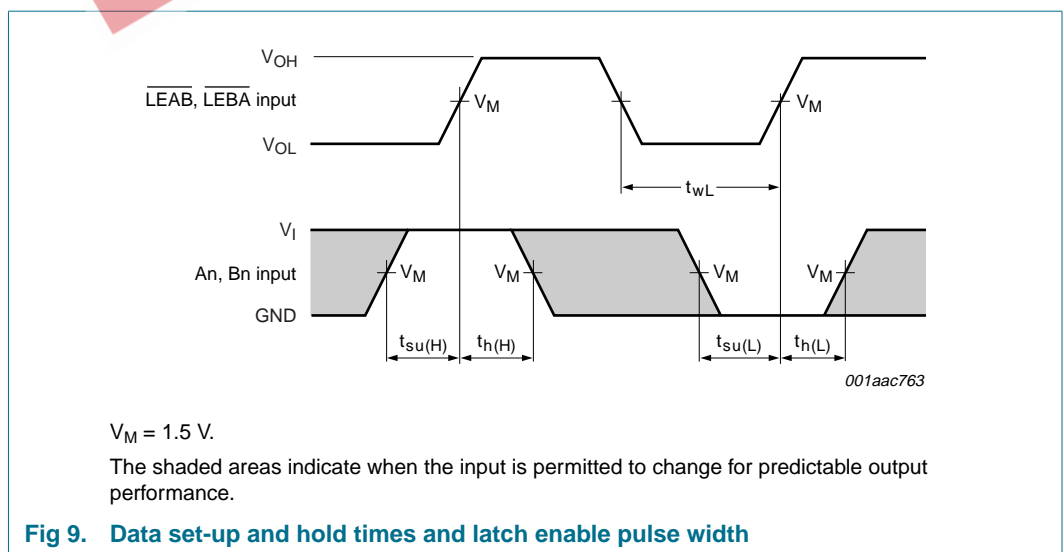
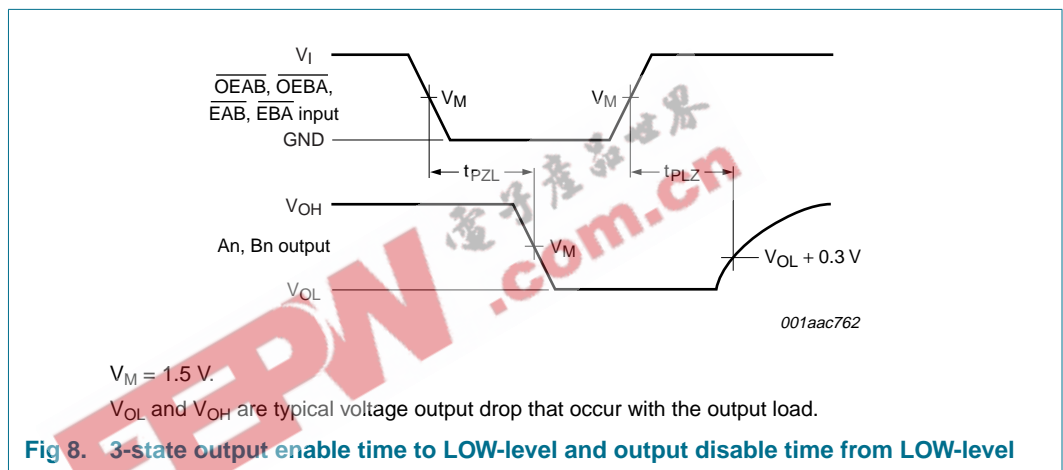
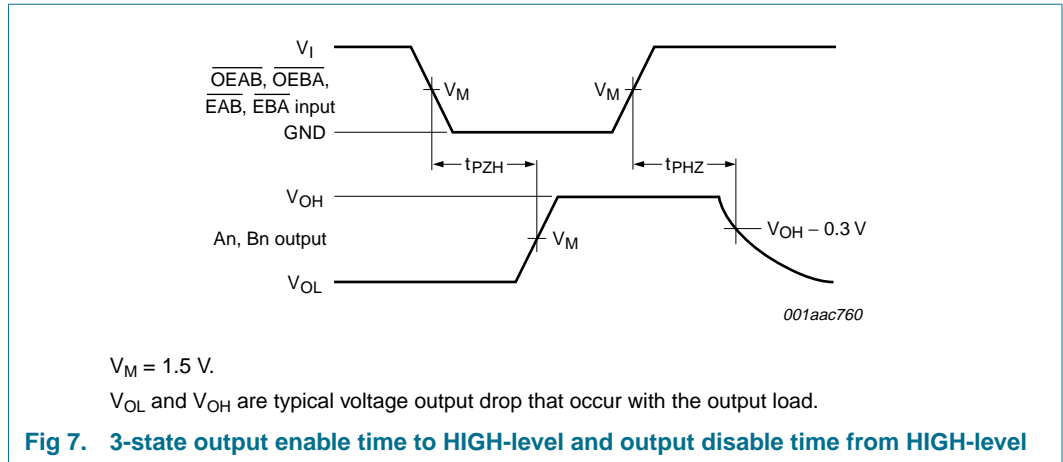
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>PHZ</sub>	output disable time from HIGH-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 7	2.0	3.3	4.3	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 7	2.1	3.4	4.5	ns
t <sub>PLZ</sub>	output disable time from LOW-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 8	2.0	2.8	5.8	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 8	2.0	3.0	6.2	ns
t <sub>su(H)</sub>	set-up time HIGH					
	An to $\overline{LEAB}$ , Bn to $\overline{LEBA}$	see Figure 9	3.0	1.5	-	ns
	An to $\overline{EAB}$ , Bn to $\overline{EBA}$	see Figure 9	3.0	1.5	-	ns
t <sub>su(L)</sub>	set-up time LOW					
	An to $\overline{LEAB}$ , Bn to $\overline{LEBA}$	see Figure 9	3.0	0.6	-	ns
	An to $\overline{EAB}$ , Bn to $\overline{EBA}$	see Figure 9	3.0	0.6	-	ns
t <sub>h(H)</sub>	hold time HIGH					
	An to $\overline{LEAB}$ , Bn to $\overline{LEBA}$	see Figure 9	0.5	-0.3	-	ns
	An to $\overline{EAB}$ , Bn to $\overline{EBA}$	see Figure 9	0.5	-0.2	-	ns
t <sub>h(L)</sub>	hold time LOW					
	An to $\overline{LEAB}$ , Bn to $\overline{LEBA}$	see Figure 9	0.5	-1.3	-	ns
	An to $\overline{EAB}$ , Bn to $\overline{EBA}$	see Figure 9	0.5	-1.3	-	ns
t <sub>wL</sub>	pulse width LOW $\overline{LEAB}$ and $\overline{LEBA}$	see Figure 9	3.5	1.8	-	ns
<b>T<sub>amb</sub> = -40 °C to +85 °C; V<sub>CC</sub> = 5.0 V ± 0.5 V</b>						
t <sub>PLH</sub>	propagation delay					
	An to Bn, Bn to An	see Figure 5	1.7	-	4.7	ns
	$\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	see Figure 5 and 6	2.1	-	5.2	ns
t <sub>PHL</sub>	propagation delay					
	An to Bn, Bn to An	see Figure 5	2.4	-	5.2	ns
	$\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	see Figure 5 and 6	3.0	-	6.2	ns
t <sub>PZH</sub>	output enable time to HIGH-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 7	1.8	-	4.7	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 7	1.9	-	5.0	ns
t <sub>PZL</sub>	output enable time to LOW-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 8	2.9	-	6.1	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 8	3.1	-	6.5	ns
t <sub>PHZ</sub>	output disable time from HIGH-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 7	2.0	-	4.9	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 7	2.1	-	5.2	ns
t <sub>PLZ</sub>	output disable time from LOW-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 8	2.0	-	6.3	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 8	2.0	-	6.7	ns

**Table 8: Dynamic characteristics ...continued**  
*GND = 0 V; for test circuit see Figure 10.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(H)}$	set-up time HIGH					
	An to $\overline{LEAB}$ , Bn to $\overline{LEBA}$	see Figure 9	3.0	-	-	ns
	An to $\overline{EAB}$ , Bn to $\overline{EBA}$	see Figure 9	3.0	-	-	ns
$t_{su(L)}$	set-up time LOW					
	An to $\overline{LEAB}$ , Bn to $\overline{LEBA}$	see Figure 9	3.0	-	-	ns
	An to $\overline{EAB}$ , Bn to $\overline{EBA}$	see Figure 9	3.0	-	-	ns
$t_{h(H)}$	hold time HIGH					
	An to $\overline{LEAB}$ , Bn to $\overline{LEBA}$	see Figure 9	0.5	-	-	ns
	An to $\overline{EAB}$ , Bn to $\overline{EBA}$	see Figure 9	0.5	-	-	ns
$t_{h(L)}$	hold time LOW					
	An to $\overline{LEAB}$ , Bn to $\overline{LEBA}$	see Figure 9	0.5	-	-	ns
	An to $\overline{EAB}$ , Bn to $\overline{EBA}$	see Figure 9	0.5	-	-	ns
$t_{wL}$	pulse width LOW $\overline{LEAB}$ and $\overline{LEBA}$	see Figure 9	3.5	-	-	ns

12. Waveforms





13. Test information

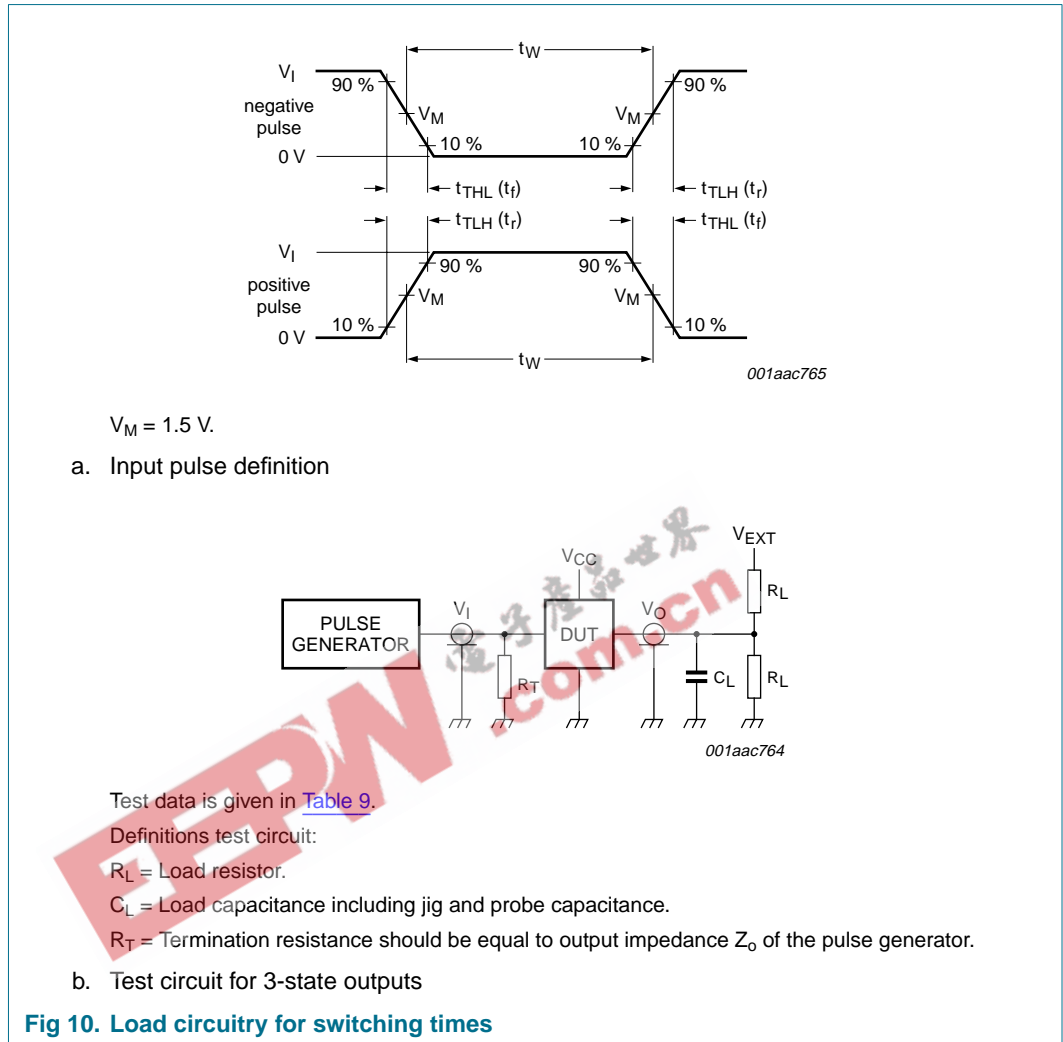


Table 9: Test data

Input				Load		$V_{EXT}$			
$V_I$	$f_i$	$t_W$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$	
3.0 V	1 MHz	500 ns	2.5 ns	50 pF	500 $\Omega$	open	7.0 V	open	

14. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

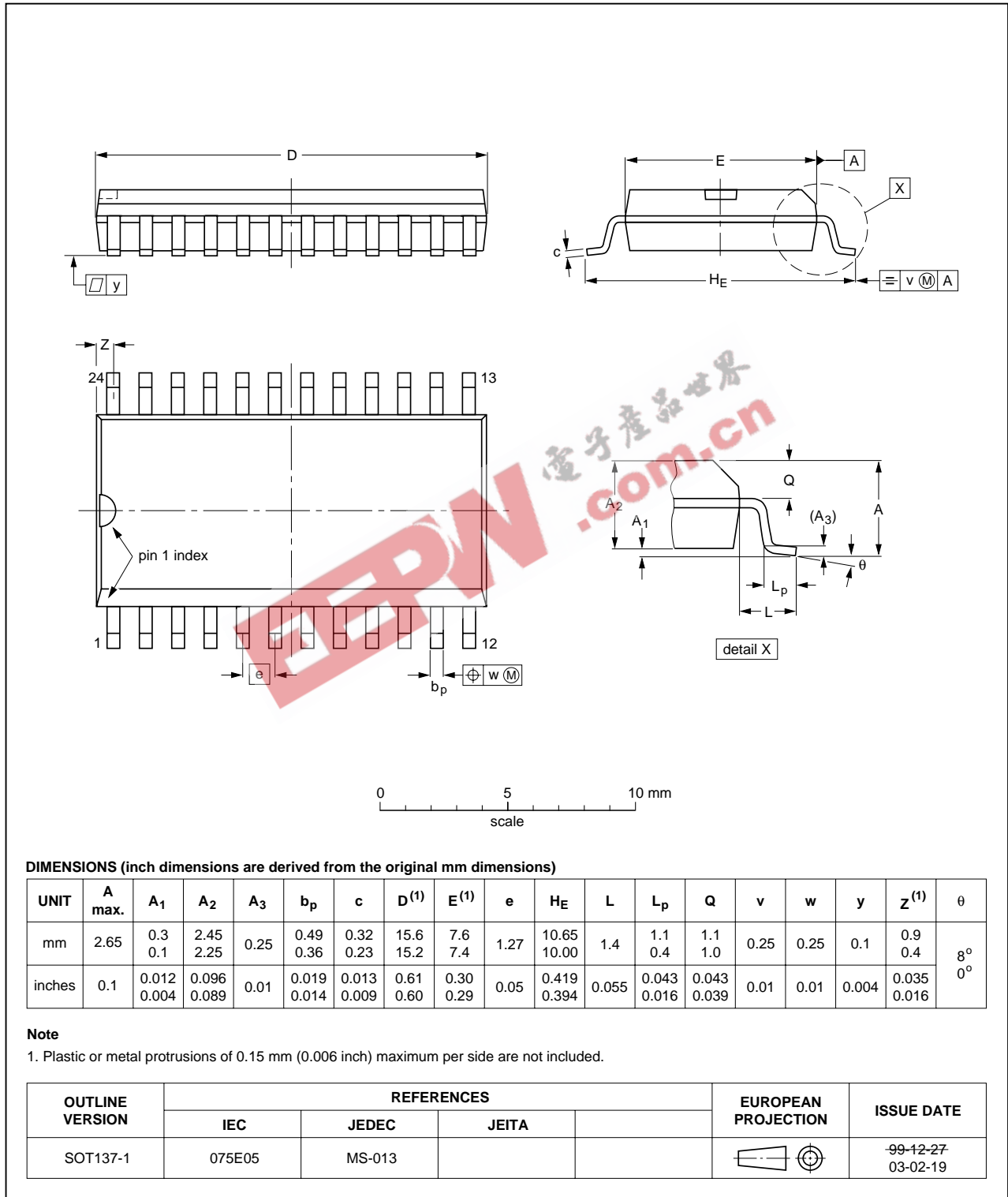


Fig 11. Package outline SOT137-1 (SO24)

DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1

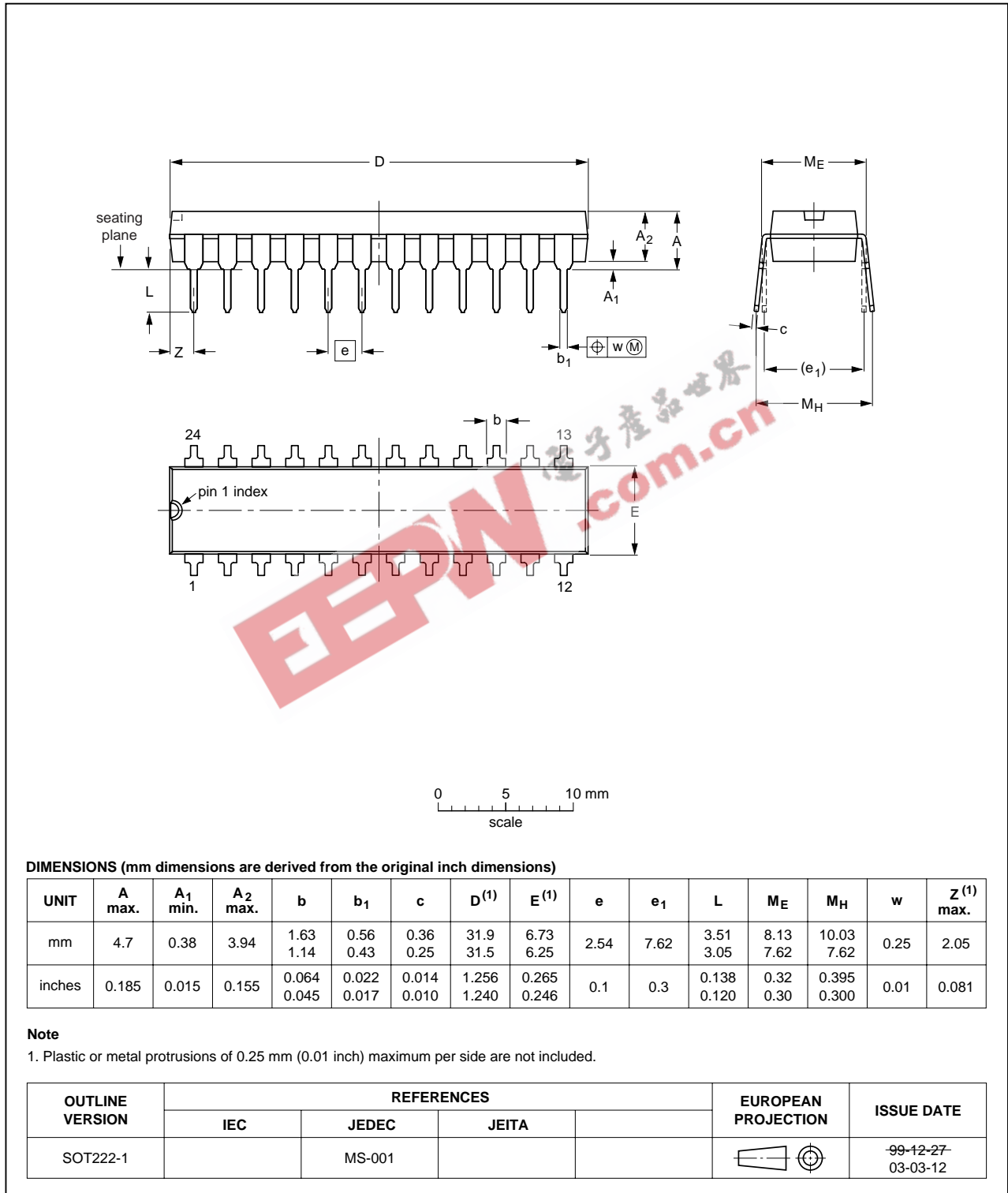


Fig 12. Package outline SOT222-1 (DIP24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

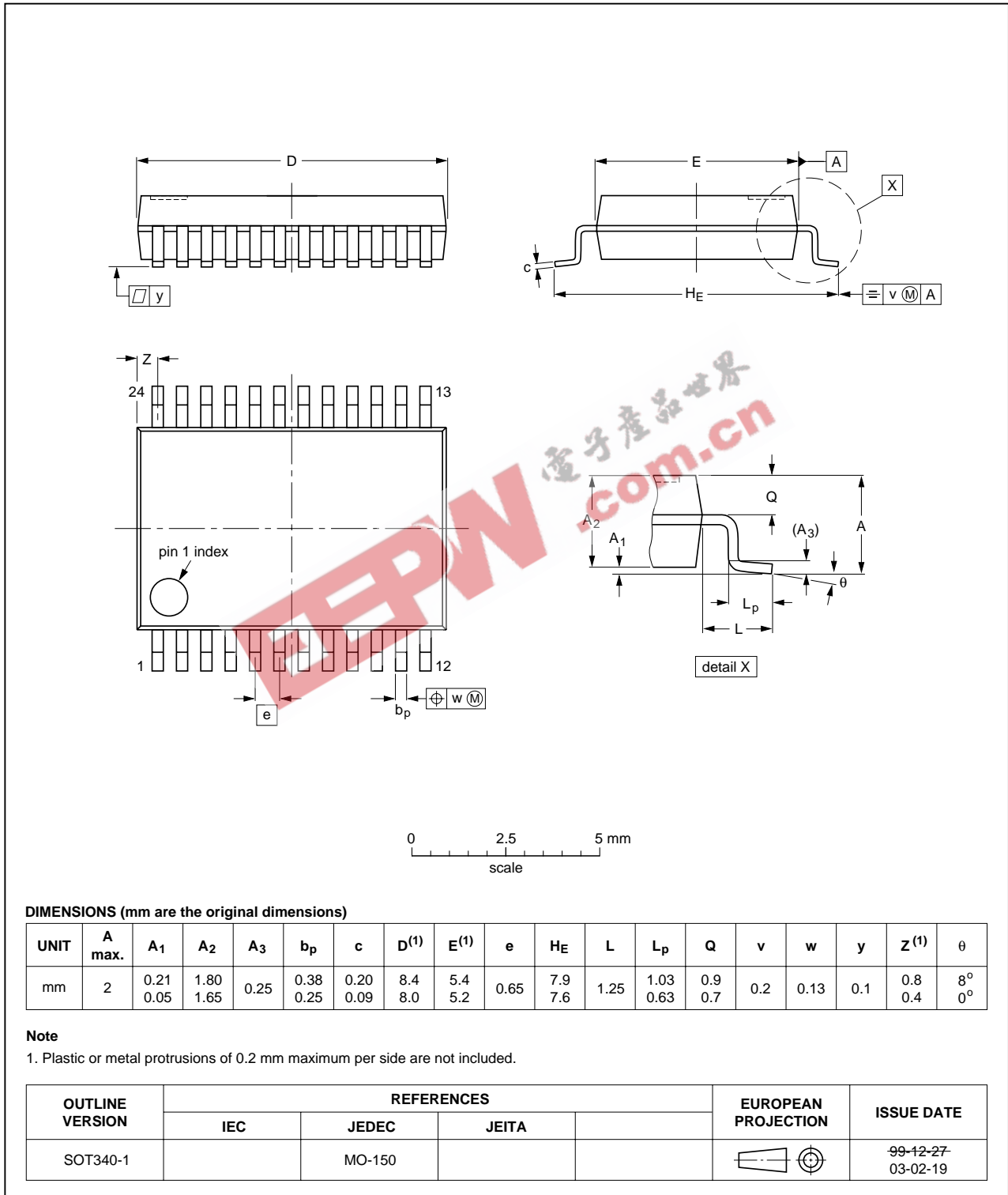


Fig 13. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

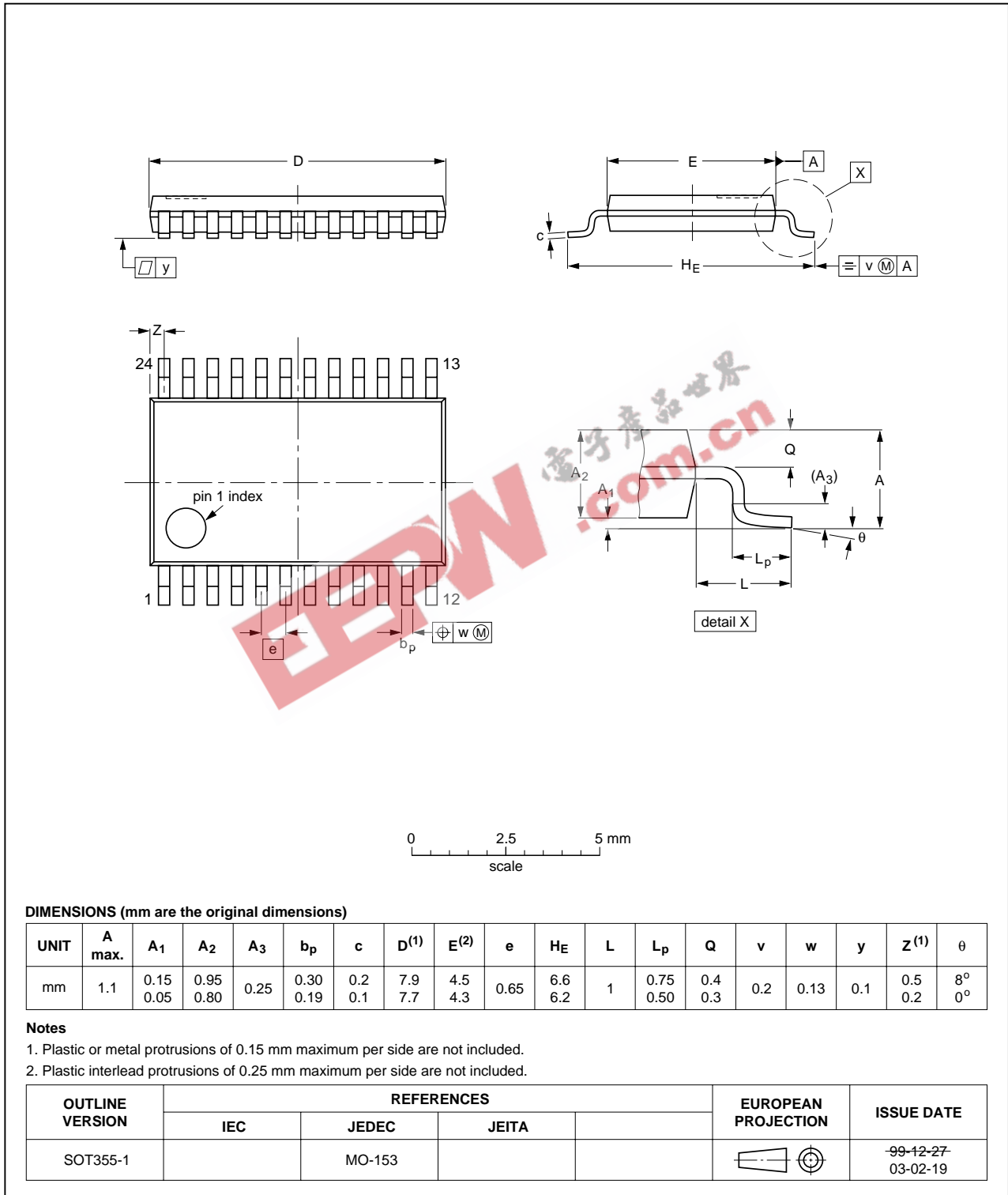


Fig 14. Package outline SOT355-1 (TSSOP24)



## 15. Revision history

**Table 10: Revision history**

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74ABT544_3	20050420	Product data sheet	-	9397 750 14756	74ABT544_2
Modifications:					
					<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li><li>• <a href="#">Section 2</a>; changed latch-up protection to JESD78.</li><li>• <a href="#">Table 1</a>; changed typical values for propagation delay.</li><li>• <a href="#">Table 8</a>; changed values for propagation delay, output enable time and output disable time.</li></ul>
74ABT544_2	20021118	Product specification	-	9397 750 10752	74ABT544
74ABT544	19930701	Product specification	-	-	-

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## 16. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 17. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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