

5-TAP, 3.3V CMOS-INTERFACED FIXED DELAY LINE (SERIES DDU8C3)

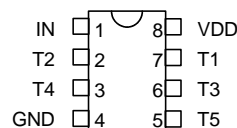
**data
delay
devices, inc.**



FEATURES

- Five equally spaced outputs
- Fits standard 8-pin DIP socket
- Low profile
- Auto-insertable
- Input & outputs fully CMOS interfaced & buffered
- 10 T²L fan-out capability

PACKAGES



DDU8C3-xx DIP
DDU8C3-xxA1 Gull-Wing

FUNCTIONAL DESCRIPTION

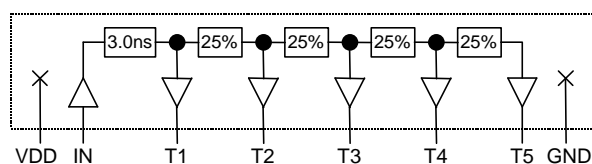
The DDU8C3-series device is a 5-tap digitally buffered delay line. The signal input (IN) is reproduced at the outputs (T1-T5), shifted in time by an amount determined by the device dash number (See Table). For dash numbers 5020 and above, the total delay of the line is measured from IN to T5, and the nominal tap-to-tap delay increment is given by one-fifth of the total delay. For dash numbers below 5020, the total delay is measured from T1 to T5, and the delay increment is given by one-fourth of the total delay.

PIN DESCRIPTIONS

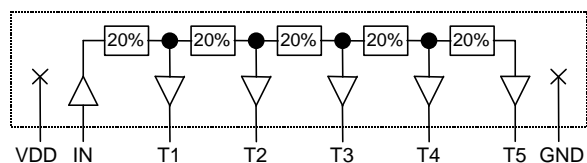
IN Signal Input
T1-T5 Tap Outputs
VDD +3.3 Volts
GND Ground

SERIES SPECIFICATIONS

- **Minimum input pulse width:** 40% of total delay
- **Output rise time:** 2ns typical
- **Supply voltage:** 3.3VDC \pm 0.3V
- **Supply current:** I_{CC}L = 40 μ a typical
I_{CC}H = 7ma typical
- **Operating temperature:** -40° to 85° C
- **Temp. coefficient of total delay:** 300 PPM/°C



Functional diagram for dash numbers < 5020



Functional diagram for dash numbers \geq 5020

DASH NUMBER SPECIFICATIONS

| Part Number | Total Delay (ns) | Delay Per Tap (ns) |
|-------------|------------------|--------------------|
| DDU8C3-5004 | 4 \pm 1.0 * | 1.0 \pm 0.5 |
| DDU8C3-5006 | 6 \pm 1.0 * | 1.5 \pm 0.5 |
| DDU8C3-5008 | 8 \pm 2.0 * | 2.0 \pm 1.0 |
| DDU8C3-5010 | 10 \pm 2.0 * | 2.5 \pm 1.0 |
| DDU8C3-5012 | 12 \pm 2.0 * | 3.0 \pm 1.0 |
| DDU8C3-5014 | 14 \pm 2.0 * | 3.5 \pm 1.0 |
| DDU8C3-5020 | 20 \pm 2.0 | 4.0 \pm 1.0 |
| DDU8C3-5025 | 25 \pm 2.0 | 5.0 \pm 1.5 |
| DDU8C3-5030 | 30 \pm 2.0 | 6.0 \pm 1.5 |
| DDU8C3-5035 | 35 \pm 2.0 | 7.0 \pm 1.8 |
| DDU8C3-5040 | 40 \pm 2.0 | 8.0 \pm 2.0 |
| DDU8C3-5045 | 45 \pm 2.25 | 9.0 \pm 2.0 |
| DDU8C3-5050 | 50 \pm 2.5 | 10.0 \pm 2.0 |
| DDU8C3-5060 | 60 \pm 3.0 | 12.0 \pm 2.0 |
| DDU8C3-5075 | 75 \pm 3.75 | 15.0 \pm 2.5 |
| DDU8C3-5100 | 100 \pm 5.0 | 20.0 \pm 3.0 |
| DDU8C3-5125 | 125 \pm 6.5 | 25.0 \pm 3.0 |
| DDU8C3-5150 | 150 \pm 7.5 | 30.0 \pm 3.0 |
| DDU8C3-5175 | 175 \pm 8.0 | 35.0 \pm 4.0 |
| DDU8C3-5200 | 200 \pm 10.0 | 40.0 \pm 4.0 |
| DDU8C3-5250 | 250 \pm 12.5 | 50.0 \pm 5.0 |

* Total delay is referenced to first tap output
Input to first tap = 3.0ns \pm 1ns

NOTE: Any dash number between 5004 and 5250 not shown is also available.

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APPLICATION NOTES

HIGH FREQUENCY RESPONSE

The DDU8C3 tolerances are guaranteed for input pulse widths and periods greater than those specified in the test conditions. Although the device will function properly for pulse widths as small as 40% of the total delay and periods as small as 80% of the total delay (for a symmetric input), the delays may deviate from their values at low frequency. However, for a given input condition, the deviation will be repeatable from pulse to pulse. Contact technical support at Data

Delay Devices if your application requires device testing at a specific input condition.

POWER SUPPLY BYPASSING

The DDU8C3 relies on a stable power supply to produce repeatable delays within the stated tolerances. A 0.1uf capacitor from VDD to GND, located as close as possible to the VDD pin, is recommended. A wide VDD trace and a clean ground plane should be used.

DEVICE SPECIFICATIONS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

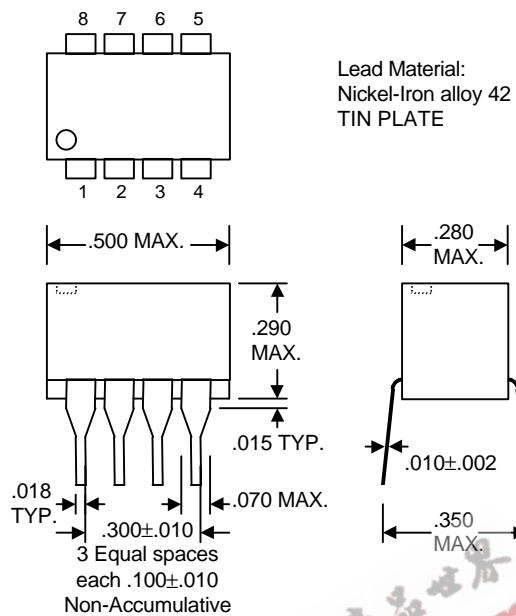
| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---------------------|------------|------|--------------|-------|--------|
| DC Supply Voltage | V_{DD} | -0.3 | 7.0 | V | |
| Input Pin Voltage | V_{IN} | -0.3 | $V_{DD}+0.3$ | V | |
| Storage Temperature | T_{STRG} | -55 | 150 | C | |
| Lead Temperature | T_{LEAD} | | 300 | C | 10 sec |

TABLE 2: DC ELECTRICAL CHARACTERISTICS

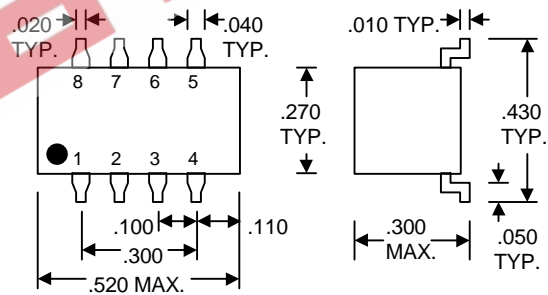
(-40C to 85C, 3.00V to 3.60V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|----------|------|------|-------|---------|--|
| High Level Output Voltage | V_{OH} | 3.00 | 3.20 | | V | $V_{DD} = 3.3$, $I_{OH} = MAX$ $V_{IH} = MIN$, $V_{IL} = MAX$ |
| Low Level Output Voltage | V_{OL} | | 0.10 | 0.30 | V | $V_{DD} = 3.3$, $I_{OL} = MAX$ $V_{IH} = MIN$, $V_{IL} = MAX$ |
| High Level Output Current | I_{OH} | | | -24.0 | mA | |
| Low Level Output Current | I_{OL} | | | 24.0 | mA | |
| High Level Input Voltage | V_{IH} | 2.50 | | | V | |
| Low Level Input Voltage | V_{IL} | | | 0.80 | V | |
| Input Current | I_{IH} | | | 0.10 | μA | $V_{DD} = 3.3$ |

PACKAGE DIMENSIONS



DDU8C3-xx (DIP)



DDU8C3-xxA1 (Gull-Wing)

DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

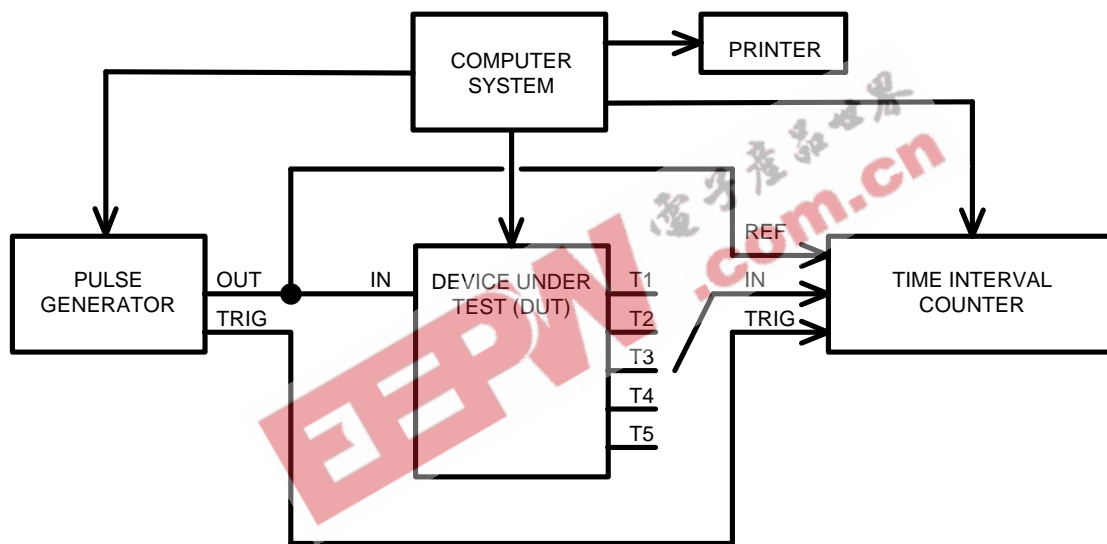
INPUT:

Ambient Temperature: $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$
Supply Voltage (VDD): $3.3\text{V} \pm 0.1\text{V}$
Input Pulse: High = $3.3\text{V} \pm 0.1\text{V}$
 Low = $0.0\text{V} \pm 0.1\text{V}$
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured
 between 0.5V and 2.8V)
Pulse Width: $\text{PW}_{\text{IN}} = 1.5 \times \text{Total Delay}$
Period: $\text{PER}_{\text{IN}} = 10 \times \text{Total Delay}$

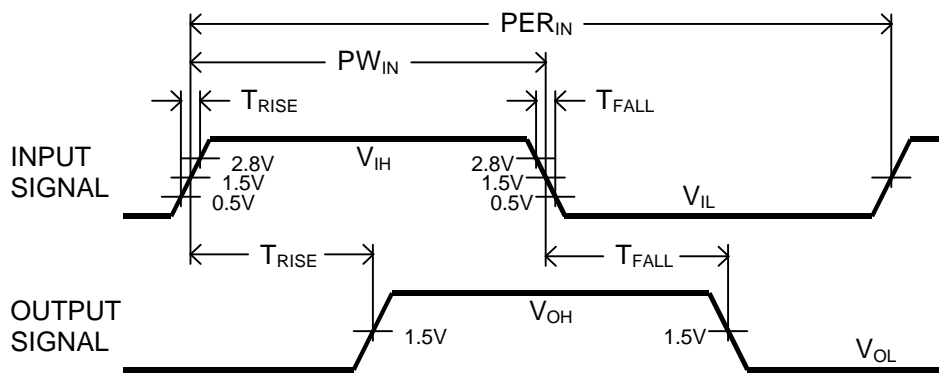
OUTPUT:

Load: 1 CMOS Gate
 C_{load} : $5\text{pf} \pm 10\%$
Threshold: 1.65V (Rising & Falling)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Test Setup



Timing Diagram For Testing