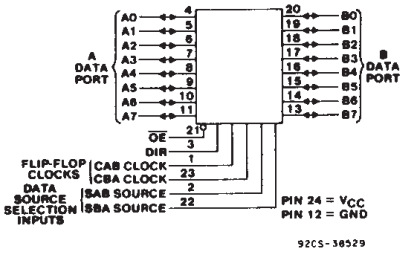
CD54/74HC646, CD54/74HCT646
CD54/74HC648, CD54/74HCT648

File Number 1664

High-Speed CMOS Logic

TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS278



FUNCTIONAL DIAGRAM

Octal Bus Transceiver/Register, 3-State

Type Features:

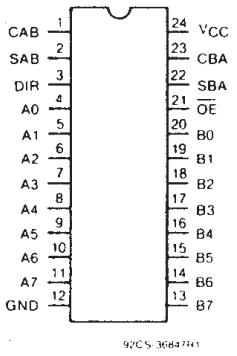
- *Independent Registers for A and B Buses*
- *CD54/74HC/HCT646 Non-Inverting CD54/74HC/HCT648 Inverting*
- *3-State Outputs*
- *Drives 15LSTTL loads*
- *Typical Propagation Delay = 12ns (A ↔ B) @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C*

The RCA-CD54/74HC646 and CD54/74HCT646 are octal bus transceivers/registers with 3-state non-inverting outputs. The RCA-CD54/74HC648 and CD54/74HCT648 are octal bus transceivers/registers with 3-state inverting outputs. These devices are bus transceivers with D-type flip-flops which act as internal storage registers. Data on the A bus or the B bus can be clocked into the registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output enable ($\overline{OE}$) and direction (DIR) inputs control the transceiver functions. Data present at the high impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The direction control determines which data bus will receive data when the output enable ($\overline{OE}$) is LOW. In the high impedance mode (output enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the direction (DIR) and output enable ($\overline{OE}$) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

The CD54HC646, 648 and CD54HCT646, 648 are supplied in 24-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC646, 648 and CD74HCT646, 648 are supplied in 24-lead dual-in-line, narrow-body plastic packages (EN suffix), in 24-lead dual-in-line, wide-body plastic packages (E suffix), and in 24-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

This data sheet is applicable to the CD54HC646 and CD74HCT646. The CD54HCT646, CD54HC648, CD54HCT648, and CD74HCT648 were not acquired from Harris Semiconductor. See SCHS193 for information on the CD74HC646.

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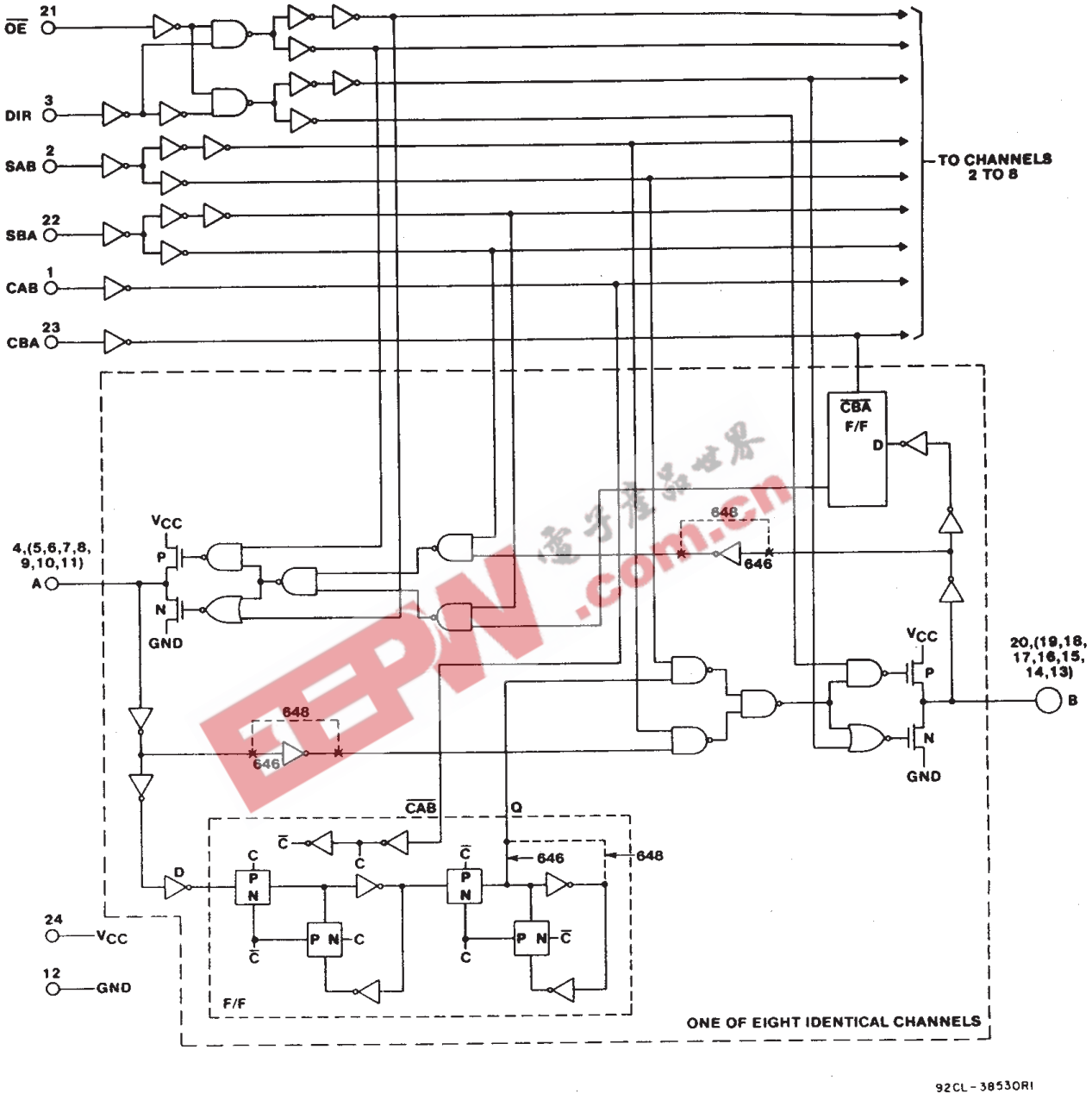

Fig. 1 — Logic Diagram.

CD54/74HC646, CD54/74HCT646
CD54/74HC648, CD54/74HCT648

FUNCTION TABLE

INPUTS						DATA I/O #		OPERATION OR FUNCTION	
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	646	648
X	X	↓	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↓	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↓	↓	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
To prevent excess currents in the High-Z modes all I/O terminals should be terminated with 10KΩ resistors.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} + 0.5V) ..... ±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±70mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to + 100° C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to + 125° C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -40 to + 85° C
PACKAGE TYPE F, H ..... -55 to + 125° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to + 150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... + 265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... + 300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC646, CD54/74HCT646
CD54/74HC648, CD54/74HCT648

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC646/CD54HC646 CD74HC648/CD54HC648										CD74HCT646/CD54HCT646 CD74HCT648/CD54HCT648									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
High-Level Output Voltage V_{OH} TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
Low-Level Output Voltage V_{OL} TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{OE}$	1.3
DIR	0.75
Clock A→B, B→A	0.6
Select A, Select B	0.45
Inputs A0-A7, B0-B7	0.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_n, t_r = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delays Store A Data to B Bus (646)	t_{PLH}, t_{PHL}	15	18	18	ns
Store B Data to A Bus (646)	t_{PLH}, t_{PHL}	15	18	18	ns
Store $\overline{A}$ Data to B Bus (648)	t_{PLH}, t_{PHL}	15	20	23	ns
Store $\overline{B}$ Data to A Bus (648)	t_{PLH}, t_{PHL}	15	20	23	ns
A Data to B Bus (646)	t_{PLH}, t_{PHL}	15	12	15	ns
B Data to A Bus (646)	t_{PLH}, t_{PHL}	15	12	15	ns
$\overline{A}$ Data to B Bus (648)	t_{PLH}, t_{PHL}	15	12	15	ns
$\overline{B}$ Data to A Bus (648)	t_{PLH}, t_{PHL}	15	12	15	ns
Select to Data (646)	t_{PLH}, t_{PHL}	15	14	19	ns
Select to Data (648)	t_{PLH}, t_{PHL}	15	16	19	ns
3-State Disabling Time	t_{PLZ}, t_{PHZ}	15	14	14	ns
3-State Enabling Time	t_{PZL}, t_{PZH}	15	14	19	ns
Max Frequency	f_{max}	15	60	45	MHz
Power Dissipation Capacitance*	C_{PD}	—	52	52	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 C_{PD} f_i + \Sigma V_{CC}^2 C_L f_o$ where:
C_L = output load capacitance
V_{CC} = supply voltage
f_i = input frequency
f_o = output frequency

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHZ
		4.5	30	—	25	—	25	—	20	—	20	—	17	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
Set Up Time Data to Clock	t_{SU}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time Data to Clock	t_H	2	35	—	—	—	45	—	—	—	55	—	—	—	ns
		4.5	7	—	5	—	9	—	5	—	11	—	5	—	
		6	6	—	—	—	8	—	—	—	9	—	—	—	
Clock Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	25	—	20	—	31	—	24	—	38	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

CD54/74HC646, CD54/74HCT646
CD54/74HC648, CD54/74HCT648

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,		2	—	220	—	—	—	275	—	—	—	330	—	—	
Store A data to B bus	t_{PLH}	4.5	—	44	—	44	—	55	—	55	—	66	—	66	ns
Store B data to B bus (646)	t_{PHL}	6	—	37	—	—	—	47	—	—	—	5.6	—	—	
Store $\overline{A}$ data to B bus	t_{PLH}	2	—	240	—	—	—	300	—	—	—	360	—	—	
Store $\overline{B}$ data to A Bus	t_{PHL}	4.5	—	48	—	54	—	60	—	68	—	72	—	81	ns
(648)		6	—	41	—	—	—	51	—	—	—	61	—	—	
A data to B bus	t_{PLH}	2	—	135	—	—	—	170	—	—	—	205	—	—	
B data to A Bus	t_{PHL}	4.5	—	27	—	37	—	34	—	46	—	41	—	56	ns
(646)		6	—	23	—	—	—	29	—	—	—	35	—	—	
$\overline{A}$ data to B bus	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
$\overline{B}$ data to A Bus	t_{PHL}	4.5	—	30	—	37	—	38	—	46	—	45	—	56	ns
(648)		6	—	26	—	—	—	33	—	—	—	38	—	—	
Select to Data		2	—	170	—	—	—	215	—	—	—	255	—	—	
	t_{PLH}	4.5	—	34	—	46	—	43	—	58	—	51	—	69	ns
(646)	t_{PHL}	6	—	29	—	—	—	37	—	—	—	43	—	—	
Select to Data		2	—	190	—	—	—	240	—	—	—	285	—	—	
	t_{PLH}	4.5	—	38	—	46	—	48	—	58	—	57	—	69	ns
(648)	t_{PHL}	6	—	32	—	—	—	39	—	—	—	48	—	—	
3-State Disabling Time		2	—	175	—	—	—	220	—	—	—	265	—	—	
Bus to Output or	t_{PLZ}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	ns
Register to Output	t_{PHZ}	6	—	30	—	—	—	37	—	—	—	45	—	—	
3-State Enabling Time		2	—	175	—	—	—	220	—	—	—	265	—	—	
Bus to Output or	t_{PZL}	4.5	—	35	—	45	—	44	—	56	—	53	—	68	ns
Register to Output	t_{PZH}	6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Transition Time		2	—	60	—	—	—	75	—	—	—	90	—	—	
	t_{TLH}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
	t_{THL}	6	—	10	—	—	—	13	—	—	—	15	—	—	
3-State Output			—	—	—	—	—	—	—	—	—	—	—	—	
Capacitance	C_o	—	—	20	—	20	—	20	—	20	—	20	—	20	pF
			—	—	—	—	—	—	—	—	—	—	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

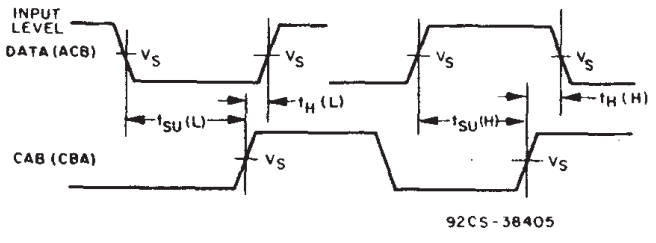
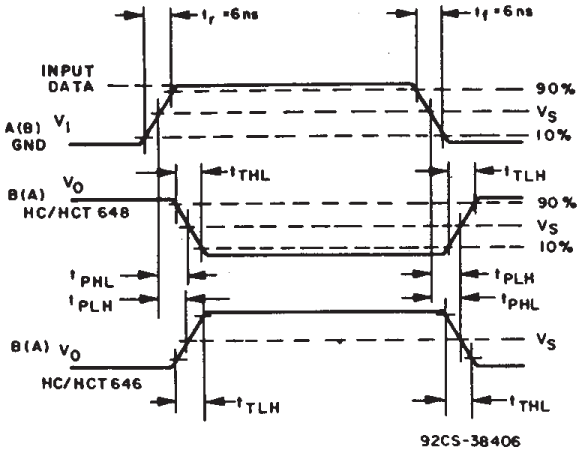
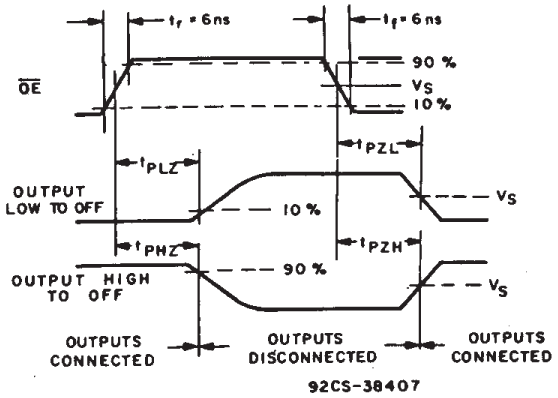


Fig. 2 — Data setup and hold times.

CD54/74HC646, CD54/74HCT646
CD54/74HC648, CD54/74HCT648





	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 3 — Transition times and propagation delay times.

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