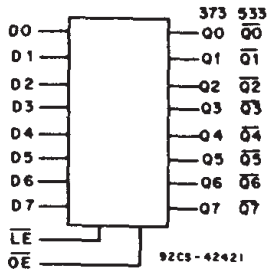


CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533



Data sheet acquired from Harris Semiconductor
SCHS289



Octal Transparent Latch, 3-State

CD54/74AC/ACT373 - Non-Inverting
CD54/74AC/ACT533 - Inverting

Type Features:

- Buffered inputs
- Typical propagation delay:
4.3 ns @ $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$

FUNCTIONAL DIAGRAM

The RCA-CD54/74AC373 and CD54/74AC533 and the CD54/74ACT373 and CD54/74ACT533 octal transparent 3-state latches use the RCA ADVANCED CMOS technology. The outputs are transparent to the inputs when the Latch Enable (\overline{LE}) is HIGH. When the Latch Enable (\overline{LE}) goes LOW, the data is latched. The Output Enable (\overline{OE}) controls the 3-state outputs. When the Output Enable (\overline{OE}) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The CD74AC/ACT373 and CD74AC/ACT533 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT373 and CD54AC/ACT533, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$ output drive current
 - Fanout to 15 FAST* ICs
 - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

| Output Enable | Latch Enable | Data | AC/ACT373 Output | AC/ACT533 Output |
|---------------|--------------|------|------------------|------------------|
| L | H | H | H | L |
| L | H | L | L | H |
| L | L | l | L | H |
| L | L | h | H | L |
| H | X | X | Z | Z |

Note:

L = Low voltage level
H = High voltage level

l = Low voltage level one set-up time prior to the high to low latch enable transition

h = High voltage level one set-up time prior to the high to low latch enable transition.

X = Don't Care
Z = High Impedance State

Technical Data

CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|--|---|
| DC SUPPLY-VOLTAGE (V_{CC}) | -0.5 to 6 V |
| DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) | ± 20 mA |
| DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) | ± 50 mA |
| DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) | ± 50 mA |
| DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) | ± 100 mA* |
| POWER DISSIPATION PER PACKAGE (P_D): | |
| For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E) | 500 mW |
| For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E) | Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW |
| For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M) | 400 mW |
| For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M) | Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW |
| OPERATING-TEMPERATURE RANGE (T_A) | -55 to $+125^\circ\text{C}$ |
| STORAGE TEMPERATURE (T_{STG}) | -65 to $+150^\circ\text{C}$ |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s maximum | $+265^\circ\text{C}$ |
| Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only | $+300^\circ\text{C}$ |

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:

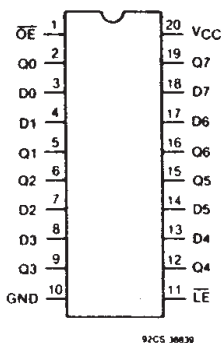
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | LIMITS | | UNITS |
|---|--------|----------|------------------|
| | MIN. | MAX. | |
| Supply-Voltage Range, V_{CC} *: (For $T_A =$ Full Package-Temperature Range) | | | |
| AC Types | 1.5 | 5.5 | V |
| ACT Types | 4.5 | 5.5 | |
| DC Input or Output Voltage, V_I, V_O | 0 | V_{CC} | V |
| Operating Temperature, T_A | -55 | $+125$ | $^\circ\text{C}$ |
| Input Rise and Fall Slew Rate, dt/dv | | | |
| at 1.5 V to 3 V(AC Types) | 0 | 50 | ns/V |
| at 3.6 V to 5.5 V(AC Types) | 0 | 20 | ns/V |
| at 4.5 V to 5.5 V(ACT Types) | 0 | 10 | ns/V |

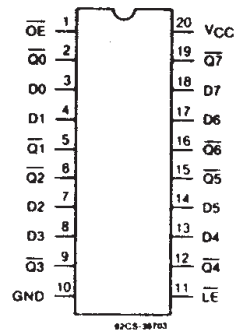
*Unless otherwise specified, all voltages are referenced to ground.

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TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC373, CD54/74ACT373



CD54/74AC533, CD54/74ACT533

Technical Data

CD54/74AC373, CD54/74AC533
CD54/74ACT373, CD54/74ACT533

STATIC ELECTRICAL CHARACTERISTICS: AC Series

| CHARACTERISTICS | TEST CONDITIONS | | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | | | UNITS |
|--|--|-------|------------------------|--|------|------------|------|-------------|------|-------|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | |
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| High-Level Input Voltage V _{IH} | | | 1.5 | 1.2 | — | 1.2 | — | 1.2 | — | V |
| | | | 3 | 2.1 | — | 2.1 | — | 2.1 | — | |
| | | | 5.5 | 3.85 | — | 3.85 | — | 3.85 | — | |
| Low-Level Input Voltage V _{IL} | | | 1.5 | — | 0.3 | — | 0.3 | — | 0.3 | V |
| | | | 3 | — | 0.9 | — | 0.9 | — | 0.9 | |
| | | | 5.5 | — | 1.65 | — | 1.65 | — | 1.65 | |
| High-Level Output Voltage V _{OH} | V _{IH} or V _{IL} | -0.05 | 1.5 | 1.4 | — | 1.4 | — | 1.4 | — | V |
| | | | 3 | 2.9 | — | 2.9 | — | 2.9 | — | |
| | | | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | |
| | | | 3 | 2.58 | — | 2.48 | — | 2.4 | — | |
| | | | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | | | 5.5 | — | — | 3.85 | — | — | — | |
| Low-Level Output Voltage V _{OL} | V _{IH} or V _{IL} | 0.05 | 1.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 3 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | | 3 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | | 5.5 | — | — | — | 1.65 | — | — | |
| Input Leakage Current I _I | V _{CC} or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA |
| | | | | | | | | | | |
| 3-State Leakage Current I _{OZ} | V _{IH} or V _{IL} | | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA |
| | | | | | | | | | | |
| Quiescent Supply Current, MS _I | V _{CC} or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

Technical Data

CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

| CHARACTERISTICS | TEST CONDITIONS | V_{CC} (V) | AMBIENT TEMPERATURE (T_A) - °C | | | | | | UNITS | | |
|---|-----------------|---|------------------------------------|------|------------|------|-------------|------|----------|---------|---|
| | | | +25 | | -40 to +85 | | -55 to +125 | | | | |
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | | |
| High-Level Input Voltage | V_{IH} | | 4.5 to 5.5 | 2 | — | 2 | — | 2 | — | V | |
| Low-Level Input Voltage | V_{IL} | | 4.5 to 5.5 | — | 0.8 | — | 0.8 | — | 0.8 | V | |
| High-Level Output Voltage | V_{OH} | V_{IH} or V_{IL} #, * | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | V |
| | | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | | | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low-Level Output Voltage | V_{OL} | V_{IH} or V_{IL} #, * | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current | I_i | V_{CC} or GND | 5.5 | — | ± 0.1 | — | ± 1 | — | ± 1 | μA | |
| 3-State Leakage Current | I_{OZ} | V_{IH} or V_{IL} $V_O = V_{CC}$ or GND | 5.5 | — | ± 0.5 | — | ± 5 | — | ± 10 | μA | |
| Quiescent Supply Current, MSI | I_{CC} | V_{CC} or GND | 5.5 | — | 8 | — | 80 | — | 160 | μA | |
| Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load | ΔI_{CC} | $V_{CC}-2.1$ | 4.5 to 5.5 | — | 2.4 | — | 2.8 | — | 3 | mA | |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

| INPUT | UNIT LOAD* | |
|-----------------|------------|--------|
| | ACT373 | ACT533 |
| \overline{OE} | 0.87 | 0.87 |
| \overline{Dn} | 0.5 | 0.5 |
| \overline{LE} | 0.8 | 0.8 |

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Technical Data

CD54/74AC373, CD54/74AC533
CD54/74ACT373, CD54/74ACT533

PREREQUISITE FOR SWITCHING: AC Series

| CHARACTERISTICS | SYMBOL | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | UNITS |
|-----------------------|-----------------|------------------------|--|------|-------------|------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| LE Pulse Width | t _w | 1.5 | 44 | — | 50 | — | ns |
| | | 3.3* | 4.9 | — | 5.6 | — | |
| | | 5† | 3.5 | — | 4 | — | |
| Setup Time Data to LE | t _{su} | 1.5 | 2 | — | 2 | — | ns |
| | | 3.3 | 2 | — | 2 | — | |
| | | 5 | 2 | — | 2 | — | |
| Hold Time Data to LE | t _h | 1.5 | 33 | — | 38 | — | ns |
| | | 3.3 | 3.7 | — | 4.2 | — | |
| | | 5 | 2.6 | — | 3 | — | |

*3.3 V: min. is @ 3 V
 †5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

| CHARACTERISTICS | SYMBOL | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | UNITS |
|---|--------------------------------------|------------------------|--|------|-------------|------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Data to Qn | t _{PLH} t _{PHL} | 1.5 | — | 96 | — | 106 | ns |
| | | 3.3* | 3.1 | 10.8 | 3 | 11.9 | |
| | | 5† | 2.2 | 7.7 | 2.1 | 8.5 | |
| 373 | t _{PLH} t _{PHL} | 1.5 | — | 119 | — | 131 | ns |
| | | 3.3 | 3.8 | 13.4 | 3.7 | 14.7 | |
| | | 5 | 2.7 | 9.5 | 2.6 | 10.5 | |
| LE on Qn | t _{PLH} t _{PHL} | 1.5 | — | 136 | — | 150 | ns |
| | | 3.3 | 4.3 | 15.2 | 4.2 | 16.8 | |
| | | 5 | 3.1 | 10.9 | 3 | 12 | |
| 533 | t _{PLH} t _{PHL} | 1.5 | — | 136 | — | 150 | ns |
| | | 3.3 | 4.3 | 15.3 | 4.2 | 16.8 | |
| | | 5 | 3.1 | 10.9 | 3 | 12 | |
| Output Enable Times | t _{PZL} t _{PZH} | 1.5 | — | 119 | — | 131 | ns |
| | | 3.3 | 4.1 | 14.4 | 4 | 15.8 | |
| | | 5 | 2.7 | 9.5 | 2.6 | 10.5 | |
| Output Disable Times | t _{PLZ} t _{PHZ} | 1.5 | — | 131 | — | 144 | ns |
| | | 3.3 | 3.7 | 13.1 | 3.6 | 14.4 | |
| | | 5 | 3 | 10.5 | 2.9 | 11.5 | |
| Power Dissipation Capacitance | C _{PD} § | — | 63 Typ. | | 63 Typ. | | pF |
| Min. (Valley) V _{OH} During Switching of Other Outputs (Output Under Test Not Switching) | V _{OHV} See Fig. 1 | 5 | 4 Typ. @ 25°C | | | | V |
| Max. (Peak) V _{OL} During Switching of Other Outputs (Output Under Test Not Switching) | V _{OLP} See Fig. 1 | 5 | 1 Typ. @ 25°C | | | | V |
| Input Capacitance | C _I | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | C _O | — | — | 15 | — | 15 | pF |

*3.3 V: min. is @ 3.6 V
 max. is @ 3 V
 †5 V: min. is @ 5.5 V
 max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per latch.
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

Technical Data

CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

PREREQUISITE FOR SWITCHING: ACT Series

| CHARACTERISTICS | SYMBOL | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) -°C | | | | UNITS |
|-----------------------|-----------------|------------------------|---|------|-------------|------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| LE Pulse Width | t _w | 5† | 3.6 | — | 4 | — | ns |
| Setup Time Data to LE | t _{su} | 5 | 2 | — | 2 | — | ns |
| Hold Time Data to LE | t _h | 5 | 2.7 | — | 3 | — | ns |

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

| CHARACTERISTICS | SYMBOL | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) -°C | | | | UNITS |
|---|--------------------------------------|------------------------|---|------|-------------|------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Data to Qn | 373 t _{PLH} | 5† | 2.7 | 9.5 | 2.6 | 10.4 | ns |
| | 533 t _{PHL} | | 3 | 10.4 | 2.9 | 11.4 | |
| LE to Qn | 373 t _{PLH} | 5 | 3.1 | 11.4 | 3 | 12.5 | ns |
| | 533 t _{PHL} | | | | | | |
| Output Enable Times | t _{PZL} t _{PZH} | 5 | 3.5 | 12.3 | 3.4 | 13.5 | ns |
| Output Disable Times | t _{PLZ} t _{PHZ} | 5 | 3.2 | 11.4 | 3.1 | 12.5 | ns |
| Power Dissipation Capacitance | C _{PD} § | — | 63 Typ. | | 63 Typ. | | pF |
| Min. (Valley) V _{OH} During Switching of Other Outputs (Output Under Test Not Switching) | V _{OHV} See Fig. 1 | 5 | 4 Typ. @ 25°C | | | | V |
| Max. (Peak) V _{OL} During Switching of Other Outputs (Output Under Test Not Switching) | V _{OLP} See Fig. 1 | 5 | 1 Typ. @ 25°C | | | | V |
| Input Capacitance | C _I | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | C _O | — | — | 15 | — | 15 | pF |

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per latch.

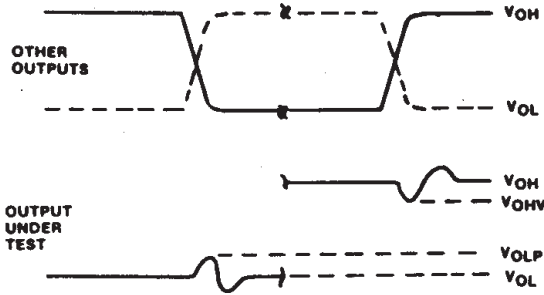
$$P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC} \text{ where } f_i = \text{input frequency}$$

C_L = output load capacitance
V_{CC} = supply voltage.

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CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

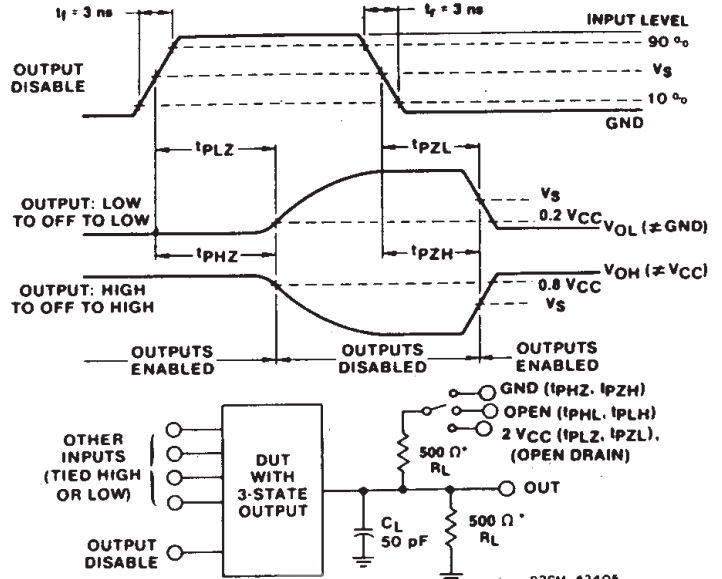
PARAMETER MEASUREMENT INFORMATION



NOTES:

1. V_{OHV} and V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:
PRR \leq 1 MHz, $t_r = 3$ ns, $t_f = 3$ ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μ F CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

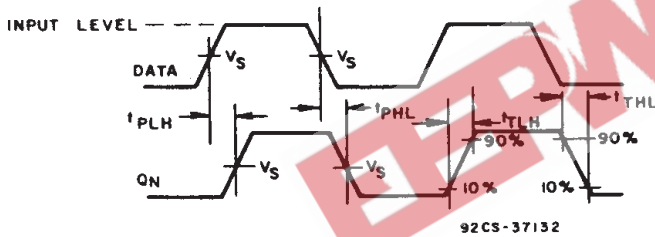


92CM-42405

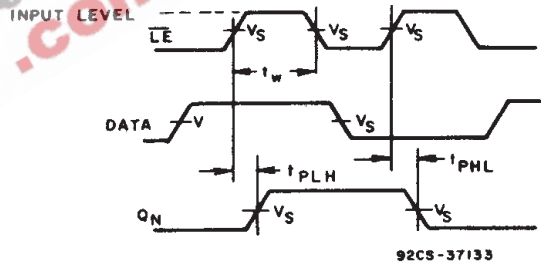
*FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5$ V, $R_L = 1$ k Ω

Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay waveforms and test circuit.



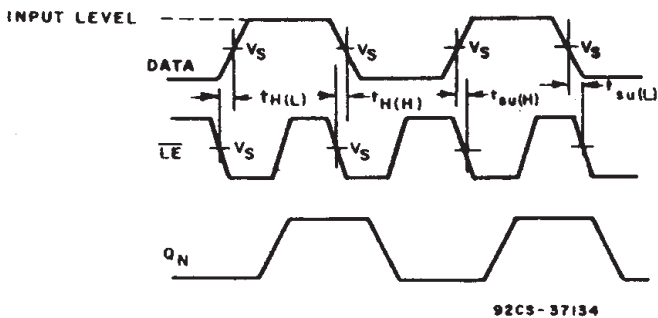
92CS-37132



92CS-37133

Fig. 3 - Data to Qn output propagation delays and output transition times.

Fig. 4 - Latch enable propagation delays.



92CS-37134

Fig. 5 - Latch enable prerequisite times.

| | CD54/74AC | CD54/74ACT |
|---------------------------------|--------------|--------------|
| Input Level | V_{CC} | 3 V |
| Input Switching Voltage, V_S | $0.5 V_{CC}$ | 1.5 V |
| Output Switching Voltage, V_S | $0.5 V_{CC}$ | $0.5 V_{CC}$ |

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