FAIRCHILD SEMICONDUCTOR™

October 1986
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DM74AS240 • DM74AS244
3-STATE Bus Driver/Receiver

General Description

This family of Advance Schottky 3-STATE Bus circuits are designed to provide either bidirectional or unidirectional buffer interface in Memory, Microprocessor, and Communication Systems. The output characteristics of the circuits have low impedance sufficient to drive terminated transmission lines down to 133Ω. The input characteristics of the circuits likewise have a high impedance so it will not significantly load the transmission line. The package contains eight 3-STATE buffers organized with four buffers having a common 3-STATE enable gate. The DM74AS240 and DM74AS244 are eight wide in a 20 pin package, and may be used as a 4 wide bidirectional or eight wide unidirectional. The buffer selection includes inverting and noninverting, with enable or disable 3-STATE control.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Improved switching performance with less power dissipation compared with Schottky counterpart
- Functional and pin compatible with 74LS and Schottky counterpart
- Switching response specified into 500Ω and 50 pF
- Specified to interface with CMOS at $V_{OH} = V_{CC} - 2V$

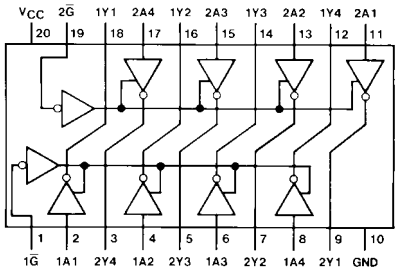
Ordering Code:

Order Number	Package Number	Package Description
DM74AS240WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74AS240N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74AS244WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74AS244N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

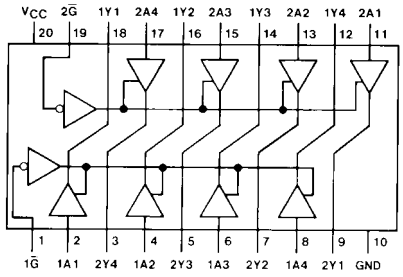
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

DM74AS240



DM74AS244



Function Tables

DM74AS240

Inputs		Output
$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Z

DM74AS244

Inputs		Output
$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

L = LOW Logic Level H = HIGH Logic Level X = Either LOW or HIGH Logic Level Z = High Impedance

Absolute Maximum Ratings(Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	57.0°C/W
M Package	76.0°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−15	mA
I_{OL}	LOW Level Output Current			64	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA					−1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = 4.5V, I_{OH} = −3 mA			2.4	3.2		V
		V_{CC} = 4.5V, I_{OH} = Max			2.4			
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V			V_{CC}−2			
V_{OL}	LOW Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max				0.35	0.55	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V	V_{IN} = 7V	Others			100	µA
I_{IH}	HIGH Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V		Others			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V		AS240, (G, $\overline{G}$), (Control Inputs), DM74AS244 ($\overline{G}$)			−500	µA
				DM74AS244 (A)			−1000	
I_{OZH}	HIGH Level 3-STATE Output Current	V_{CC} = 5.5V, V= 2.7V					50	µA
I_{OZL}	LOW Level 3-STATE Output Current	V_{CC} = 5.5V, V = 0.4V		DM74AS240, DM74AS244			−50	µA
I_O (Note 2)	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V			−50	−115	−150	mA
I_{CC}	DM74AS240 Supply Current	V_{CC} = 5.5V	Outputs HIGH			11	17	mA
			Outputs LOW			51	75	
			3-STATE			24	38	
I_{CC}	DM74AS244 Supply Current	V_{CC} = 5.5V	Outputs HIGH			22	34	mA
			Outputs LOW			60	90	
			3-STATE			34	54	

Note 2: The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS}.

DM74AS240 Switching Characteristics

over recommended operating free air temperature range

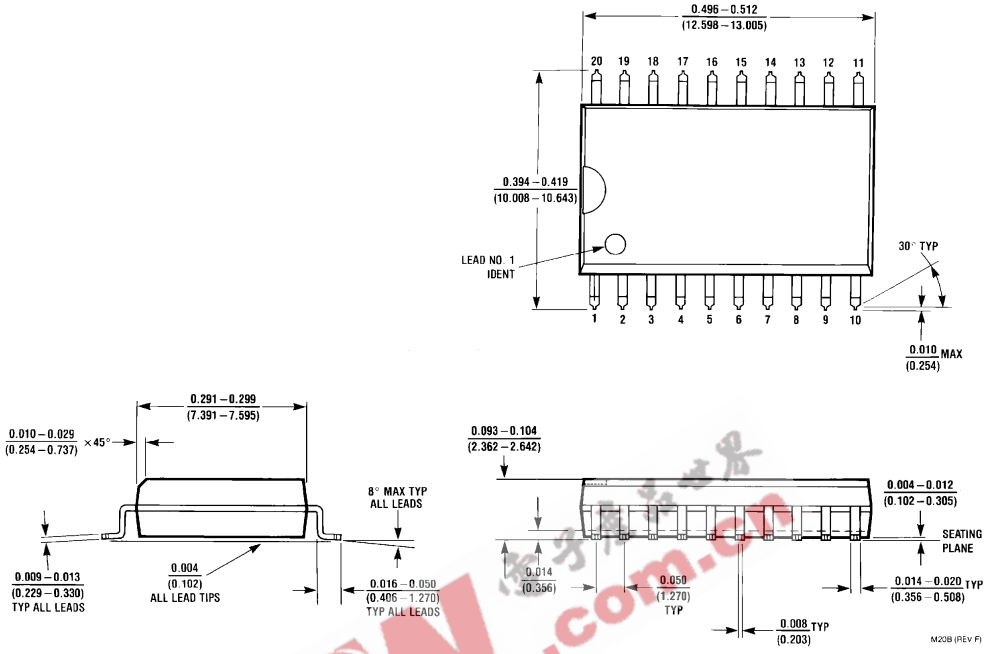
Symbol	Parameter	Conditions	From (Input)	To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	V_{CC} = 4.5V to 5.5V $R_1 = R_2 = 500\Omega$ C_L = 50 pF	A	Y	2	6.5	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		A	Y	2	5.7	ns
t_{PZL}	Output Enable to LOW Level		$\overline{G}$	Y	2	9	ns
t_{PZH}	Output Enable to HIGH Level		$\overline{G}$	Y	2	6.4	ns
t_{PLZ}	Output Disable from LOW Level		$\overline{G}$	Y	2	9.5	ns
t_{PHZ}	Output Disable from HIGH Level		$\overline{G}$	Y	2	5	ns

DM74AS244 Switching Characteristics

over recommended operating free air temperature range

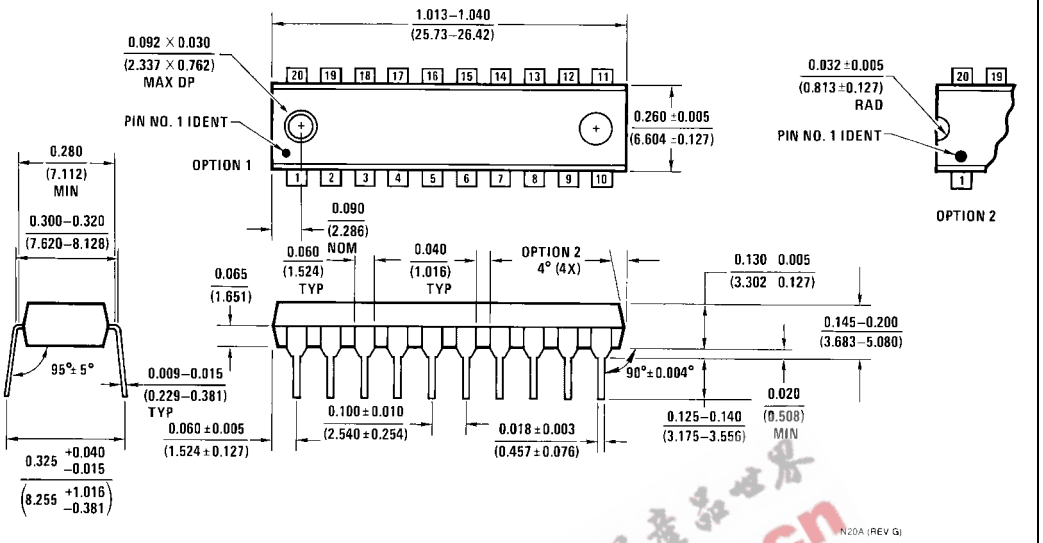
Symbol	Parameter	Conditions	From (Input)	To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	V_{CC} = 4.5V to 5.5V $R_1 = R_2 = 500\Omega$ C_L = 50 pF	A	Y	2	6.2	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		A	Y	2	6.2	ns
t_{PZL}	Output Enable to LOW Level		$\overline{G}$	Y	2	7.5	ns
t_{PZH}	Output Enable to HIGH Level		$\overline{G}$	Y	2	9	ns
t_{PLZ}	Output Disable from LOW Level		$\overline{G}$	Y	2	9	ns
t_{PHZ}	Output Disable from HIGH Level		$\overline{G}$	Y	2	6	ns

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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