

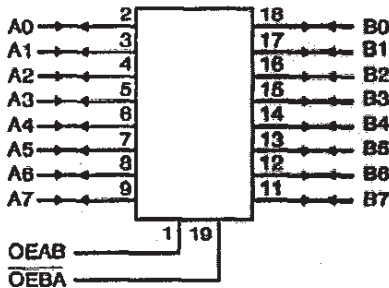


Data sheet acquired from Harris Semiconductor
SCHS296

The CD54FCT623 was not acquired from Harris Semiconductor.

CD54/74FCT623

Octal-Bus Transceiver, 3-State, Non-Inverting



FUNCTIONAL DIAGRAM

Type Features:

- Buffered inputs
- Typical propagation delay:
5.3ns @ VCC = 5V, TA = +25°C, CL = 50pF

The CD54/74FCT623 octal-bus transceiver uses a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

The CD54/74FCT623 is a non-inverting, 3-state, bidirectional transceiver-buffer intended for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus, depending on the logic levels of the Output Enable (OEAB, OEBA) inputs.

The dual Output Enable provision gives these devices the capability to store data by simultaneously enabling OEAB and OEBA. Each output reinforces its input under these conditions, and when all other data sources to the bus lines are at high impedance, both sets of bus lines will remain in their last states.

The CD54/74FCT623 is supplied in the 20-lead small-outline plastic package (M suffix). The package type is operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT623 is also available in chip form (H suffix). This unpackaged device is operable over the -55°C to +125°C temperature range.

Family Features:

- SCR-latchup-resistant BiCMOS process and circuit design
- FCTXXX Types - Speed of bipolar FAST*/AS/S
- 64/48-mA output sink current (commercial/extended industrial)
- Output voltage swing limited to 3.7V @ VCC = 5V
- Controlled output-edge rates
- Input/output isolation to VCC
- BiCMOS technology with low quiescent power

* FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

OUTPUT ENABLE INPUTS		OPERATION
OEBA	OEAB	
L	L	B Data to A Bus
H	H	A Data to B Bus
H	L	Isolation
L	H	B Data to A Bus, A Data to B Bus,

H = High level, L = Low level

To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

MAXIMUM RATINGS, Absolute-Maximum Values:

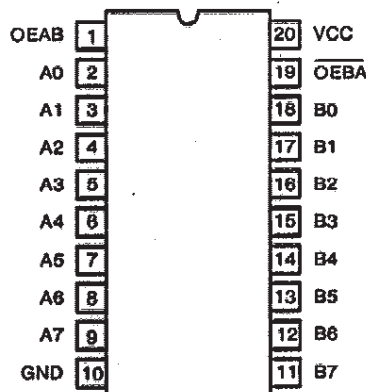
DC SUPPLY-VOLTAGE (VCC)	-0.5V to 6V
DC INPUT DIODE CURRENT, I _{IK} (for V _I < -0.5V)	-20mA
DC OUTPUT DIODE CURRENT, I _{OK} (for V _O < -0.5V)	-50mA
DC OUTPUT SINK CURRENT per Output Pin, I _O	+70mA
DC OUTPUT SOURCE CURRENT per Output Pin, I _O	-30mA
DC VCC CURRENT (I _{CC})	140mA
DC GROUND CURRENT (I _{GND})	528mA
POWER DISSIPATION PER PACKAGE (PD):	
For TA = -55°C to +70°C (PACKAGE TYPE M)	400mW
For TA = +70°C to +125°C (PACKAGE TYPE M)	Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):	
PACKAGE TYPE M	-55°C to +125°C
STORAGE TEMPERATURE (T _{stg})	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum	+265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:

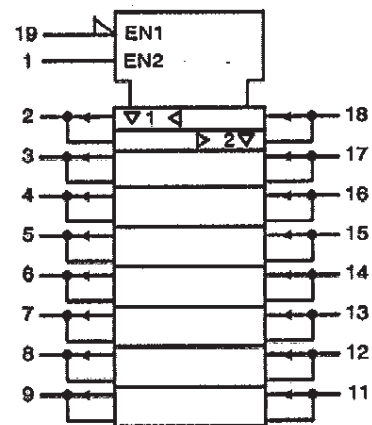
The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC	LIMITS		UNITS
	MIN	MAX	
Supply-Voltage Range, VCC*: CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, V _I	0	VCC	V
DC Output Voltage, V _O	0	≤ VCC	V
Operating Temperature, TA	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V

54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS		VCC (V)	AMBIENT TEMPERATURE (TA)						UNITS
					+25°C		0°C to +70°C		-55°C to +125°C		
		VI (V)	IO (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or VIL	-15	MIN	2.4	-	2.4	-	-	-	V
			-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or VIL	64	MIN	-	0.55	-	0.55	-	-	V
			48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	I _{IH}	VCC		MAX	-	0.1	-	1	-	1	μA
Low-Level Input Current	I _{IL}	GND		MAX	-	-0.1	-	-1	-	-1	μA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	μA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	μA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.

† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

CD54/74FCT623

Switching Specifications FCT Series $t_r, t_f = 2.5\text{ns}, C_L = 50\text{pF}, R_L$ - See Figure 3

PARAMETER	SYMBOL	V_{CC} (V)	+25°C	0°C to +70°C		-55°C to +125°C		UNITS
			TYP	MIN	MAX	MIN	MAX	
Propagation Delays								
Data to Outputs	t_{PLH}, t_{PHL}	5†	5.3	1.5	7	1.5	7.5	ns
Output Disable to Output	t_{PLZ}, t_{PHZ}	5	5.6	1.5	7.5	1.5	10	ns
Output Enable to Output	t_{PZH}, t_{PZL}	5	7.1	1.5	9.5	1.5	10	ns
Power Dissipation Capacitance	$C_{PD}§$	-	48 Typical					pF
Min. (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Figure 1	5	0.5 Typical at +25°C					V
Max. (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Figure 1	5	1 Typical at +25°C					V
Input Capacitance	C_I	-	-	-	10	-	10	pF
Input/Output Capacitance	$C_{I/O}$	-	-	-	15	-	15	pF

† 5V: min. is at 5.5V, max. is at 4.5V.

5V: min. is at 5.25V for 0°C to +70°C, max. is at 4.75V for 0°C to +70°C, typ. is at 5V

§ C_{PD} , measured per function, is used to determine the dynamic power consumption, P_D (per package) = $V_{CC} I_{CC} + \Sigma (V_{CC}^2 f_i C_{PD} + V_O^2 f_o C_L + V_{CC} \Delta I_{CC} D)$ where:

V_{CC} = supply voltage

ΔI_{CC} = flow through current x unit load

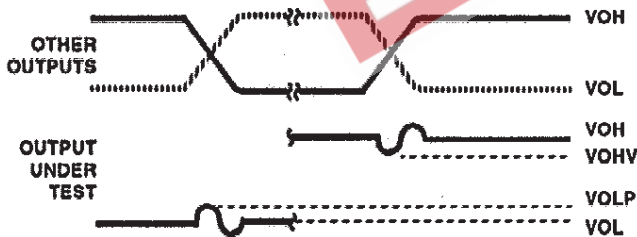
C_L = output load capacitance

D = duty cycle of input high

f_o = output frequency

f_i = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

- V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH} .
- Input pulses have the following characteristics: PRR \leq 1MHz, $t_r = 2.5\text{ns}$, $t_f = 2.5\text{ns}$, skew 1ns.
- R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1 μ F capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 1. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

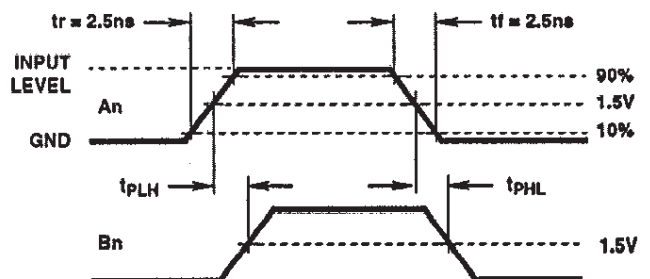
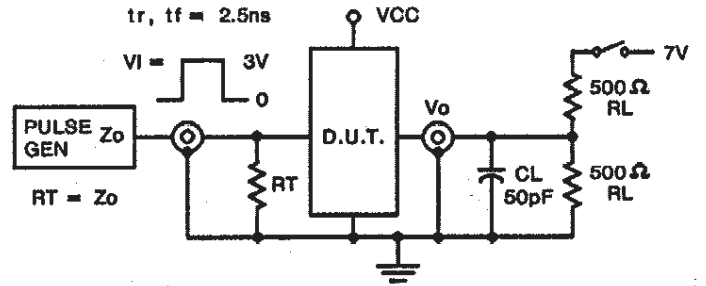
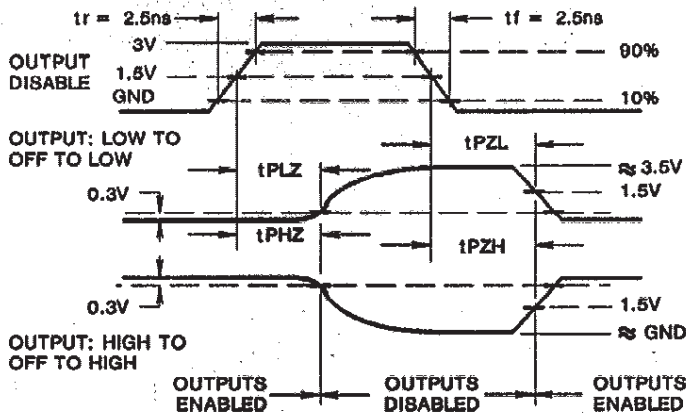


FIGURE 2. PROPAGATION DELAY TIMES



TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 3 - Three-state propagation delay times and test circuit.

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