3.3V, SMD, LV-PECL Oscillator

Model: FCPAXT Series **RoHS Compliant / Pb Free** **Rev. 3/9/2007 Preliminary**

http://www.foxonline.com/need_a_sample.htm

Need a Sample

FEATURES

- 3.3V Operation
- LV-PECL
- Enable/Disable
- Tape and Reel (2,000 pcs. STD)

• PART NUMBER SELECTION

Learn More - Internet Required

Part Number	Model Number	Frequency Stability[1]	Operating Temperature	Frequency Range (MHz)
728-Frequency-xxxxx	**FCP90AXT**	±100PPM	-10 ~ +70 **(ºC)**	12.000 ~ 600.000
745-Frequency-xxxxx	**FCP95AXT**	±50PPM	-10 ~ +70 **(ºC)**	12.000 ~ 600.000

• ELECTRICAL CHARACTERISTICS

PARAMETERS	MAX (unless otherwise noted)
Frequency Range (FO)	12.000 ~ 600.000 MHz
Storage Temperature Range (TSTG)	-55ºC ~ +125ºC
Supply Voltage (VDD)	3.3V ± 5%
Input Current (IDD)	120mA
Output Symmetry (50% Vp-p)	40% ~ 60%
Rise Time (20% ~ 80% Vp-p) (TR)	0.5nS
Fall Time (80% ~ 20% Vp-p) (TF)	0.5nS
Output Voltage (VOL) (VOH)	1.7V 2.2V Min
Output Load	See Recommended Circuit
Start-up Time (Ts)	10mS
Output Disable Time	100nS
Output Enable Time	10mS
Phase Noise (@ 10kHz)	-120dBc/Hz
Phase Jitter (12kHz ~ 20MHz)	5pS RMS
Maximum Soldering Temp / Time	260ºC / 10 Seconds
Moisture Sensitivity Level (MSL)	1

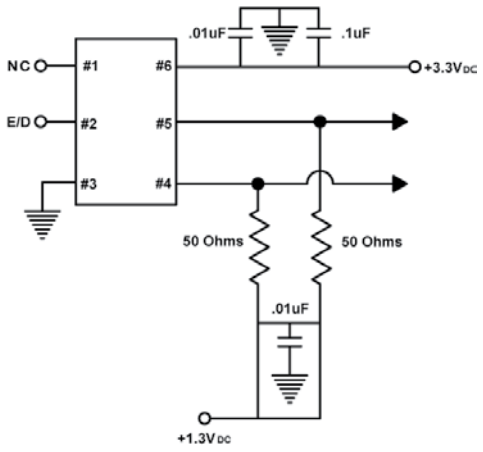
[1] Inclusive of 25ºC tolerance, operating temperature range, input voltage change, load change, aging, shock, vibration.

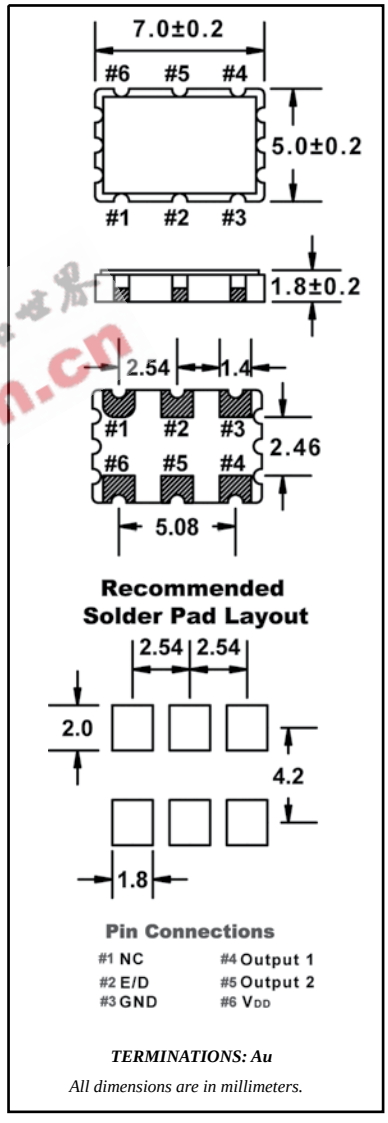
[2] An internal pulldown resistor from pin 2 to pin 3 allows active output if pin 2 is left open.

Note: A 0.01µF bypass capacitor should be placed between VDD (Pin 6) and GND (Pin 3) to minimize power supply line noise.

All specifications subject to change without notice.

FCPAXT Series Recommended Circuit





TERMINATIONS: Au

All dimensions are in millimeters.

• ENABLE / DISABLE FUNCTION[2]

(Pin 2)	OUTPUT (Pin 4, Pin 5)
OPEN	ACTIVE
'1' Level VIH ≥ VDD-1.1V	High Z
'0' Level VIL ≤ VDD-1.6V	ACTIVE