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PRELIMINARY

ICS843246

FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER W/INTEGRATED FANOUT BUFFER

GENERAL DESCRIPTION



The ICS843246 is a Crystal-to-3.3V LVPECL Clock Synthesizer/Fanout Buffer designed for Fibre Channel and Gigabit Ethernet applications and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The output frequency can be set using the frequency select pins and a 25MHz crystal for Ethernet frequencies, or a 26.5625MHz crystal for a Fibre Channel. The low phase noise characteristics of the ICS843246 make it an ideal clock for these demanding applications.

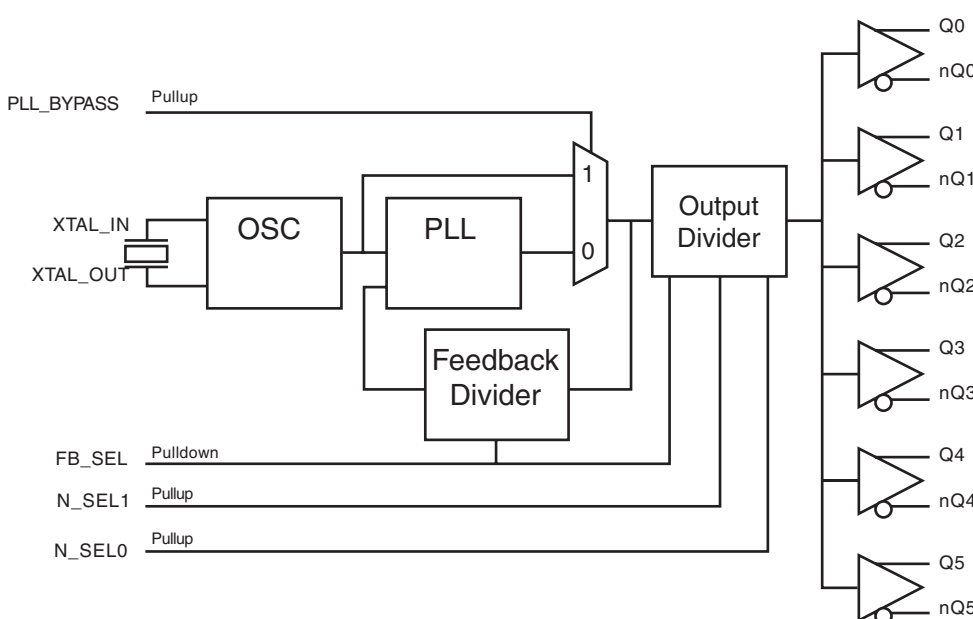
FEATURES

- Six LVPECL outputs
- Crystal oscillator interface
- Output frequency range: 53.125MHz to 333.3333MHz
- Crystal input frequency range: 25MHz to 33.333MHz
- RMS phase jitter at 125MHz, using a 25MHz crystal (1.875MHz to 20MHz): 0.41ps (typical)
- Full 3.3V or 3.3V core, 2.5V output supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard and lead-free RoHS-compliant packages

SELECT FUNCTION TABLE

Inputs			Function		
FB_SEL	N_SEL1	N_SELO	M Divide	N Divide	M/N
0	0	0	20	2	10
0	0	1	20	4	5
0	1	0	20	5	4
0	1	1	20	8	2.5
1	0	0	24	3	8
1	0	1	24	4	6
1	1	0	24	6	4
1	1	1	24	12	2

BLOCK DIAGRAM



PIN ASSIGNMENT

Vcco	1	24	Q3
Vcco	2	23	nQ3
nQ2	3	22	Q4
Q2	4	21	nQ4
nQ1	5	20	Q5
Q1	6	19	nQ5
nQ0	7	18	N_SEL1
Q0	8	17	VEE
PLL_BYPASS	9	16	VEE
VCCA	10	15	N_SELO
VCC	11	14	XTAL_OUT
FB_SEL	12	13	XTAL_IN

ICS843246

24-Lead, 300-MIL SOIC
7.5mm x 15.33mm x 2.3mm
body package
M Package
Top View

24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
body package
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	V _{CCO}	Power		Output supply pins.
3, 4	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
5, 6	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
7, 8	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.
9	PLL_BYPASS	Input	Pullup	Selects between the PLL and crystal inputs as the input to the dividers. When LOW, selects PLL. When HIGH, selects XTAL_IN, XTAL_OUT. LVCMOS / LVTTTL interface levels.
10	V _{CCA}	Power		Analog supply pin.
11	V _{CC}	Power		Core supply pin.
12	FB_SEL	Input	Pulldown	Feedback frequency select pin. LVCMOS/LVTTTL interface levels.
13, 14	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
15, 18	N_SEL0 N_SEL1	Input	Pullup	Output frequency select pin. LVCMOS/LVTTTL interface levels.
16, 17	V _{EE}			Negative supply pin.
19, 20	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.
21, 22	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ



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TABLE 3. CRYSTAL FUNCTION TABLE

Inputs				Function			
XTAL (MHz)	FB_SEL	N_SEL1	N_SEL0	M	VCO (MHz)	N	Output (MHz)
25	0	0	0	20	500	2	250
25	0	0	1	20	500	4	125
25	0	1	0	20	500	5	100
25	0	1	1	20	500	8	62.5
25	1	0	0	24	600	3	200
25	1	0	1	24	600	4	150
25	1	1	0	24	600	6	100
25	1	1	1	24	600	12	50
26.5625	0	1	0	20	531.25	5	106.25
26.5625	1	0	0	24	637.5	3	212.5
26.5625	1	0	1	24	637.5	4	159.375
26.5625	1	1	0	24	637.5	6	106.25
26.5625	1	1	1	24	637.5	12	53.125
30	0	0	0	20	600	2	300
30	0	0	1	20	600	4	150
30	0	1	0	20	600	5	120
30	0	1	1	20	600	8	75
31.25	0	0	0	20	625	2	312.5
31.25	0	0	1	20	625	4	156.25
31.25	0	1	0	20	625	5	125
31.25	0	1	1	20	625	8	78.125
33.3333	0	0	0	20	666.6667	2	333.3333
33.3333	0	0	1	20	666.6667	4	166.6667
33.3333	0	1	0	20	666.6667	5	133.3333
33.3333	0	1	1	20	666.6667	8	83.3333



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to $V_{CC} + 0.5V$
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	
24 Lead SOIC	50°C/W (0 lfpm)
24 Lead TSSOP	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			107		mA
I_{CCA}	Analog Supply Current			7		mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $V_{CCO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			107		mA
I_{CCA}	Analog Supply Current			7		mA

TABLE 4C. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $V_{CCO} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	FB_SEL	$V_{CC} = V_{IN} = 3.465V$		150	μA
		PLL_BYPASS, N_SEL0, N_SEL1	$V_{CC} = V_{IN} = 3.465V$		5	μA
I_{IL}	Input Low Current	FB_SEL	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		μA
		PLL_BYPASS, N_SEL0, N_SEL1	$V_{CC} = 3.465V, V_{IN} = 0V$	-150		μA



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TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $V_{CCO} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} - 2V$.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		25		33.333	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pf parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		53.125		333.33	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random)	125MHz, Integration Range: 1.875MHz - 20MHz		0.41		ps
$t_{sk(o)}$	Output Skew; NOTE 1, 2			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		380		ps
odc	Output Duty Cycle			50		%
t_{LOCK}	PLL Lock Time				1	ms

See Parameter Measurement Information section.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential crossing points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $V_{CCO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		53.125		333.33	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random)	125MHz, Integration Range: 1.875MHz - 20MHz		0.41		ps
$t_{sk(o)}$	Output Skew; NOTE 1, 2			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		360		ps
odc	Output Duty Cycle			50		%
t_{LOCK}	PLL Lock Time				1	ms

See Parameter Measurement Information section.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential crossing points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.



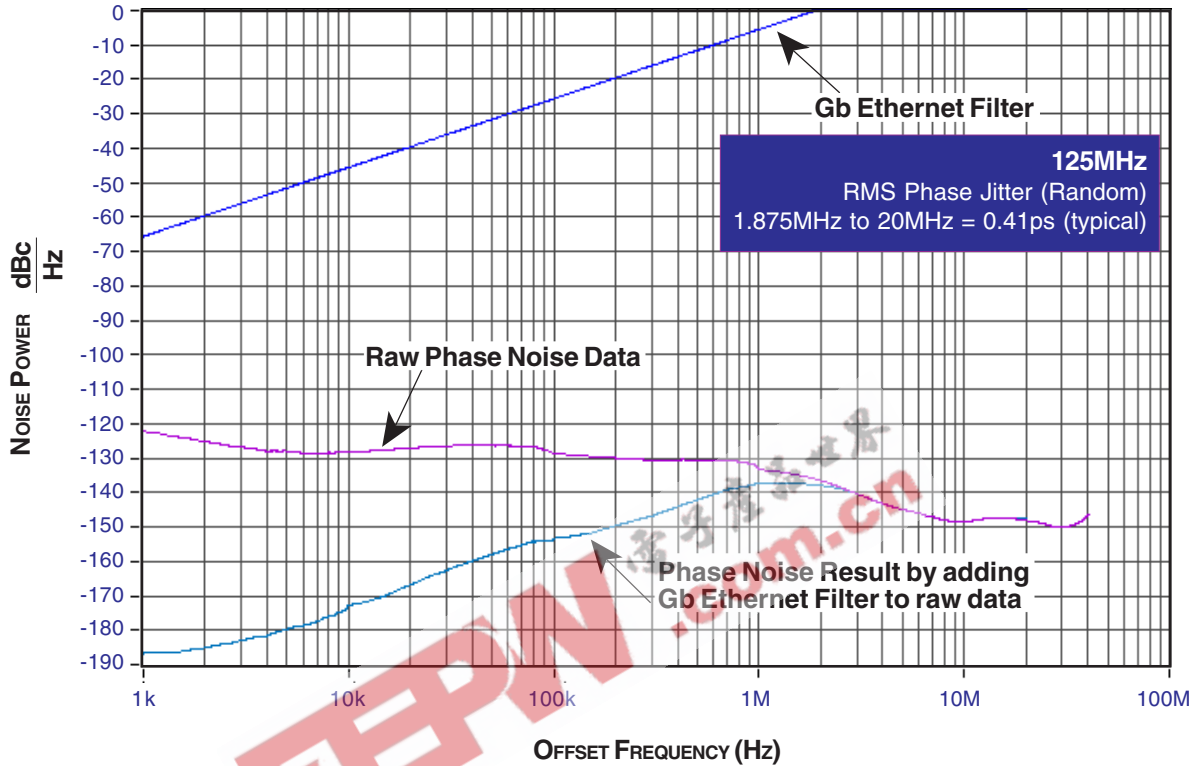
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TYPICAL PHASE NOISE AT 125MHz @ 3.3V





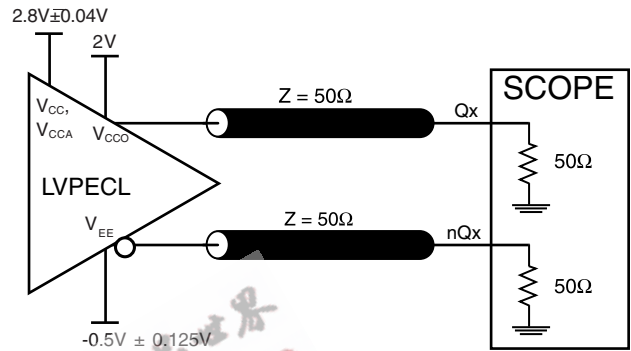
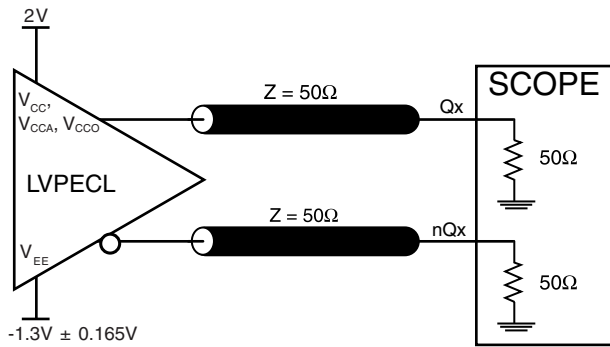
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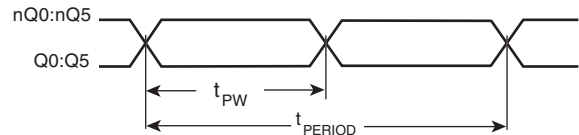
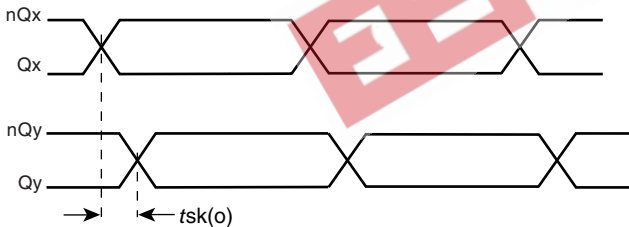
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PARAMETER MEASUREMENT INFORMATION



3.3V OUTPUT LOAD AC TEST CIRCUIT

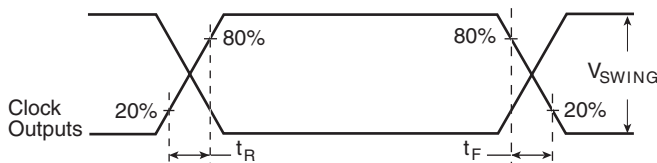
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT SKEW

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



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APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843246 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} , V_{CCA} and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu F$ and a $.01\mu F$ bypass capacitor should be connected to each V_{CCA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

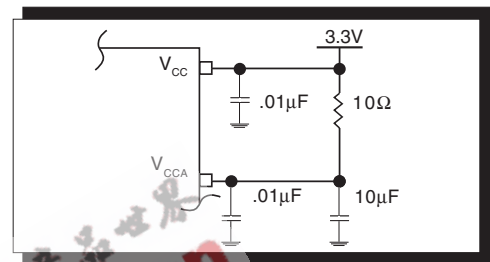


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843246 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2*

below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

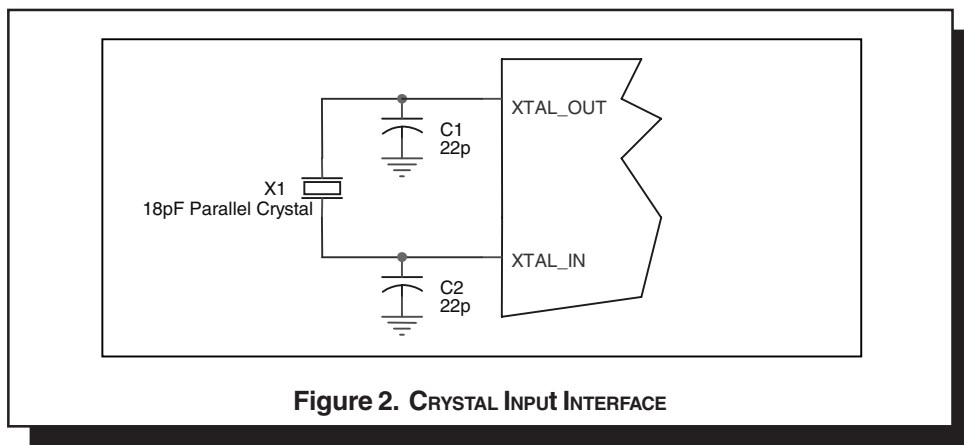


Figure 2. CRYSTAL INPUT INTERFACE



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RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are

designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

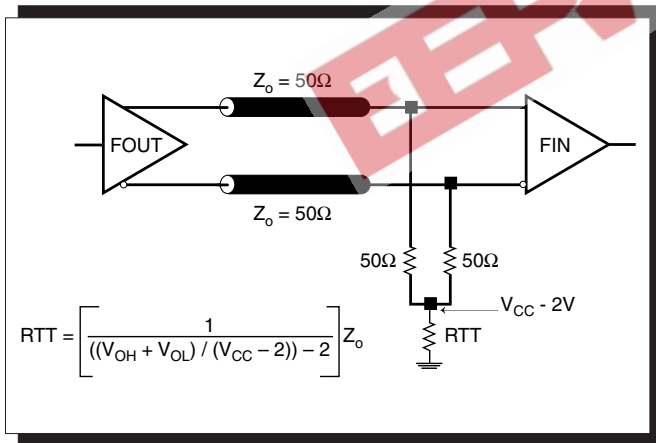


FIGURE 3A. LVPECL OUTPUT TERMINATION

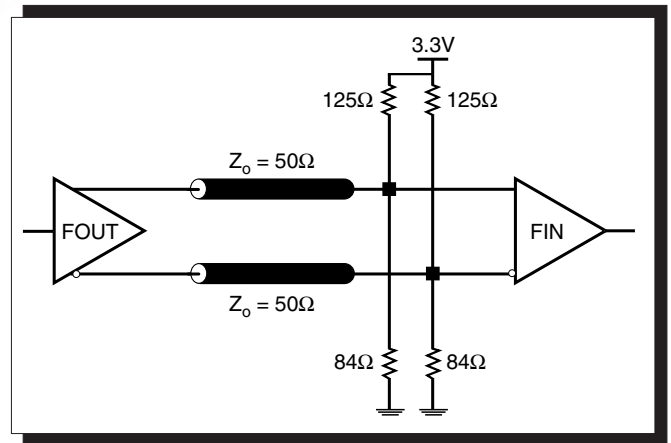


FIGURE 3B. LVPECL OUTPUT TERMINATION



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TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC} = 2.5V$, the $V_{CC} - 2V$ is very

close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in Figure 4C.

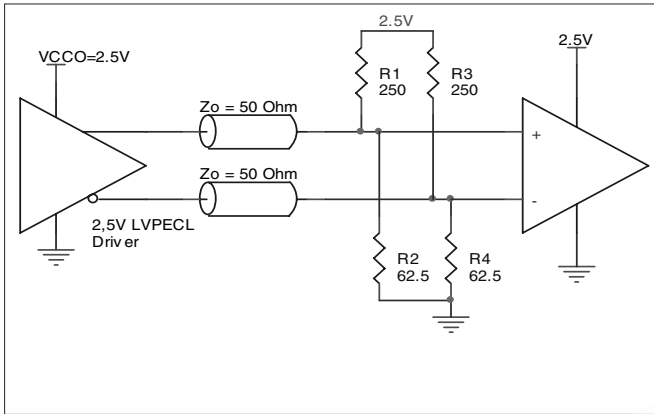


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

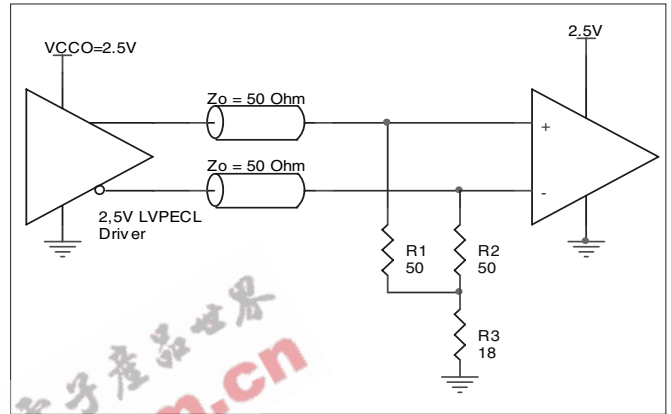


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

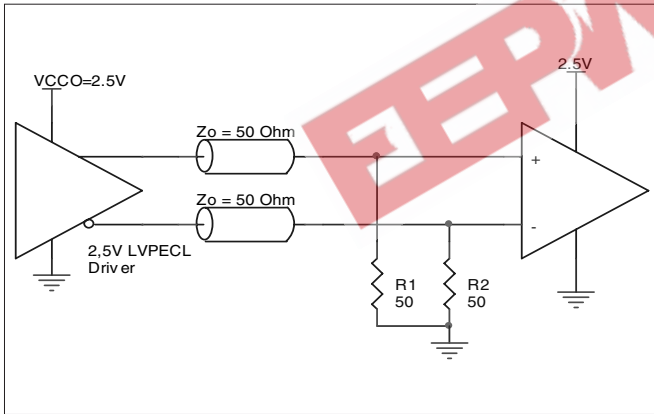


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843246. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843246 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 107mA = 370.75mW$
- Power (outputs)_{MAX} = **30.2mW/Loaded Output pair**
If all outputs are loaded, the total power is $6 * 30mW = 180mW$

Total Power_{MAX} (3.465V, with all outputs switching) = $370.75mW + 180mW = 550.75mW$

2. Junction Temperature.

Junction temperature, T_j, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 43°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.551W * 43^\circ C/W = 93.7^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 24-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	50°C/W	43°C/W	38°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 5.

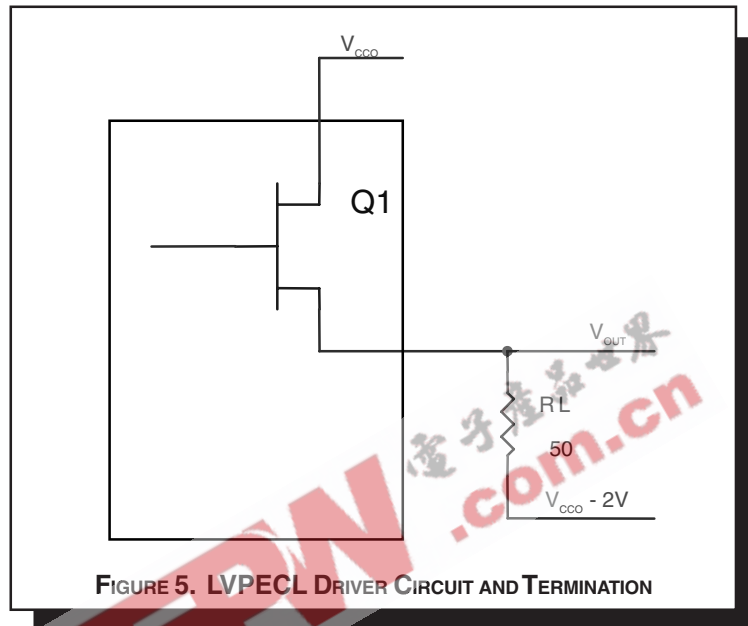


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 0.9V$
 $(V_{CCO_MAX} - V_{OH_MAX}) = 0.9V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.7V$
 $(V_{CCO_MAX} - V_{OL_MAX}) = 1.7V$

Pd_H is power dissipation when the output drives high.
 Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = $Pd_H + Pd_L = 30mW$



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RELIABILITY INFORMATION

TABLE 8A. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	50°C/W	43°C/W	38°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TABLE 8B. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS843246 is: 3863



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PACKAGE OUTLINE - M SUFFIX FOR 24 LEAD SOIC

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

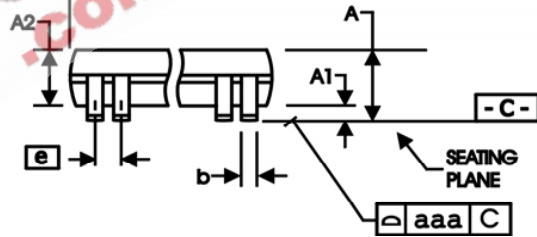
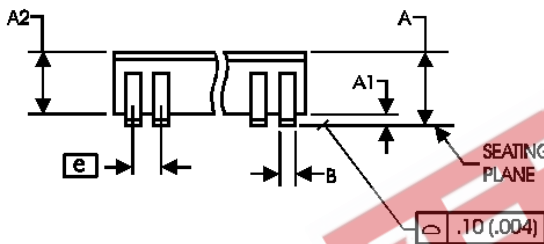
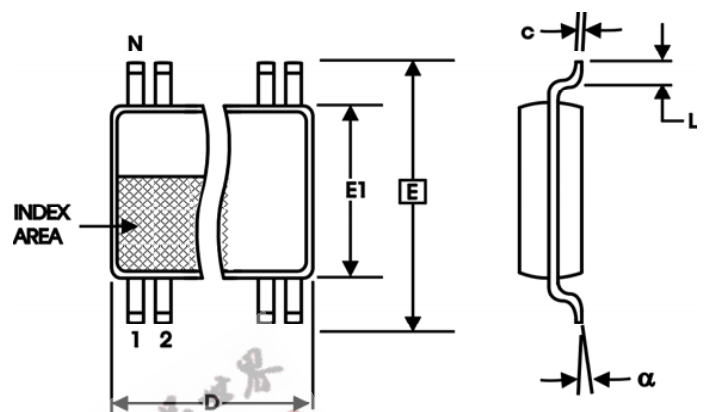
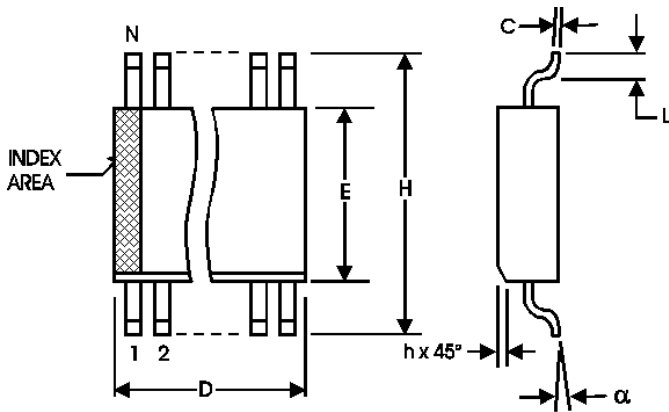


TABLE 9A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	15.20	15.85
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

TABLE 9B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153



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PRELIMINARY

ICS843246

FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL
FREQUENCY SYNTHESIZER W/INTEGRATED FANOUT BUFFER

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843246AM	TBD	24 Lead SOIC	tube	0°C to 70°C
ICS843246AMT	TBD	24 Lead SOIC	1000 tape & reel	0°C to 70°C
ICS843246AMLF	TBD	24 Lead "Lead-Free" SOIC	tube	0°C to 70°C
ICS843246AMLFT	TBD	24 Lead "Lead-Free" SOIC	1000 tape & reel	0°C to 70°C
ICS843246AG	ICS843246AG	24 Lead TSSOP	tube	0°C to 70°C
ICS843246AGT	ICS843246AG	24 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS843246AGLF	TBD	24 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS843246AGLFT	TBD	24 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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