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FEBRUARY 1994
ADVANCE INFORMATION
D.S. 3931 1.5

SP5654

2.7GHz 3–WIRE BUS CONTROLLED SYNTHESISER

The SP5654 is a single chip frequency synthesiser designed for satellite TV tuning systems. It is a programming variant of the SP5655 allowing the design of one tuner with either I^2C bus or a 3–wire bus format depending on which device is inserted. The device when used with a varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide–by–16 prescaler with its own preamplifier and a 14/15 bit programmable divider controlled by a serially loaded data register. Four independently programmable open collector outputs are included. The device contains five modes of operation each compatible with Toshiba 18 and 19 bit software.

The comparison frequencies are obtained from a crystal controlled on–chip oscillator typically operating at 4MHz. The comparator has a charge pump output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

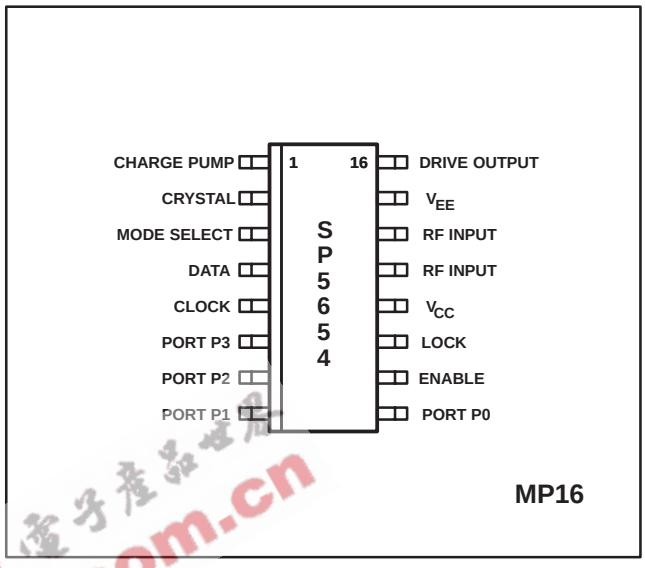


Fig. 1 Pin connections – top view

FEATURES

- Complete 2.7GHz Single Chip System
- High Sensitivity RF Input
- Low power Consumption (5V, 30mA)
- On–Chip Oscillator with 1kΩ negative resistance
- On chip oscillator start–up circuit
- Programming Compatible with Toshiba TD6380, TD6381 and TD6382#
- Pin compatible with SP5655#
- 5 Modes of Operation with different step sizes, see Table 1; each selectable with 18 or 19 bit transmission length.
- Single Port 18/19 Bit Serial Data Entry
- Auto select for Data transmission length, 18 or 19
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- Charge Pump Disable
- Four Controllable Outputs
- ESD Protection †

See notes on pin and programming compatibility

† Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

ORDERING INFORMATION

SP5654/KG/MPAS (Tubes)
SP5654/KG/MPAD (Tape and Reel)

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}=+4.5V to +5.5V. Reference frequency =4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	12		30	40	mA	Typical applies to V_{CC} = 5V
Prescaler Input Voltage		13, 14	12.5		300	mV_{rms}	300MHz to 2GHz sinewave.
			40		300	mV_{rms}	120MHz & 2.7GHz See Fig.6.
Prescaler Input Impedance Input Capacitance		13, 14		50 2		Ω pF	
Data Clock and Enable							
High Level Input Voltage		4, 5, 10	3		V_{CC}	V	
Low Level Input Voltage		4, 5, 10	0		1.5	V	
High Level Input Current		4, 5, 10			10	µA	V_{IN}=5.5V V_{CC}=5.5V
Low Level Input Current		4, 5, 10			–10	µA	V_{IN}=0V V_{CC}=5.5V
Input Hysteresis		4, 5, 10		0.8		V	
Clock Rate		5			500	kHz	
Timing Information							
Data Setup Time	t_{SU}	4	300			ns	See Fig.4
Data Hold Time	t_{HD}	4	600			ns	See Fig. 4
Enable Setup time	t_{ES}	10	300			ns	See Fig. 4
Enable Hold Time	t_{EH}	10	600			ns	See Fig. 4
Clock–to–Enable Time	t_{CE}	10	300			ns	See Fig. 4
Clock Low Period	t_{LO}	5	600			ns	See Fig. 4
Clock High Period	t_{HI}	5	600			ns	See Fig. 4
Mode Select							
High Level Input Current		3			700	µA	V_{IN}=5.5V V_{CC}=5.5V
Low Level Input Current		3			–700	µA	V_{IN}=0V V_{CC}=5.5V
Charge Pump Output Current		1		±150		µA	V pin 1 = 2.0V, device 'out of lock'
Charge Pump Output Current		1		±50		µA	V pin 1 = 2.0V, device 'locked'
Charge Pump Output Leakage Current		1			±5	nA	V pin 1 = 2.0V, charge pump disabled
Charge Pump Drive Output Current		16	1			mA	V pin 16 = 0.7V
Charge Pump Amplifier Gain				6400			Pin 18 Current = 100µA
Oscillator Temperature Stability					2	ppm/°C	
Oscillator Stability with Supply Voltage					2	ppm/V	
Recommended Crystal Series Resistance			10		200	Ω	"Parallel resonant crystal." Figure quoted is under all conditions including start up.
Crystal Oscillator Drive Level		2		80		mV p–p	
Crystal Oscillator Negative Resistance		2	750			Ω	Includes temperature and process tolerances
Reference Crystal Frequency		2	4		8	MHz	
External Reference input Frequency		2	2		16	MHz	AC coupled sinewave
External Reference input Amplitude		2	400		1000	$mV_{p–p}$	AC coupled sinewave

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= –20°C to +80°C, V_{CC}= +4.5V to +5.5V. Reference frequency =4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Ports and Lock output							
Sink Current		6–9, 11	10			mA	V_{out}=0.7V
Lock Leakage Current		11			10	µA	V_{out}=V_{CC}
Port Leakage Current		6–9			10	µA	V_{out}=13.2V
Varactor Drive Amp Disable		10	–50			µA	V_{pin} 10 < 0V. Current sourced from device
Charge Pump Disable		4	–50			µA	V_{pin} 4 < 0V. Current sourced from device
Test Mode Enable		5	–50			µA	V_{pin} 5 < 0V. Current sourced from device. See Table 2

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE}=0V

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Supply voltage	12	–0.3	7	V	
Prescaler input voltage	13, 14		2.5	Vp–p	
Prescaler DC offset	13, 14	–0.3	V_{CC}+0.3	V	
Port voltage	6–9	–0.3	14	V	Port in off state
		–0.3	6	V	Port in on state
Total port output current	6–9		50	mA	
Loop amplifier DC offset	1, 16	–0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	–0.3	V_{CC}+0.3	V	
3–wire bus inputs	4, 5, 10	–0.7	6	V	
Mode select input	3	–0.3	V_{CC}+0.3	V	
Lock output voltage	11	–0.3	V_{CC}+0.3	V	
Lock output current	11		15	mA	
Storage temperature		–55	+150	°C	
Junction temperature			+150	°C	
MP16 thermal resistance, chip–to–ambient			111	°C/W	
MP16 thermal resistance, chip–to–case			41	°C/W	
Power consumption			220	mW	All ports off
ESD protection	All	4		kV	MIL STD 883 TM 3015

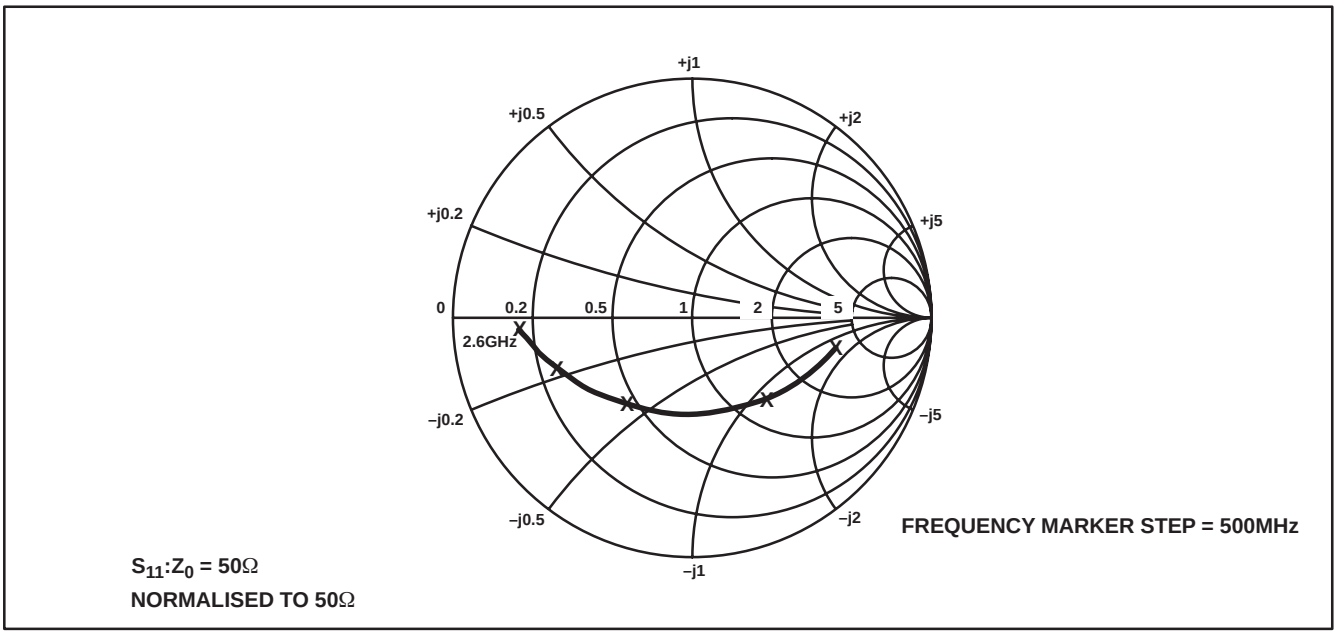


Fig. 2 Typical input impedance

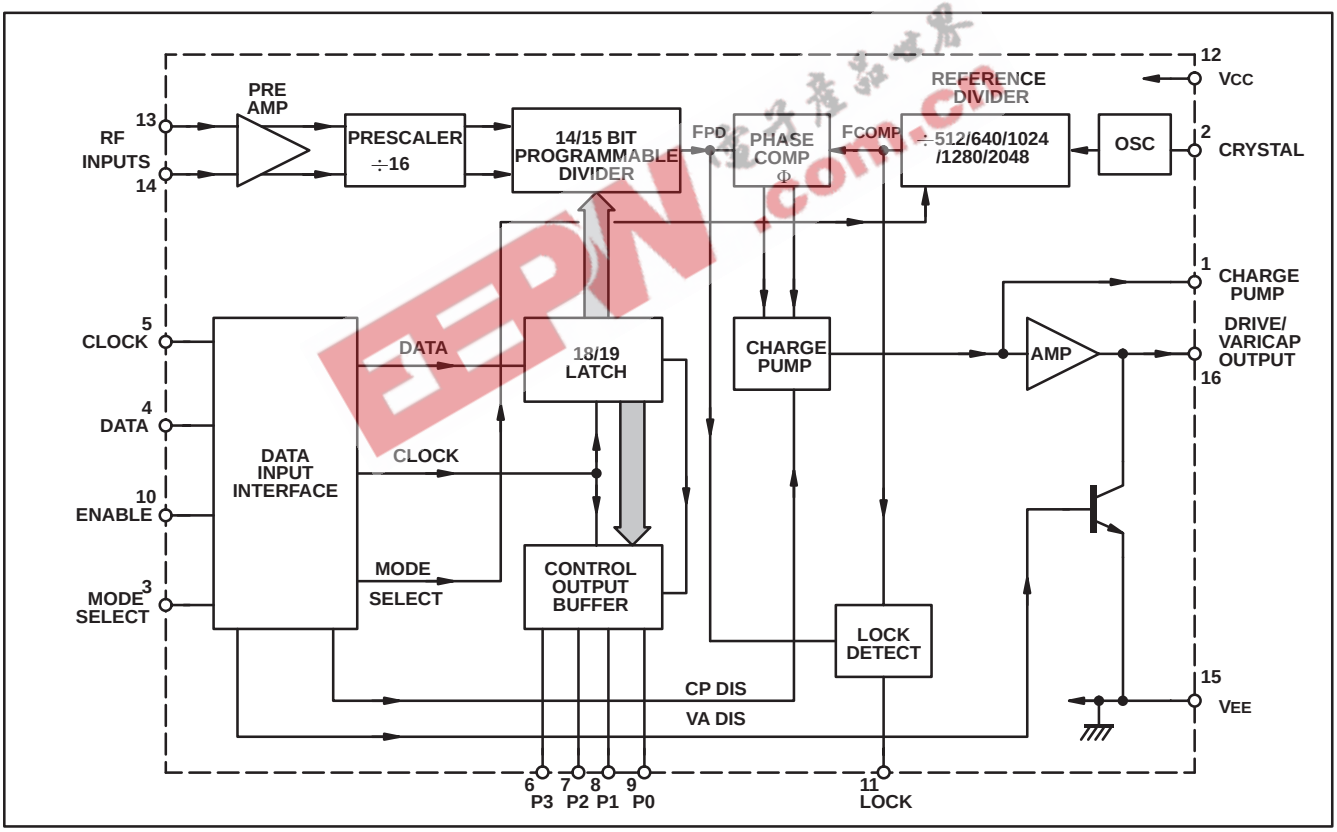


Fig. 3 Block diagram

FUNCTIONAL DESCRIPTION

The SP5654 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor, to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard data, clock and enable three–wire bus. The data load consists of a single word, which contains the frequency and port information, and is only transferred to the internal data shift register during an enable high period. The clock is disabled during low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tuning facility for digital AFC etc.

The device has 5 modes of operation, as defined in Table 1, and each of these modes can accept either 18–bit or 19–bit data entry. The format of the data entry is shown in Fig. 4, and consists of 4–bits for port switching, plus 14/15 bits to control the 15–bit programmable divider. For 18–bit data entry (4+14), the MSB of the 15–bit programmable divider is internally set to logic '0' effectively making the divider 14–bits. The device recognises the data entry as 18–bit when a falling edge at the enable input occurs during the 18th clock period. The device associates falling enable edges during the 19th clock period with 19–bit data entry. A falling edge at the enable input before the 18th clock period constitutes invalid data entry to the device.

The frequency is set by first selecting the required mode of operation as detailed in Table 1, and then by loading the programmable divider with the required 14/15–bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency to the internally generated comparison frequency, F_{COMP}.

The comparison frequency F_{COMP} is obtained by dividing the output of the on–chip crystal controlled oscillator. The crystal frequency generally used is 4MHz, giving an F_{COMP} of 7.8125kHz in mode 4, which when multiplied back up to the LO gives a minimum step size of 125kHz.

The programmable divider is preceded by an input RF preamplifier and high speed low radiation prescaler. The preamplifier is arranged to be self oscillating, so giving excellent input sensitivity. The input impedance and sensitivity are shown in Fig. 2 and 6 respectively.

The device contains a lock detect circuit which generates a flag when the loop has attained lock. The 'in lock' condition is indicated by a high impedance state.

The charge pump current is initially set to ±150μA. When the device attains frequency lock, the charge pump current is switched to ±50μA, so improving the local oscillator short term jitter.

The device also contains four general purpose open collector output ports P0–P3. These outputs are each capable of sinking a minimum of 10mA, when the appropriate bits P0–P3 of the programming data, see Fig. 4 are set to a logic '1'.

PIN and PROGRAMMING COMPATIBILITY

The SP5654 may be used in SP5655 applications which require 3–wire bus as opposed to I^2C bus data format. In SP5655 applications where the reference crystal is grounded to pin 3, a small modification is required to ground the crystal as shown in Fig. 5.

Appropriate connections must also be to the mode select input (see Table 1). For each mode of operation, the SP5654 is programming and step size compatible with Toshiba devices as shown in Table 3.

TEST FEATURES

Charge pump disable

The charge pump may be disabled by sourcing current from the data input, i.e. by forcing a negative input voltage.

Varactor line disable

The charge pump amplifier drive output may be disabled by sourcing current from the enable input, i.e. by forcing a negative voltage.

Device test mode

Further test modes can be invoked by sourcing current from the clock input, i.e. by forcing a negative input voltage. These test modes when invoked are determined by the data held in the P1, P2 and P3 internal registers as detailed in Table 2.

MODE	'MODE SELECT' INPUT VOLTAGE	PROGRAMMABLE DIVIDER BIT LENGTH	REFERENCE DIVIDER RATIO	*FREQUENCY STEP SIZE (kHz)	*MAXIMUM OPERATING FREQUENCY (GHz)	
					14 bit	15 bit
4	0.85 V_{CC} – V_{CC}	14/15	512	125	2.0479	2.7000
3	0.65 V_{CC} – 0.75V_{CC} #	14/15	1280	50	0.8191	1.6383
2	OPEN CIRCUIT	14/15	1024	62.5	1.0239	2.0479
1	0.25 V_{CC} – 0.35V_{CC} †	14/15	2048	31.25	0.5119	1.0239
0	0 – 0.15 V_{CC}	14/15	640	100	1.6383	2.7000

*When used with a 4MHz crystal

Selected by connecting a 15kΩ resistor to V_{CC}

† Selected by connecting a 15kΩ resistor to V_{EE}

Table 1. Modes of operation

Test Mode	P1	P2	P3	Test Mode Description
0	0	0	0	Charge pump down 170µA
1	0	0	1	Charge pump up 170µA
2	1	0	0	Charge pump down 50µA
3	1	0	1	Charge pump up 50µA
4	d	1	0	F_{COMP} to P2; F_{PD}/2 to P3; Lock output switched to out of lock condition
5	d	1	1	Lock output switched to inlock condition

These test modes are invoked by taking the clock input below V_{EE}
d=don't care

Table 2 Test mode options

MODE	COMPATIBILITY	
	18 Bit Data entry	19 Bit Data entry
4	TD6380 plus ÷2 prescaler	TD6382 plus ÷4 prescaler
3	None	TD6381
2	TD6380	TD6382 plus ÷2 prescaler
1	None	TD6382
0	None	TD6381 plus ÷2 prescaler

Table 3. Programming compatibilities

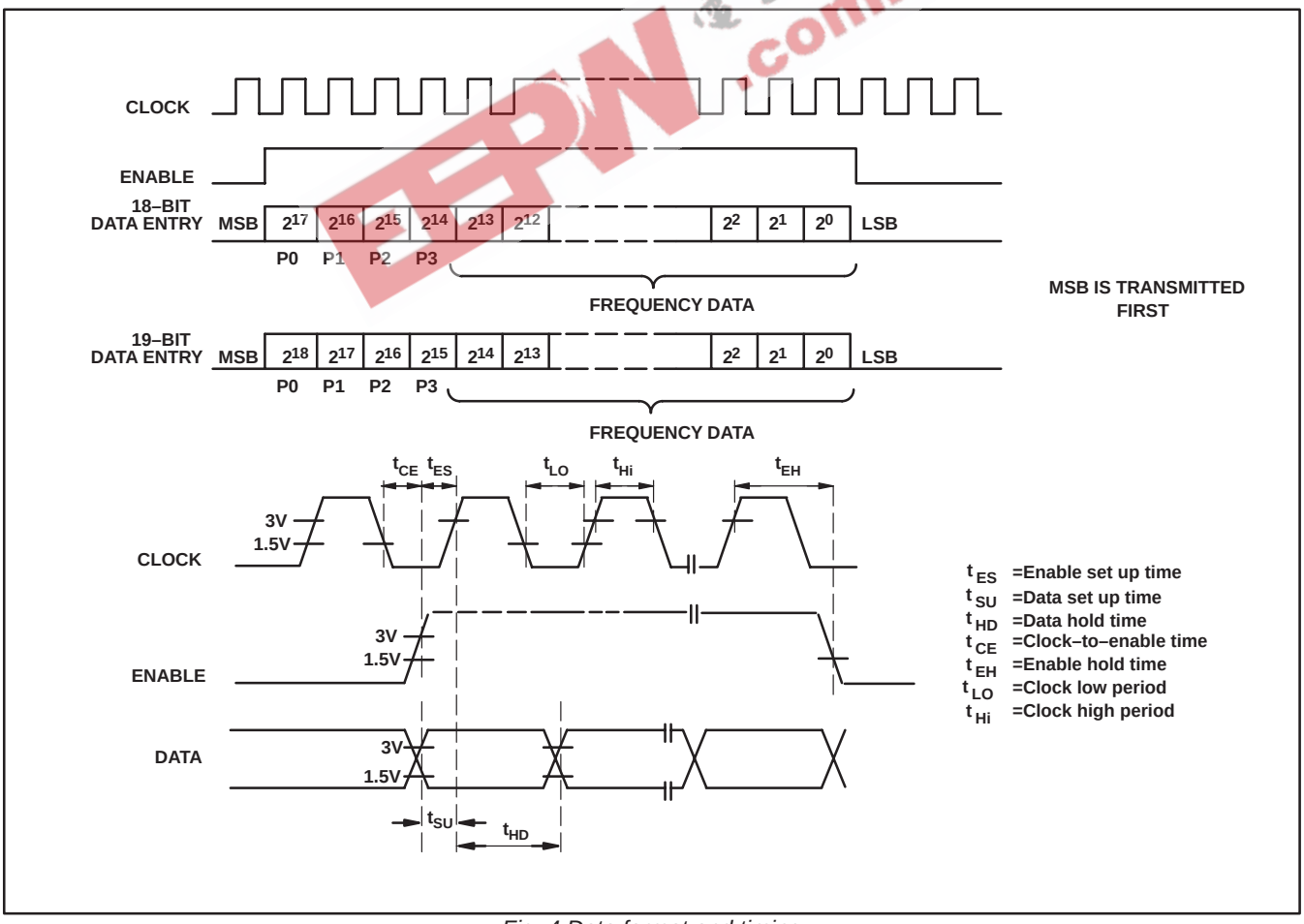


Fig. 4 Data format and timing

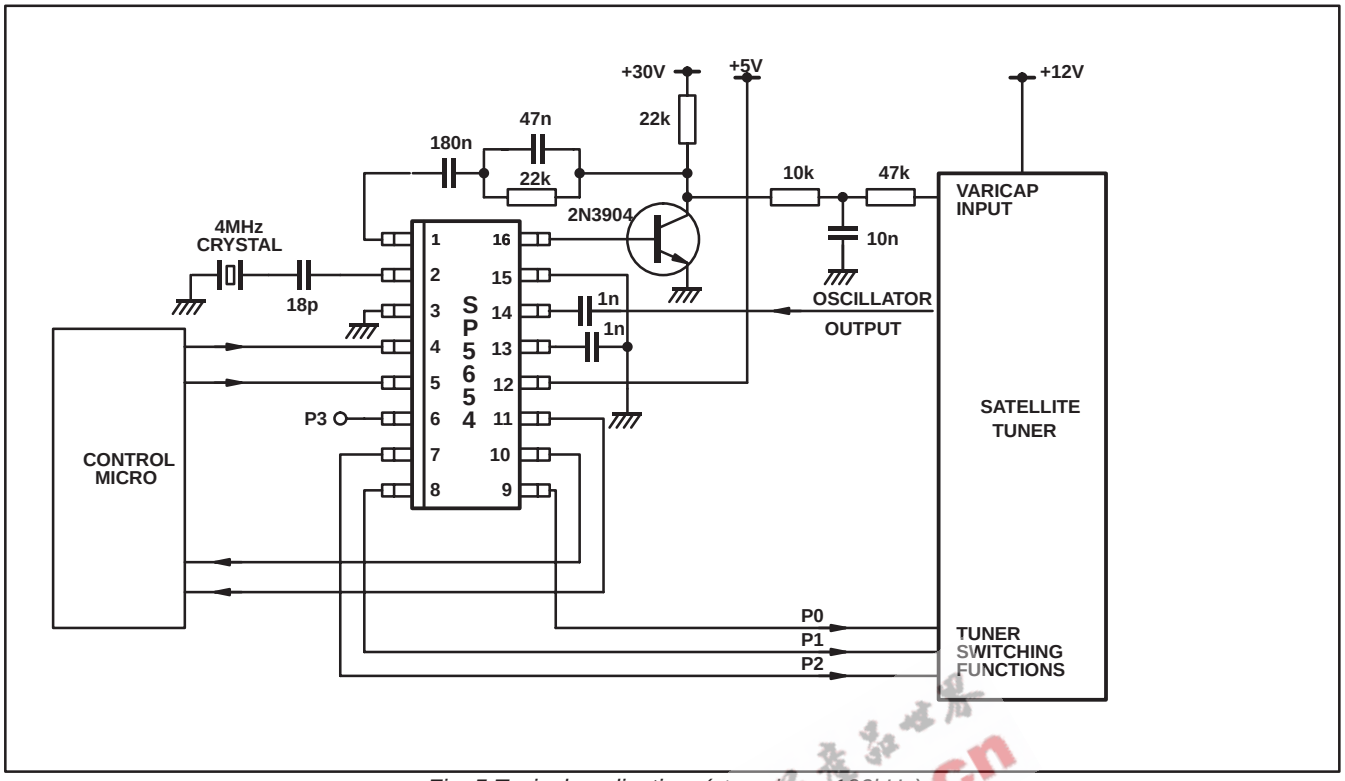


Fig. 5 Typical application (step size = 100kHz)

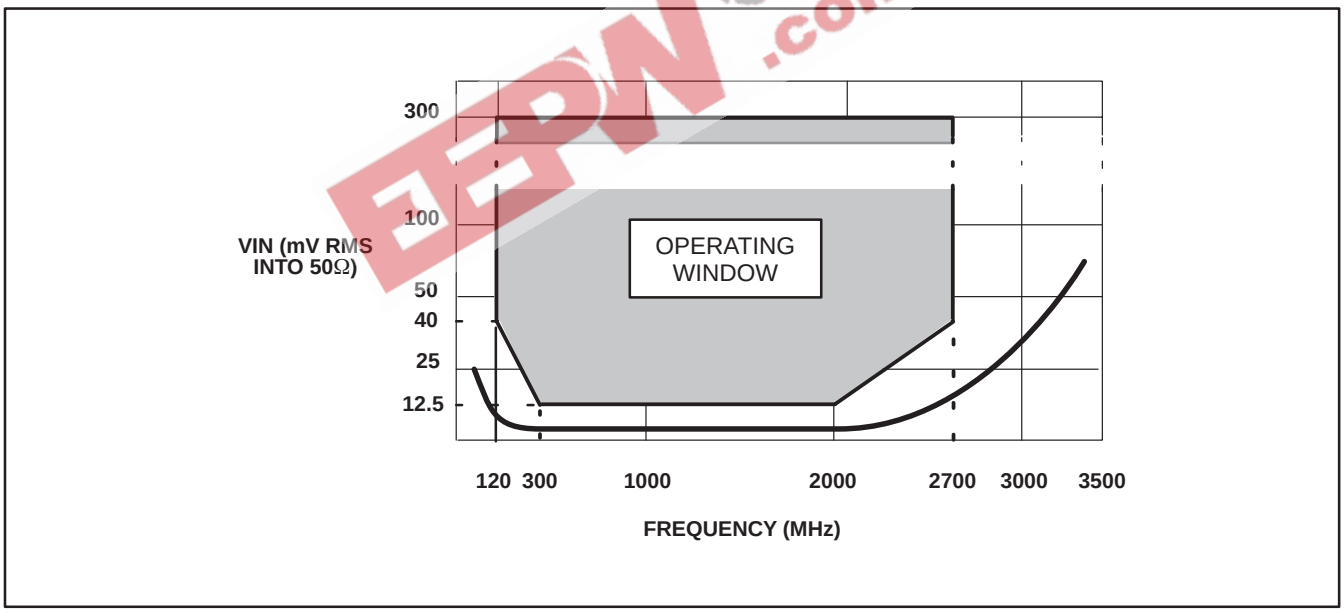
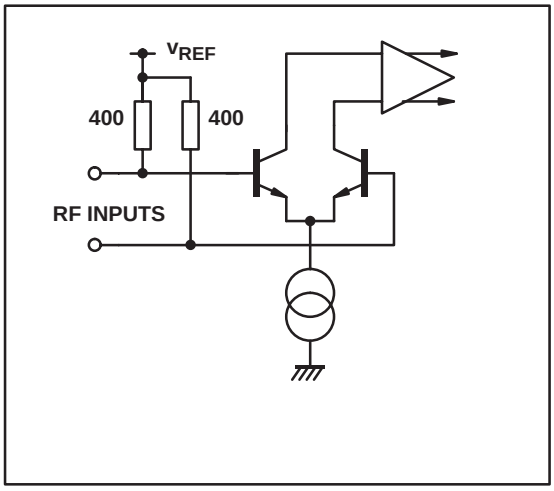
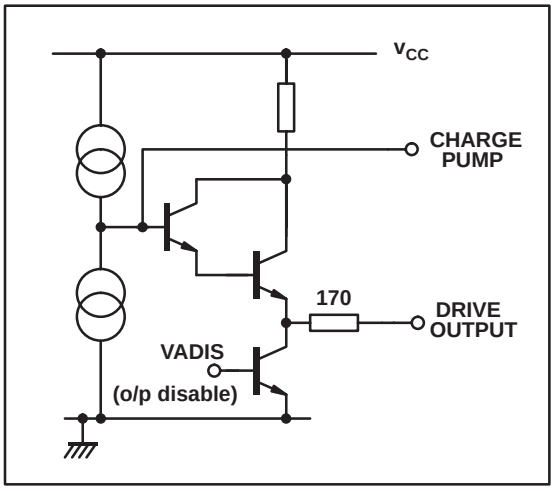


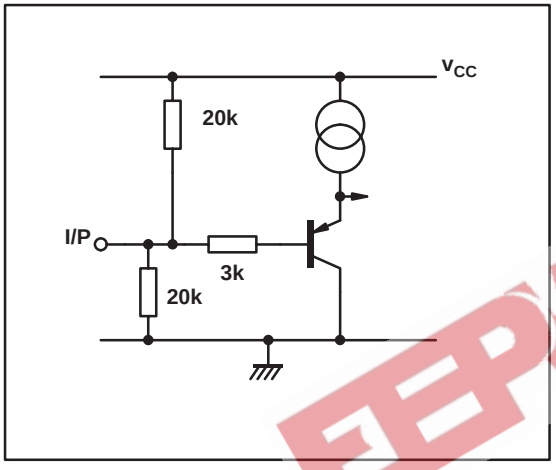
Fig. 6 Typical input sensitivity



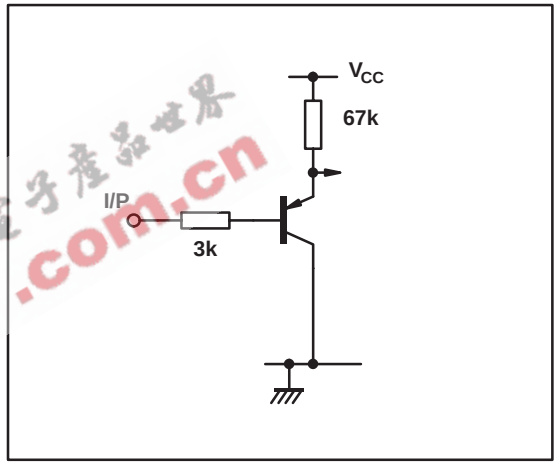
RF inputs



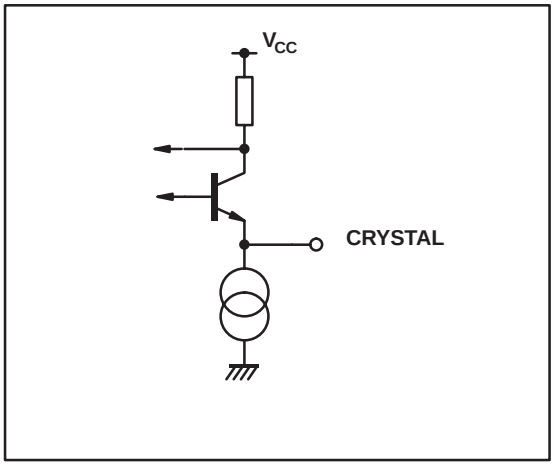
Loop amplifier



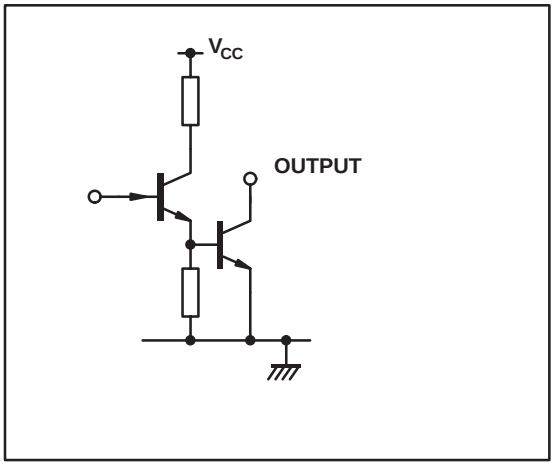
Mode select input



Data, Clock, Enable inputs



Reference oscillator

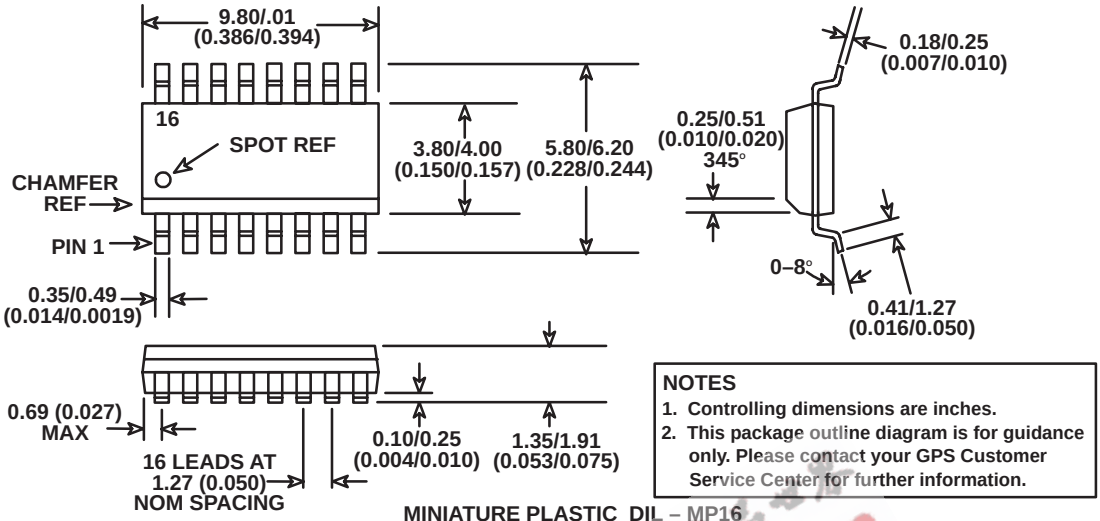


Output ports P0–P3 and lock output

Fig. 7. Input/Output interface circuits

PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information please contact your local Customer Service Centre.



NOTES

1. **Controlling dimensions are inches.**
2. **This package outline diagram is for guidance only. Please contact your GPS Customer Service Center for further information.**

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