PRELIMINARY

Integrated Circuit Systems, Inc.

ICS843204I

FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

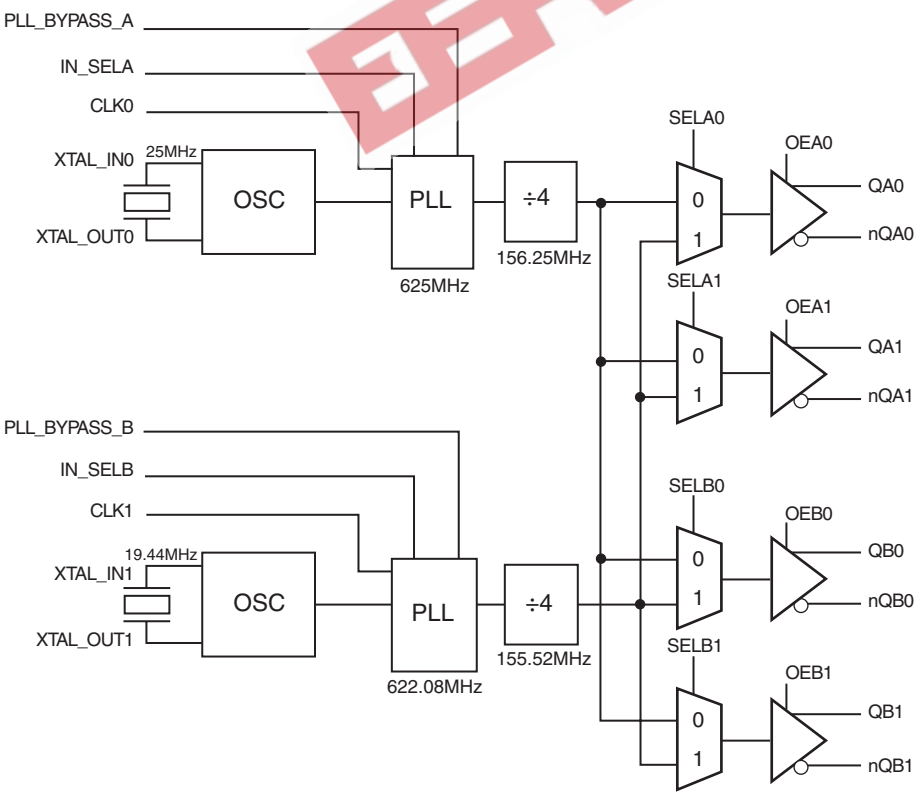
GENERAL DESCRIPTION

The ICS843204I is a 4 output LVPECL Synthesizer optimized to generate Gigabit Ethernet and SONET reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 19.44MHz and 25MHz, 18pF parallel resonant crystal, 155.52MHz and 156.25MHz frequencies can be generated. The ICS843204I uses ICS' FemtoClock™ low phase noise VCO technology and can achieve 1ps or lower typical RMS phase jitter. The ICS843204I is packaged in a 48-pin TSSOP package.

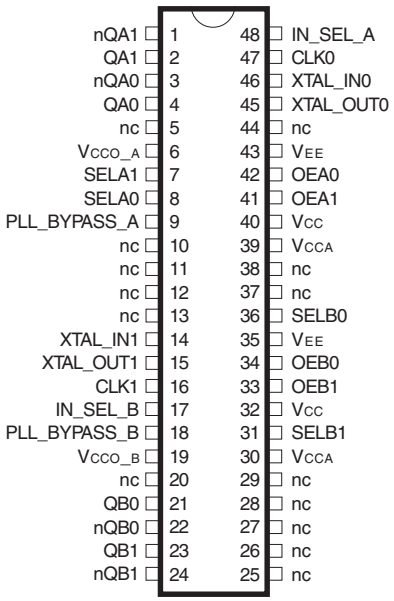
FEATURES

- Four 3.3V LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 155.52MHz and 156.25MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 155.52MHz, using a 19.44MHz crystal (12kHz - 13MHz): 0.86ps (typical)
- RMS phase jitter @ 156.25MHz, using a 19.44MHz crystal (1.875MHz - 20MHz): 0.52ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS843204I
48 Lead TSSOP
6.1mm x 12.5mm x 0.93mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQA1, QA1	Output		Differential output pair. LVPECL interface levels.
3, 4	nQA0, QA0	Output		Differential output pair. LVPECL interface levels.
5, 10, 11, 12, 13, 20, 25, 26, 27, 28, 29, 37, 38, 44	nc	Unused		No connect.
6	V_{CCO_A}	Power		Output supply pin for Bank A outputs.
7	SELA1	Input	Pulldown	Select pin. When HIGH, selects QA1/nQA1 at 155.52MHz. When LOW, selects QA1/nQA1 at 156.25MHz. LVCMOS/LVTTL interface levels.
8	SELA0	Input	Pulldown	Select pin. When HIGH, selects QA0/nQA0 at 155.52MHz. When LOW, selects QA1/nQA1 at 156.25MHz. LVCMOS/LVTTL interface levels.
9	PLL_BYPASS_A	Input	Pullup	When LOW, PLL is bypassed. When HIGH, PLL output is active.
14, 15	XTAL_IN1, XTAL_OUT1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
16, 47	CLK1, CLK0	Input	Pulldown	LVCMOS/LVTTL clock inputs.
21, 22	QB0, nQB0	Ouput		Differential output pair. LVPECL interface levels.
17	IN_SEL_B	Input	Pullup	Select pin. When HIGH, selects XTAL1 inputs. When LOW, selects CLK1 input. LVCMOS/LVTTL interface levels.
18	PLL_BYPASS_B	Input	Pullup	When LOW, PLL is bypassed. When HIGH, PLL output is active.
19	V_{CCO_B}	Power		Output supply pin for Bank B outputs.
23, 24	QB1, nQB1	Ouput		Differential output pair. LVPECL interface levels.
31	SELB1	Input	Pullup	Select pin. When HIGH, selects QB1/nQB1 at 155.52MHz. When LOW, selects QB1/nQB1 at 156.25MHz. LVCMOS/LVTTL interface levels.
30, 39	V_{CCA}	Power		Analog supply pins.
32, 40	V_{CC}	Power		Core supply pins.
33	OEB1	Input	Pullup	Output enable pin. QB1/nQB1 outputs are enable. LVCMOS/LVTTL interface levels.
34	OEB0	Input	Pullup	Output enable pin. QB0/nQB0 outputs are enabled. LVCMOS/LVTTL interface levels.
35, 43	V_{EE}	Power		Negative supply pins.
36	SELB0	Input	Pullup	Select pin. When HIGH, selects QB0/nQB0 at 155.52MHz. When LOW, selects QB0/nQB0 at 156.25MHz. LVCMOS/LVTTL interface levels.
41	OEA1	Input	Pullup	Output enable pin. QA1/nQA1 outpus are enabled. LVCMOS/LVTTL interface levels.
42	OEA0	Input	Pullup	Output enable pin. QA0/nQA0 outputs are enabled. LVCMOS/LVTTL interface levels.
45, 46	XTAL_OUT0, XTAL_IN0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
48	IN_SEL_A	Input	Pullup	Select pin. When HIGH, selects XTAL0 inputs. When LOW, selects CLK0 input. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	58.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 10\%$, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.97	3.3	3.63	V
V_{CCA}	Analog Supply Voltage		2.97	3.3	3.63	V
V_{CCO_A}, V_{CCO_B}	Output Supply Voltage		2.97	3.3	3.63	V
I_{EE}	Power Supply Current			125		mA
I_{CC}	Core Supply Current			92		mA
I_{CCA}	Analog Supply Current			14		mA
I_{CCO_A}, I_{CCO_B}	Output Supply Current			16		mA

TABLE 3B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 10\%$, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK0, CLK1, SELA0, SELA1	$V_{CC} = V_{IN} = 3.63V$			150	µA
		PLL_BYPASS_A, PLL_BYPASS_B, IN_SEL_A, IN_SEL_B, SELB1, SELB0, OEB0, OEB1, OEA0, OEA1	$V_{CC} = V_{IN} = 3.63V$			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, SELA0, SELA1	$V_{CC} = 3.63V$, $V_{IN} = 0V$	-5			µA
		PLL_BYPASS_A, PLL_BYPASS_B, IN_SEL_A, IN_SEL_B, SELB1, SELB0, OEB0, OEB1, OEA0, OEA1	$V_{CC} = 3.63V$, $V_{IN} = 0V$	-150			µA

TABLE 3C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±10%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		19.44		25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

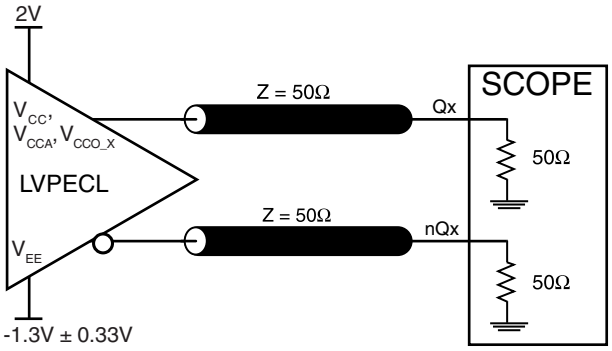
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±10%, TA = -40°C TO 85°C

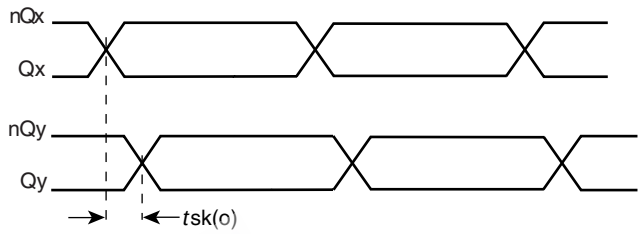
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	SELB0 = 1; OEB0 = 1		155.52		MHz
		SELA0 = 0; OEA0 = 1		156.25		MHz
*t*sk(o)	Output Skew; NOTE 1, 2			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	155.52MHz, (12kHz - 1.3MHz)		0.86		ps
		156.25MHz, (1.875MHz - 20MHz)		0.52		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		475		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at V_{CCO}/2.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: See Phase Noise plot.

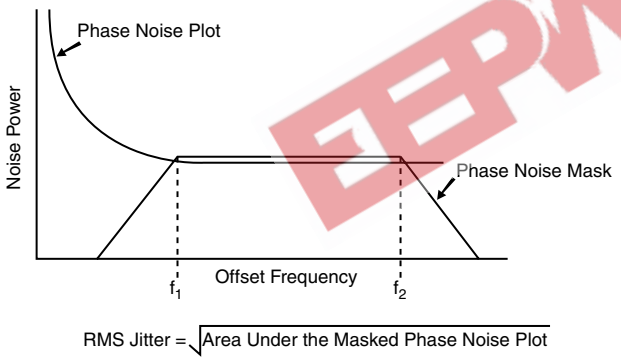
PARAMETER MEASUREMENT INFORMATION



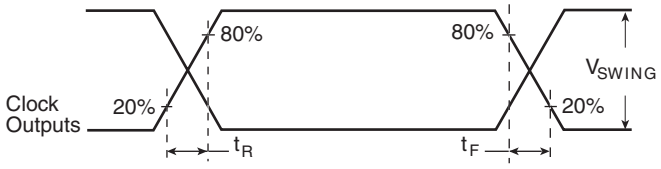
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



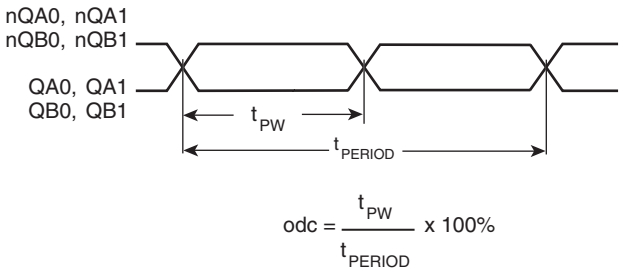
OUTPUT SKEW



RMS PHASE JITTER



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843204I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO_x} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA}.

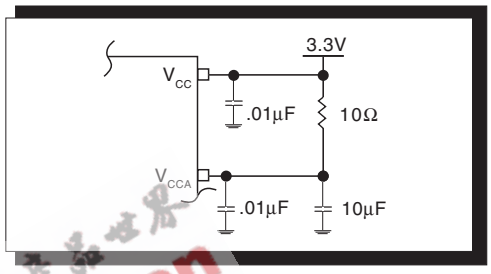


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843204I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

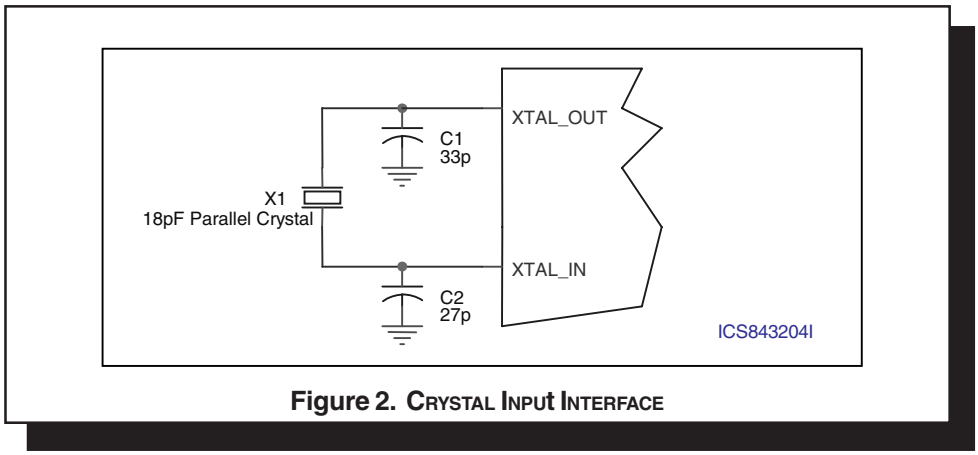


Figure 2. CRYSTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK INPUT:
For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

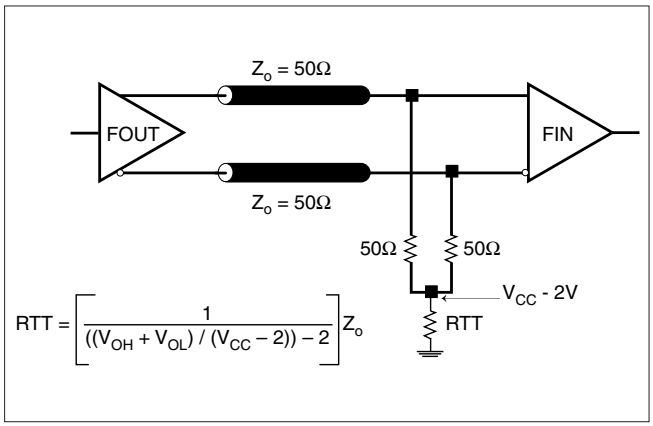


FIGURE 3A. LVPECL OUTPUT TERMINATION

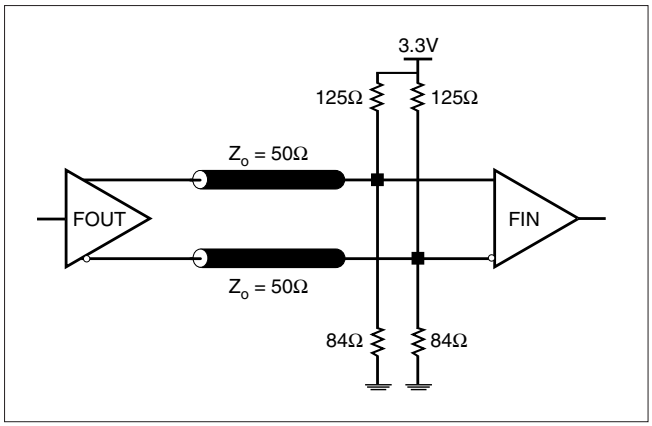


FIGURE 3B. LVPECL OUTPUT TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843002. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS843002 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 10% = 3.63V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.63V * 125mA = **453.75mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30mW = **120mW**

Total Power$_{_MAX}$ (3.63V, with all outputs switching) = 453.75mW + 120mW = **573.75mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 52.3°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.574W * 52.3°C/W = 115°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 48-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	82.6°C/W	70.3°C/W	63.7°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	58.3°C/W	52.3°C/W	49.9°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

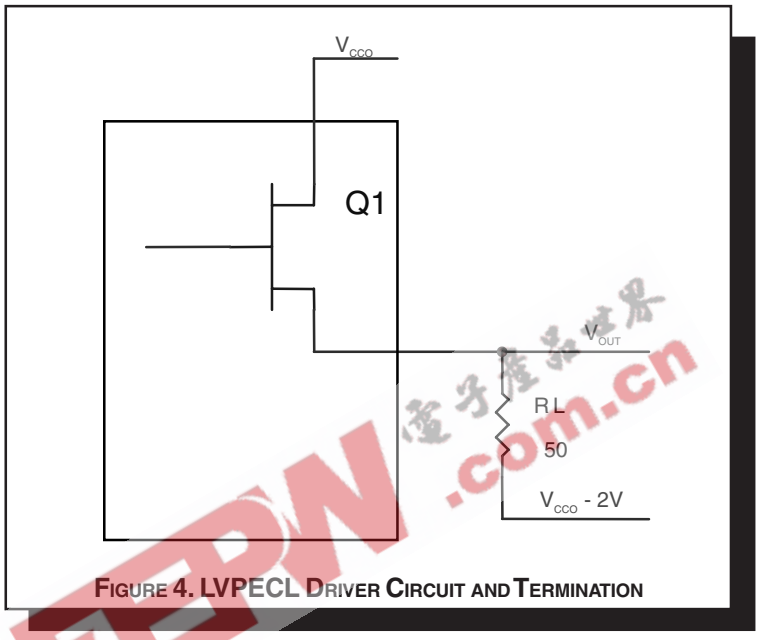


FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	82.6°C/W	70.3°C/W	63.7°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	58.3°C/W	52.3°C/W	49.9°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS843204I is: 4090

PACKAGE OUTLINE - G SUFFIX FOR 48 LEAD TSSOP

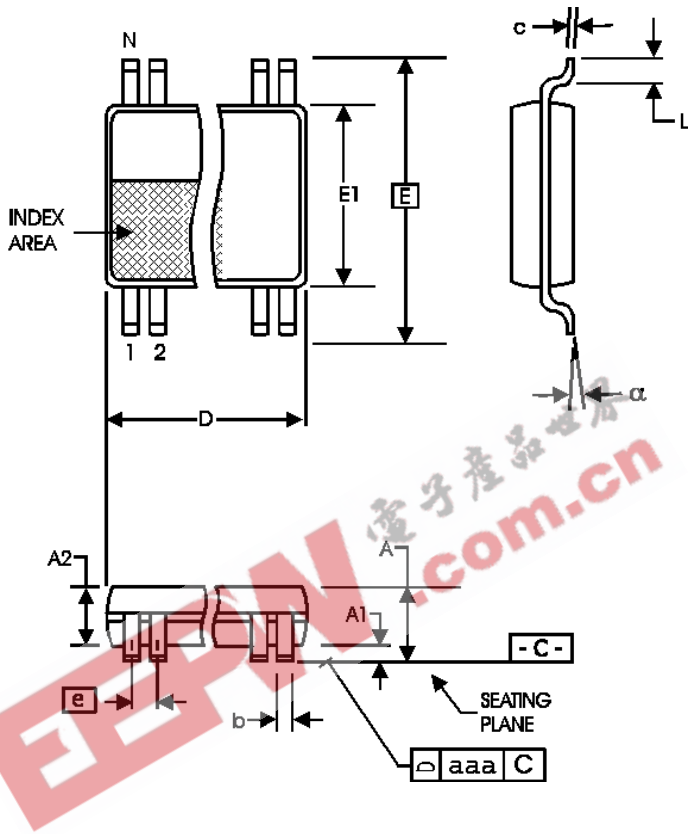


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	48	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.17	0.27
c	0.09	0.20
D	12.40	12.60
E	8.10 BASIC	
E1	6.00	6.20
e	0.50 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843204AGI	ICS843204AGI	48 Lead TSSOP	tube	-40°C to 85°C
ICS843204AGIT	ICS843204AGI	48 Lead TSSOP	1000 tape & reel	-40°C to 85°C
ICS843204AGILF	TBD	48 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS843204AGILFT	TBD	48 Lead "Lead-Free" TSSOP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.