PRELIMINARY

Integrated Circuit Systems, Inc.

ICS843001BI

FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS843001BI is a Fibre Channel Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS843001BI uses either a 26.5625MHz or a 23.4375MHz crystal to synthesize 106.25MHz, 187.5MHz or 212.5MHz, using the FREQ_SEL pin. The ICS843001BI has excellent <1ps phase jitter performance, over the 637kHz – 10MHz integration range. The ICS843001BI is packaged in a small 8-pin TSSOP and 16 VFQFN, making it ideal for use in systems with limited board space.

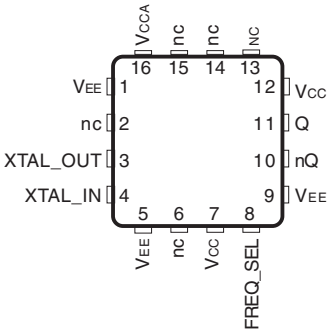
FEATURES

- One differential 3.3V LVPECL output
- Crystal oscillator interface designed for 23.4375MHz or 26.5625MHz, 18pF parallel resonant crystal
- Selectable 106.25MHz, 187.5MHz or 212.5MHz output frequency
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 106.255MHz, using a 26.5625MHz crystal (637kHz - 10MHz): 0.60ps (typical)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

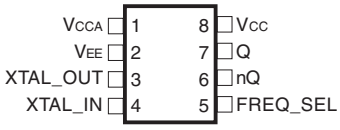
FUNCTION TABLE

Inputs		Output Frequencies
Crystal Frequency	FREQ_SEL	
26.5625MHz	0	106.25MHz (Default)
26.5625MHz	1	212.5MHz
23.4375MHz	1	187.5MHz

PIN ASSIGNMENT

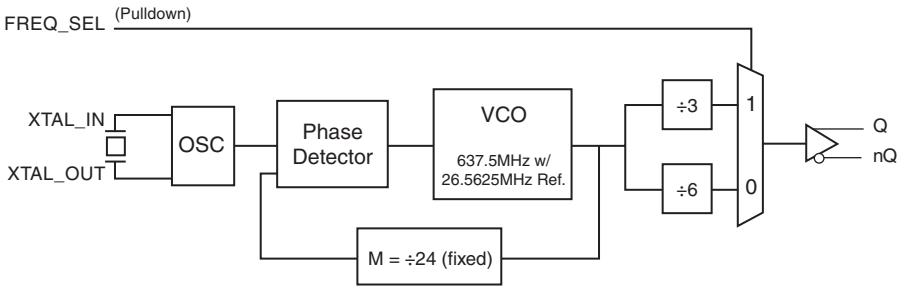


ICS843001BI
16-Lead VFQFN
3mm x 3mm x 0.95 package body
K Package
Top View



ICS843001BI
8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

BLOCK DIAGRAM



The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Name	Type		Description
V_{CC}	Power		Power supply pin.
V_{CCA}	Power		Analog supply pin.
V_{EE}	Power		Negative supply pin.
XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
nQ, Q	Output		Differential clock outputs. LVPECL interface levels.
nc	Unused		No connect.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	
8 Lead TSSOP	101.7°C/W (0 mps)
16 Lead VFQFN	51.5°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{CCA}	Analog Supply Current	included in I_{EE}		8		mA
I_{EE}	Power Supply Current			60		mA

TABLE 3B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	FREQ_SEL	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	FREQ_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA

TABLE 3C. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4. CRYSTAL CHARACTERISTICS

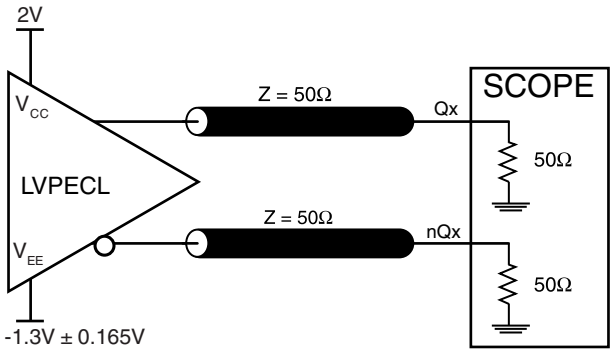
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		23.4375		26.5625	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 5. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, T_A = -40°C TO 85°C

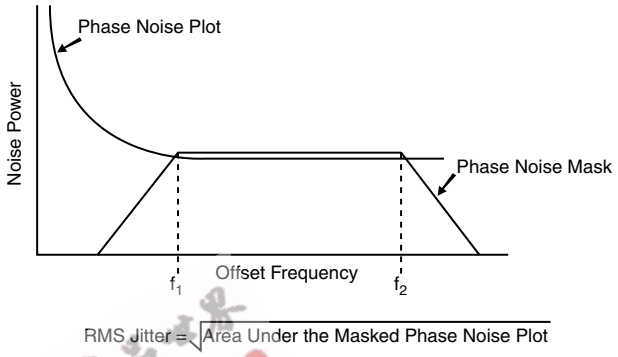
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	FREQ_SEL = 1	186.67		226.66	MHz
		FREQ_SEL = 0	93.33		113.33	MHz
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 1	212.5MHz, (637kHz to 10MHz)		0.60		ps
		187.5MHz, (1.875MHz to 20MHz)		TBD		ps
		106.25MHz, (637kHz to 10MHz)		0.60		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle	FSEL = 0		50		%
		FSEL = 1		50		%

NOTE 1: Please refer to Phase Noise Plot.

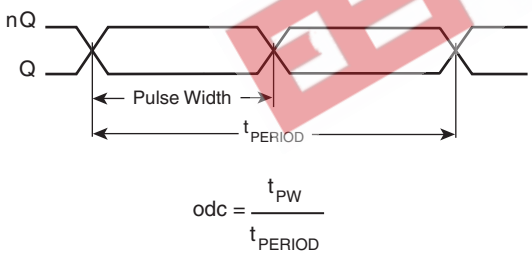
PARAMETER MEASUREMENT INFORMATION



3.3V OUTPUT LOAD AC TEST CIRCUIT



RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843001BI provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

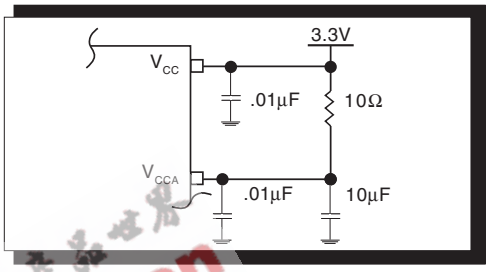


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843001BI has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

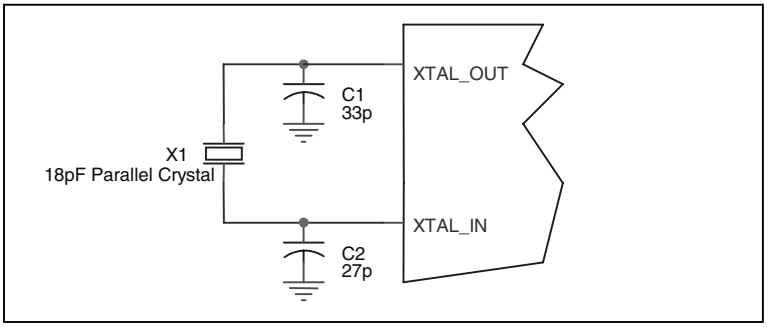


Figure 2. CRYSTAL INPUT INTERFACE

LAYOUT GUIDELINE

Figure 3A shows a schematic example of the ICS843001BI. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18pF parallel resonant crystal is used. The C1 = 27pF and C2 = 33pF are recommended for frequency accuracy. The C1 and C2 values may be slightly adjusted for optimizing frequency accuracy.

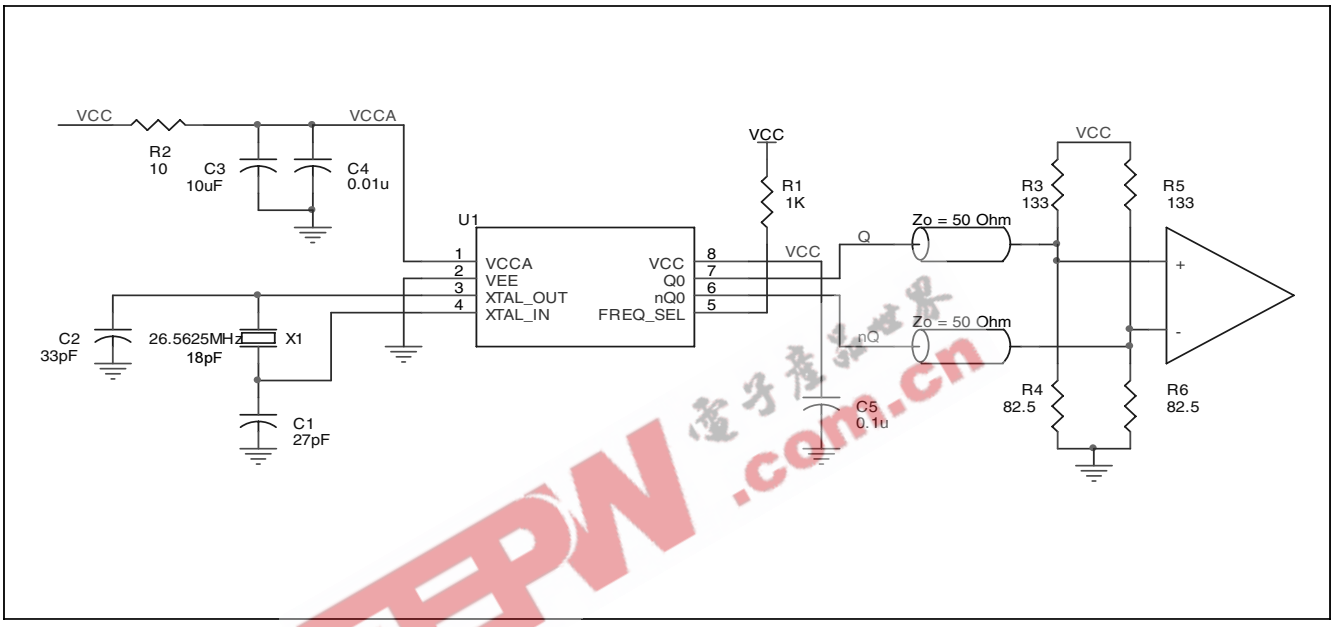


FIGURE 3A. ICS843001BI SCHEMATIC EXAMPLE

PC BOARD LAYOUT EXAMPLE

Figure 3B shows an example of ICS843001BI P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in the *Table 6.* There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

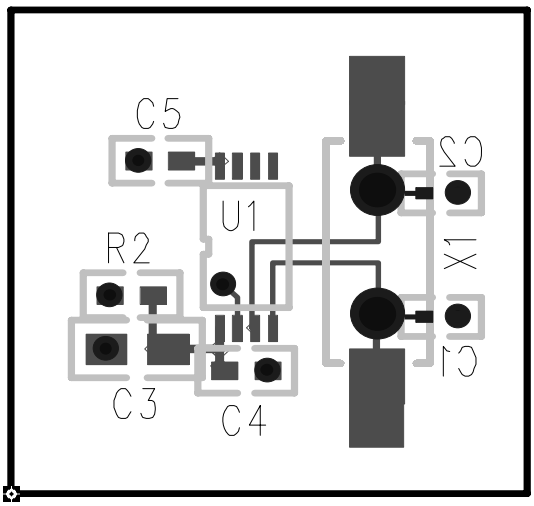


FIGURE 3B. ICS843001BI PC BOARD LAYOUT EXAMPLE

TABLE 6. FOOTPRINT TABLE

Reference	Size
C1, C2	0402
C3	0805
C4, C5	0603
R2	0603

NOTE: Table 6, lists component sizes shown in this layout example.

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843001BI. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS843001BI is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 60mA = **207.9mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 207.9mW + 30mW = **237.9mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 7A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.238W * 90.5°C/W = 106.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7A. THERMAL RESISTANCE θ_{JA} FOR 8-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TABLE 7B. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} at 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

3. Calculations and Equations.
The purpose of this section is to derive the power dissipated into the load.
LVPECL output driver circuit and termination are shown in *Figure 4.*

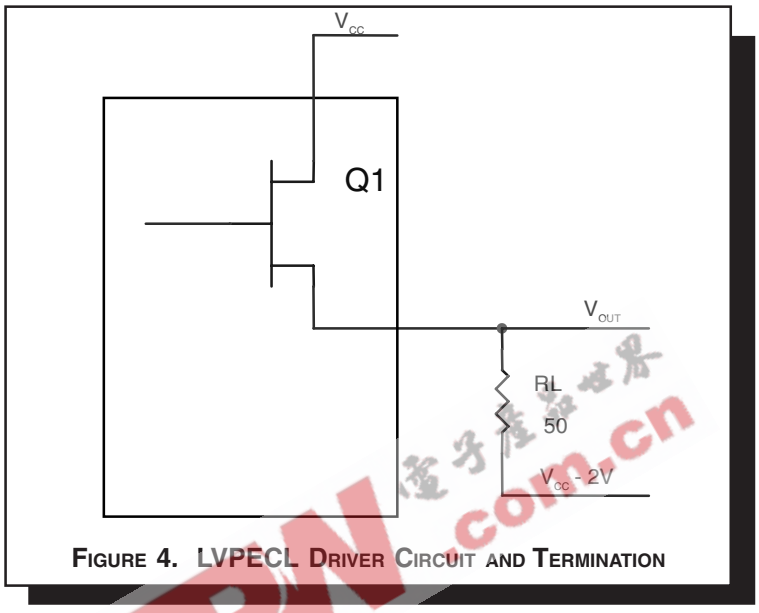


FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 8A. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters Per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TABLE 8B. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} at 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

TRANSISTOR COUNT

The transistor count for ICS843001BI is: 2069

PACKAGE OUTLINE - G SUFFIX 8 LEAD TSSOP

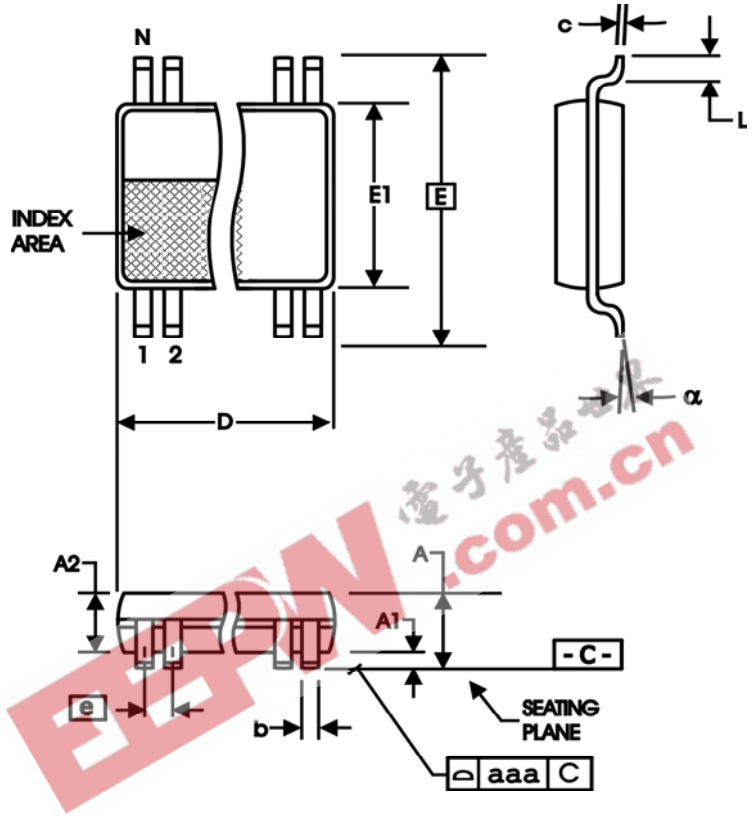


TABLE 9A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

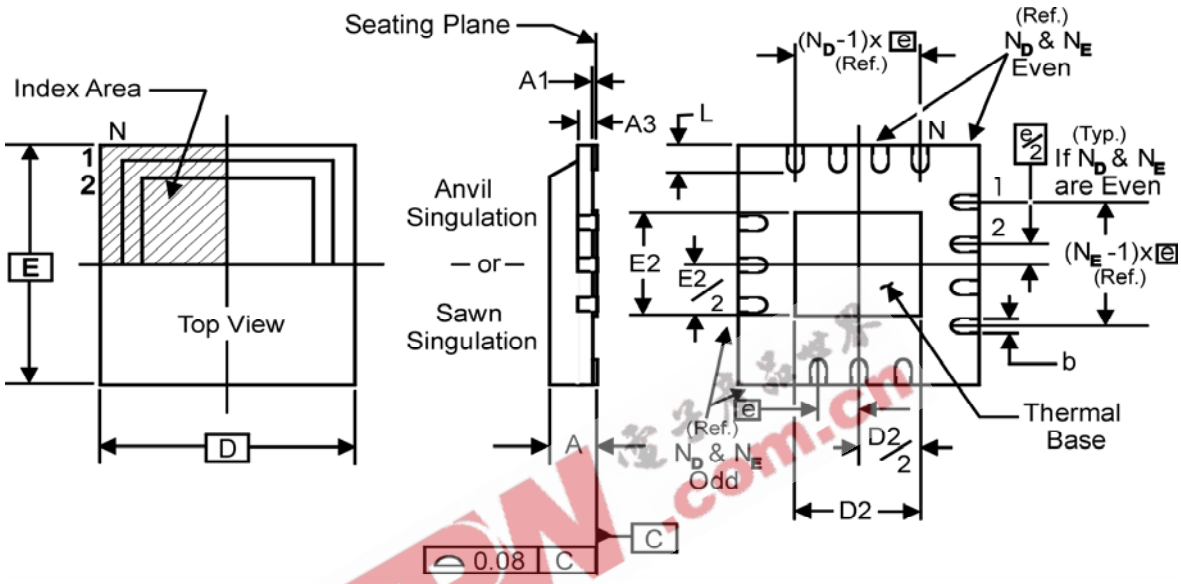


TABLE 9B. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	0.25	1.25
E	3.0	
E2	0.25	1.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843001BGI	TBD	8 Lead TSSOP	tube	-40°C to 85°C
ICS843001BGIT	TBD	8 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS843001BGILF	TBD	8 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS843001BGILFT	TBD	8 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C
ICS843001BKI	TBD	16 Lead VFQFN	tube	-40°C to 85°C
ICS843001BKIT	TBD	16 Lead VFQFN	2500 tape & reel	-40°C to 85°C
ICS843001BKILF	TBD	16 Lead "Lead-Free" VFQFN	tube	-40°C to 85°C
ICS843001BKILFT	TBD	16 Lead "Lead-Free" VFQFN	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.