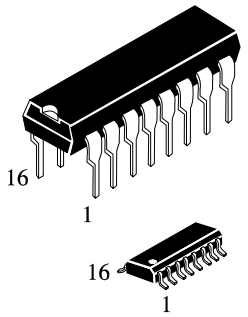
IW4043B

Quad 3-State R/S Latches
High-Voltage Silicon-Gate CMOS

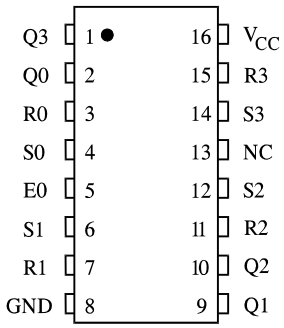


ORDERING INFORMATION
IW4043BN Plastic
IW4043BD SOIC
T_A = -55° to 125° C for all packages

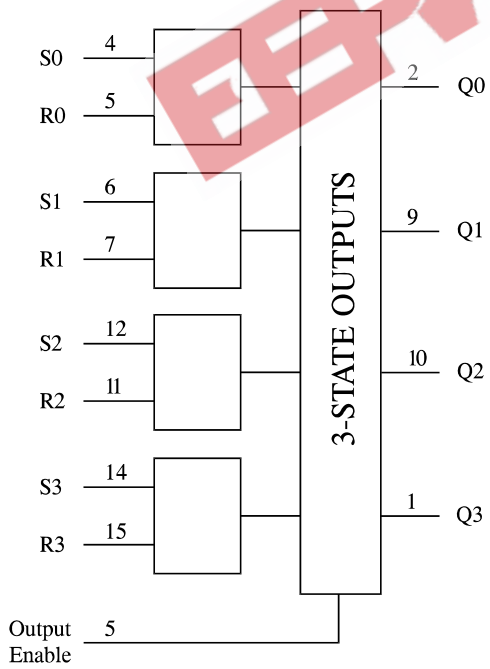
The IW4043B types are quad cross-coupled 3-state CMOS NOR latces. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic “1” or high on the ENABLE input connects the latch states to the Q outputs. A logic “0” or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  1.0 V min @ 5.0 V supply
  2.0 V min @ 10.0 V supply
  2.5 V min @ 15.0 V supply

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 13 = NO CONNECTION
PIN 16=V_{CC}
PIN 8= GND

FUNCTION TABLE

Inputs			Outputs
S	R	OE	Q
X	X	L	High Impedance
L	L	H	No change
L	H	H	L
H	L	H	H
H	H	H	H

X = don’t care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}= 0.5 V or V_{CC} - 0.5V V_{OUT}= 1.0 V or V_{CC} - 1.0 V V_{OUT}= 1.5 V or V_{CC} - 1.5V	5.0 10 15	3.5 7 11	3.5 7 11	3.5 7 11	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}= 0.5 V or V_{CC} - 0.5V V_{OUT}= 1.0 V or V_{CC} - 1.0 V V_{OUT}= 1.5 V or V_{CC} - 1.5V	5.0 10 15	1.5 3 4	1.5 3 4	1.5 3 4	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	4.95 9.95 14.95	4.95 9.95 14.95	4.95 9.95 14.95	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	V
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	μA
I_{OZ}	Maximum Three State Leakage Current	Output in High-Impedance State V_{IN}= GND or V_{CC} V_{OUT}= GND or V_{CC}	18	±0.4	±0.4	±12.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0 10 15 20	1 2 4 20	1 2 4 20	30 60 120 600	μA
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC} U_{OL}=0.4 V U_{OL}=0.5 V U_{OL}=1.5 V	 5.0 10 15	 0.64 1.6 4.2	 0.51 1.3 3.4	 0.36 0.9 2.4	mA
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC} U_{OH}=2.5 V U_{OH}=4.6 V U_{OH}=9.5 V U_{OH}=13.5 V	 5.0 5.0 10 15	 -2 -0.64 -1.6 -4.2	 -1.6 -0.51 -1.3 -3.4	 -1.15 -0.36 -0.9 -2.4	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, R_L=200kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	25°C	≤125°C	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SET or RESET to Q (Figure 1)	5.0 10 15	300 140 100	300 140 100	600 280 200	ns
t_{PHZ}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2,4)	5.0 10 15	230 110 80	230 110 80	460 220 160	ns
t_{PLZ}, t_{PZL}	Maximum Propagation Delay, Output Enable to Q (Figures 2,4)	5.0 10 15	180 100 70	180 100 70	360 200 140	ns
t_{THL}, t_{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
C_{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS (C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	25°C	≤125°C	Unit
t_w	Minimum Pulse Width, SET or RESET (Figure 3)	5.0 10 15	160 80 40	160 80 40	320 160 80	ns

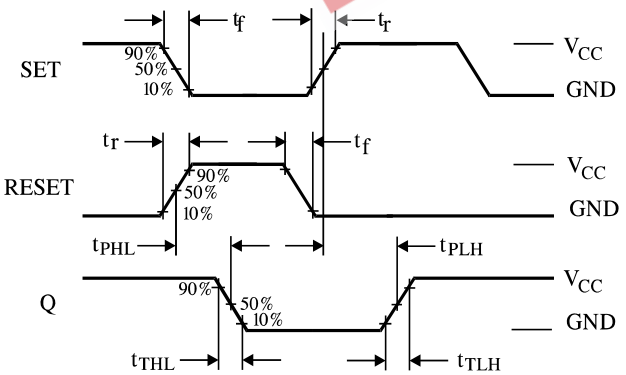


Figure 1. Switching Waveforms

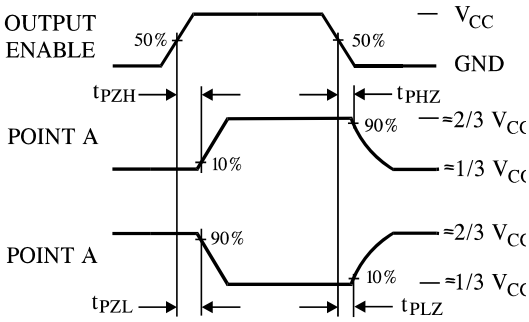


Figure 2. Switching Waveforms

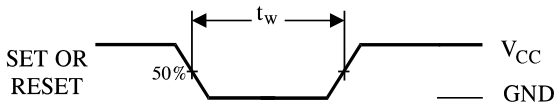
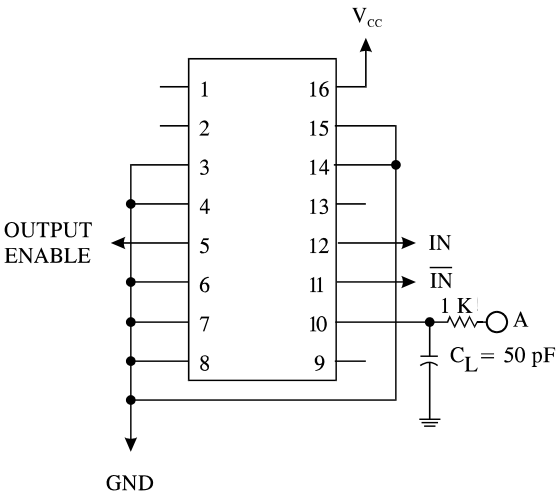


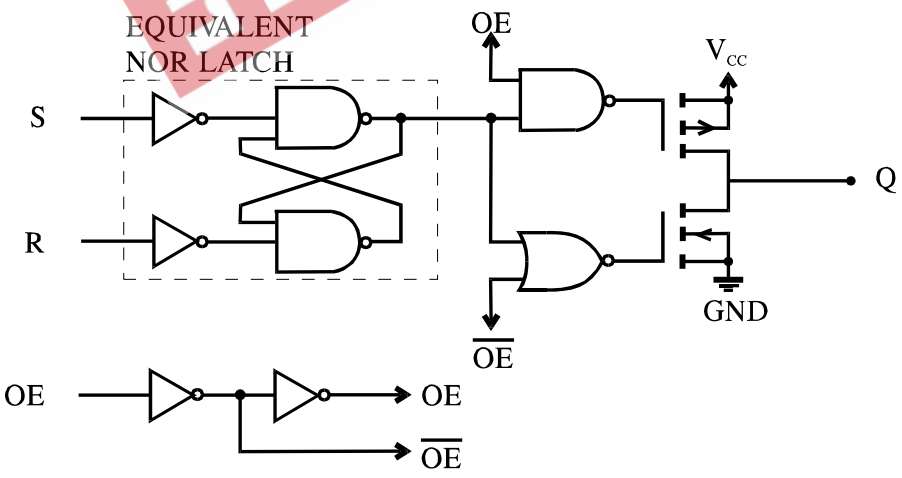
Figure 3. Switching Waveforms



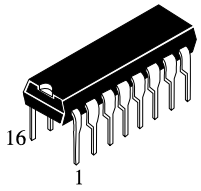
TEST	IN	$\overline{IN}$	A
t_{PHZ}	V_{CC}	GND	GND
t_{PLZ}	GND	V_{CC}	V_{CC}
t_{PZH}	V_{CC}	GND	GND
t_{PZL}	GND	V_{CC}	V_{CC}

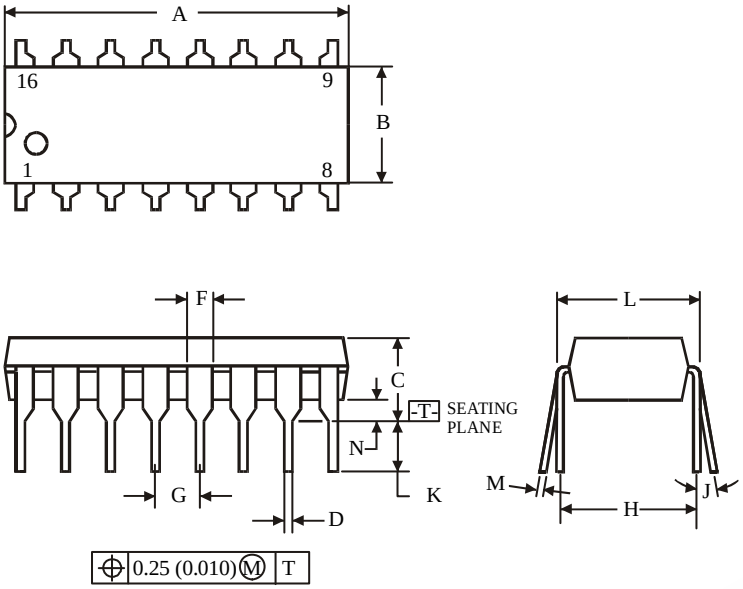
Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM
(1/4 of the Device)



N SUFFIX PLASTIC
(MS - 001BB)



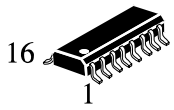


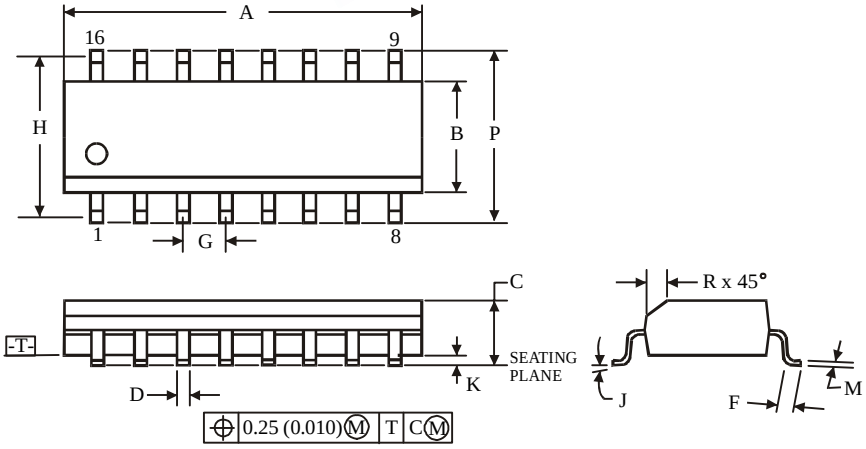
Symbol	Dimensions, mm	
	MIN	MAX
A	18.67	19.69
B	6.10	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.20	0.36
N	0.38	

NOTES:

1. imensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 012AC)





Symbol.	Dimensions, mm	
	MIN	MAX
A	9.80	10.0
B	3.80	4.00
C	1.35	1.75
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.10	0.25
M	0.19	0.25
P	5.80	6.20
R	0.25	0.50

NOTES:

1.Dimensions A and B do not include mold flash or protrusion.
2.Maximum mold flash or protrusion 0.15 mm (0.006) per side for A, for B - 0.25 mm (0.010) per side.