



HCPL062N

3.3V Dual Channel High Speed-10 MBit/s Logic Gate Optocouplers

Features

- Compact SO8 package
- Very high speed – 10MBit/s
- Superior CMR – 25kV/μs minimum (1,000 volts common mode)
- Logic gate output
- Wired OR-open collector
- Fixed threshold detector design minimizes thermal impact on switching times
- U.L. recognized (File # E90700)

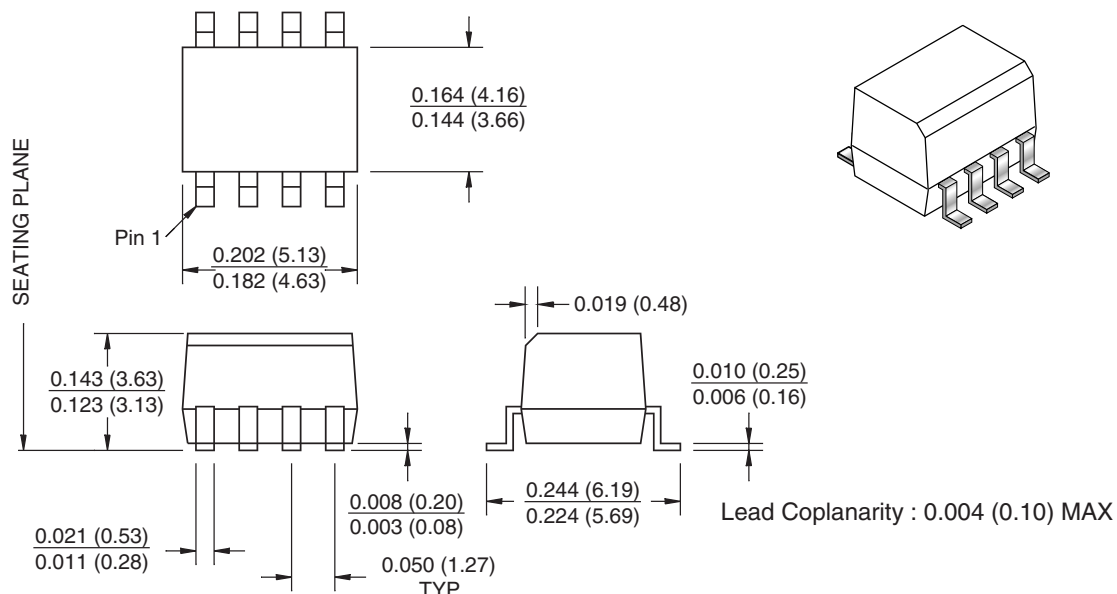
Description

The HCPL062N optocouplers consist of an AlGaAs LED, optically coupled to a very high speed integrated photo-detector logic gate consisting of bipolar transistors on a CMOS process for reduced power consumption. The output features an open collector, thereby permitting wired OR outputs. The devices are housed in a compact small-outline package. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. An internal noise shield and provides superior common mode rejection.

Applications

- Ground loop elimination
- Field buses
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface
- Instrumentation input/output isolation

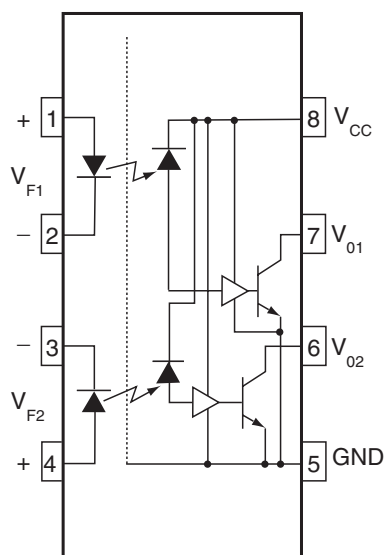
Package Dimensions



Note:

All dimensions are in inches (millimeters)

Circuit Drawing⁽¹⁾



Note:

1. The V_{CC} supply to each optoisolator must be bypassed by a $0.1\mu\text{F}$ capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected no further than 3mm from the V_{CC} and GND pins of each device.

Truth Table (Positive Logic)

Input	Output
H	L
L	H

A $0.1\mu\text{F}$ bypass capacitor must be connected between pins 8 and 5.

Absolute Maximum Ratings (No derating required up to 85°C)

Symbol	Parameter	Value	Units
T _{STG}	Storage Temperature	-40 to +125	°C
T _{OPR}	Operating Temperature	-40 to +85	°C
EMITTER			
I _F	DC/Average Forward Input Current (each channel)	50	mA
V _R	Reverse Input Voltage (each channel)	5.0	V
P _I	Power Dissipation	45	mW
DETECTOR			
V _{CC} (1 minute max)	Supply Voltage	7.0	V
I _O	Output Current (each channel)	15	mA
V _O	Output Voltage (each channel)	7.0	V
P _O	Collector Output Power Dissipation	85	mW

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
I _{FL}	Input Current, Low Level	0	250	μA
I _{FH}	Input Current, High Level	6.3 ⁽²⁾	15	mA
V _{CC}	Supply Voltage, Output	2.7	3.3	V
T _A	Operating Temperature	-40	+85	°C
N	Fan Out (TTL load)	–	5	TTL Loads
R _L	Output Pull-up	330	4K	Ω

Note:

- 6.3mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0mA or less

Electrical Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ Unless otherwise specified.)

Individual Component Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽³⁾	Max.	Unit
EMITTER						
V_F	Input Forward Voltage	$I_F = 10\text{mA}$ $T_A = 25^\circ\text{C}$	–	–	1.8	V
			–	–	1.75	
B_{VR}	Input Reverse Breakdown Voltage	$I_R = 10\mu\text{A}$	5.0	–	–	V
$\Delta V_F/\Delta T_A$	Input Diode Temperature Coefficient	$I_F = 10\text{mA}$	–	-1.5	–	mV/ $^\circ\text{C}$
DETECTOR						
I_{CCH}	High Level Supply Current	$I_F = 0\text{mA}$, $V_{CC} = 3.3\text{V}$	–	7.1	10	mA
I_{CCL}	Low Level Supply Current	$I_F = 10\text{mA}$, $V_{CC} = 3.3\text{V}$	–	6.7	15	mA

Switching Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 3.3\text{V}$, $I_F = 7.5\text{mA}$ Unless otherwise specified.)

Symbol	AC Characteristics	Test Conditions	Min.	Typ. ⁽³⁾	Max.	Unit
T_{PLH}	Propagation Delay Time to Output High Level	$R_L = 350\Omega$, $C_L = 15\text{pF}$ Note 4, Fig. 10	–	–	90	ns
T_{PHL}	Propagation Delay Time to Output Low Level	$R_L = 350\Omega$, $C_L = 15\text{pF}$ Note 5, Fig. 10	–	–	75	ns
$ T_{PHL} - T_{PLH} $	Pulse Width Distortion	$R_L = 350\Omega$, $C_L = 15\text{pF}$ Fig. 10	–	–	25	ns
t_r	Output Rise Time (10–90%)	$R_L = 350\Omega$, $C_L = 15\text{pF}$ Note 6, Fig. 10	–	16	–	ns
t_f	Output Fall Time (90–10%)	$R_L = 350\Omega$, $C_L = 15\text{pF}$ Note 7, Fig. 10	–	4	–	ns
ICM_{HI}	Common Mode Transient Immunity (at Output High Level)	$R_L = 350\Omega$, $T_A = 25^\circ\text{C}$, $I_F = 0\text{mA}$, $V_{CC} = 3.3\text{V}$, $V_{O(\text{Min.})} = 2\text{V}$ $ V_{CM} = 1,000\text{V}$ Notes 8, 11, Fig. 11	25,000	–	–	V/ μs
ICM_{LI}	Common Mode Transient Immunity (at Output Low Level)	$R_L = 350\Omega$, $T_A = 25^\circ\text{C}$, $I_F = 7.5\text{mA}$, $V_{CC} = 3.3\text{V}$, $V_{O(\text{Max.})} = 0.8\text{V}$ $ V_{CM} = 1,000\text{V}$ Notes 9, 11, Fig. 11	25,000	–	–	V/ μs

Transfer Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ Unless otherwise specified.)

Symbol	DC Characteristics	Test Conditions	Min.	Typ. ⁽³⁾	Max.	Unit
V_{OL}	Low Level Output Voltage	$V_{CC} = 3.3\text{V}$, $I_F = 5\text{mA}$, $I_{OL} = 13\text{mA}$	–	–	0.6	V
I_{FT}	Input Threshold Current	$V_{CC} = 3.3\text{V}$, $V_O = 0.6\text{V}$, $I_{OL} = 13\text{mA}$	–	–	5	mA

Isolation Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ Unless otherwise specified.)

Symbol	Characteristics	Test Conditions	Min.	Typ. ⁽³⁾	Max.	Unit
I_{I-O}	Input-Output Insulation Leakage Current	Relative humidity = 45% $T_A = 25^\circ\text{C}$, $t = 5$ sec. $V_{I-O} = 3000$ VDC, Note 10	–	–	1.0	μA
V_{ISO}	Withstand Insulation Test Voltage	$R_H < 50\%$, $T_A = 25^\circ\text{C}$ $I_{I-O} \leq 2\mu\text{A}$, $t = 1$ min., Note 10	2500	–	–	V_{RMS}
R_{I-O}	Resistance (Input to Output)	$V_{I-O} = 500\text{V}$, Note 10	–	10^{12}	–	Ω
C_{I-O}	Capacitance (Input to Output)	$f = 1\text{MHz}$, Note 10	–	0.6	–	pF

Notes:

3. All typical values are at $V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.
4. t_{PLH} – Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
5. t_{PHL} – Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
6. t_r – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
7. t_f – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
8. CM_H – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e., $V_{OUT} > 2.0$ V). Measured in volts per microsecond (V/ μs).
9. CM_L – The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., $V_{OUT} < 0.8$ V). Measured in volts per microsecond (V/ μs).
10. Device considered a two-terminal device: Pins 1,2,3 and 4 shorted together, and Pins 5,6,7 and 8 shorted together.
11. The power supply bypass capacitors must be no further than 3mm from the leads of the optocoupler. A low inductance ground plane width of with $\leq 5\text{nH}$ of series lead inductance is required.

Typical Performance Curves

Fig. 1 Forward Current vs. Forward Voltage

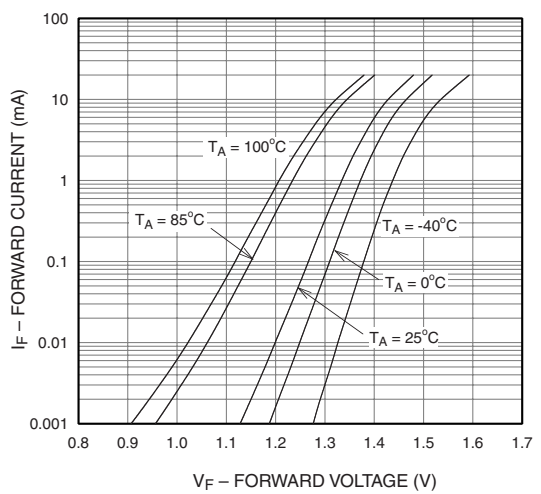


Fig. 2 High Level Output Current vs. Ambient Temperature

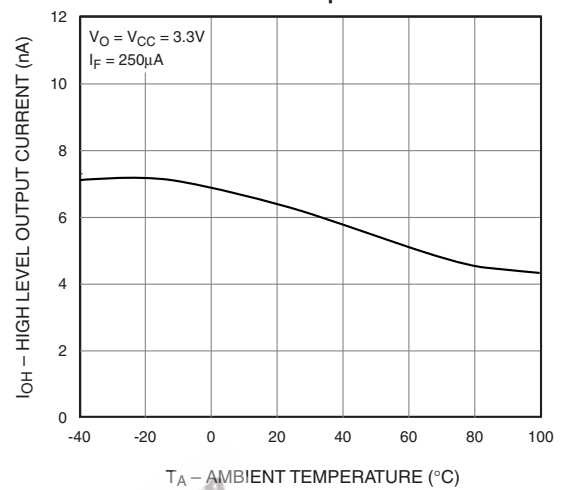


Fig. 3 Low Level Output Current vs. Ambient Temperature

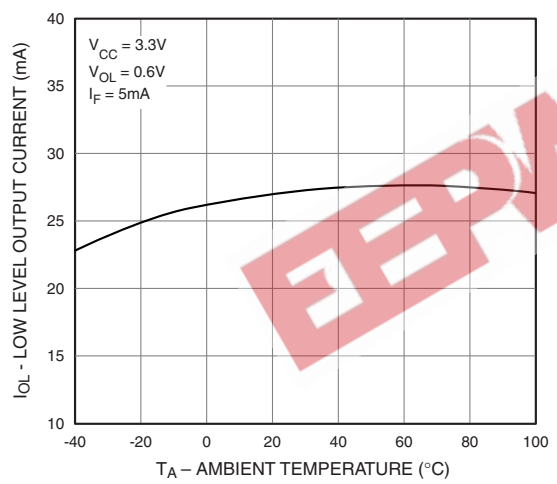
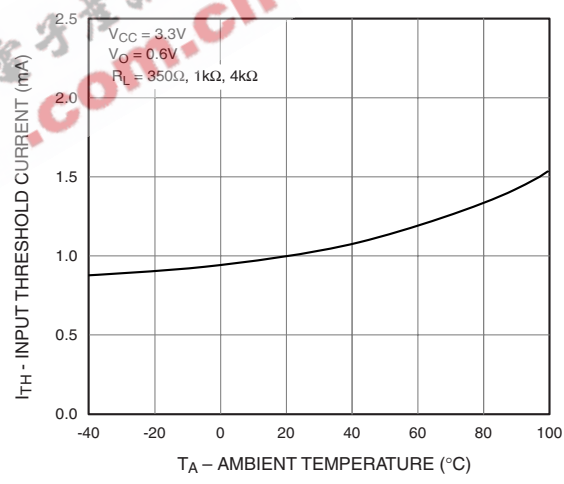


Fig. 4 Input Threshold Current vs. Temperature



Typical Performance Curves (Continued)

Fig. 5 Pulse Width Distortion vs. Ambient Temperature

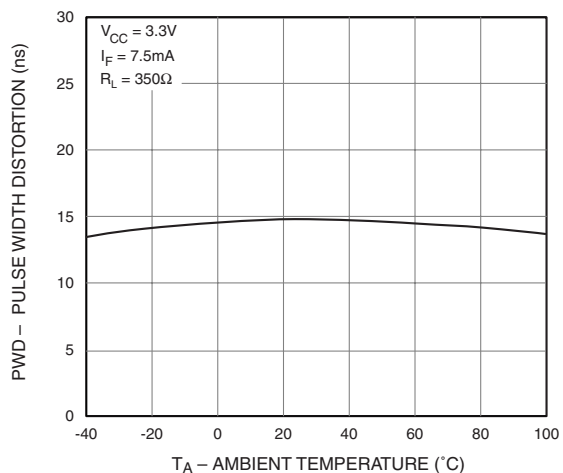


Fig. 6 Propagation Delay vs. Pulse Input Current

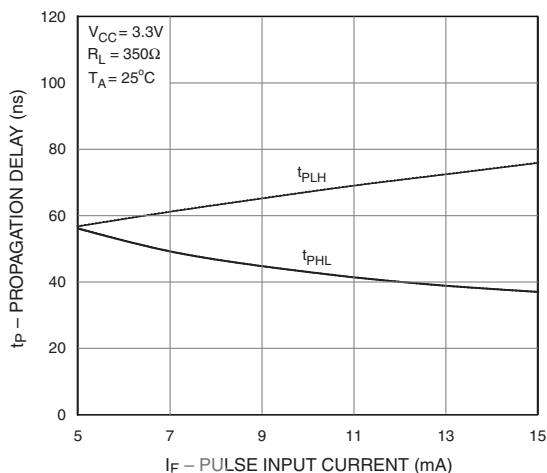


Fig. 7 Propagation Delay vs. Ambient Temperature

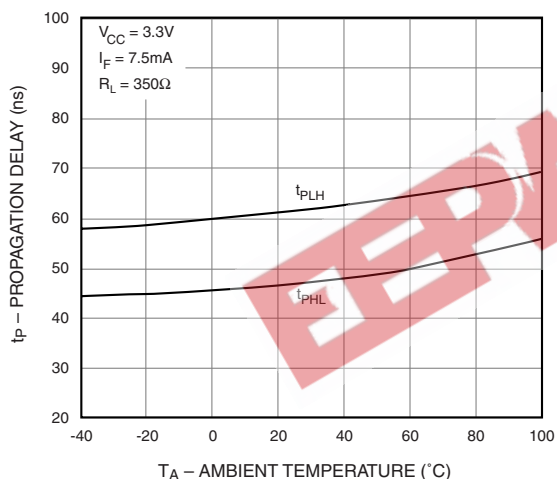
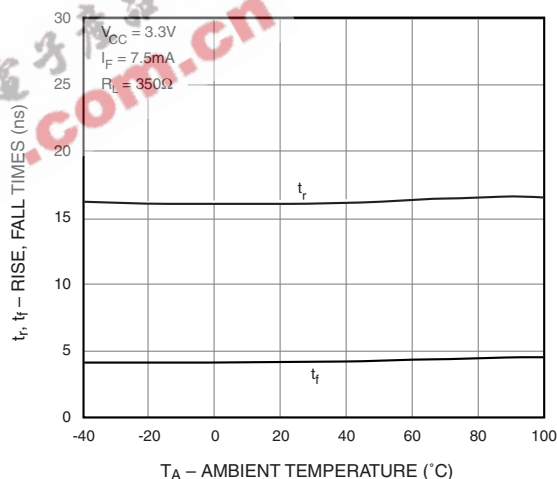
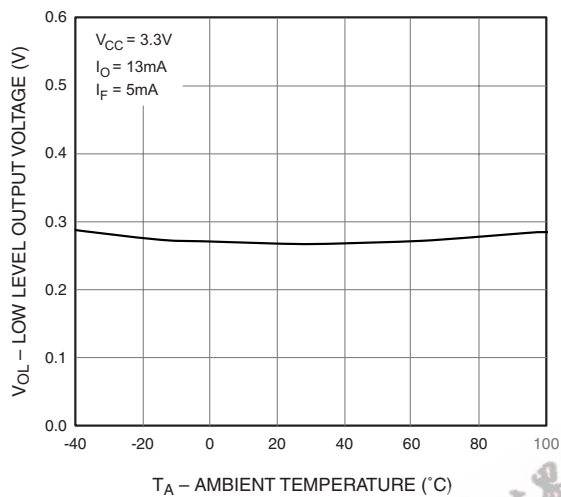


Fig. 8 Rise and Fall Times vs. Ambient Temperature



Typical Performance Curves (Continued)

Fig. 9 Low Level Output Voltage vs. Ambient Temperature



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Test Circuits

Fig. 10 Test Circuit and Waveforms for t_{PLH} , t_{PHL} , t_r and t_f

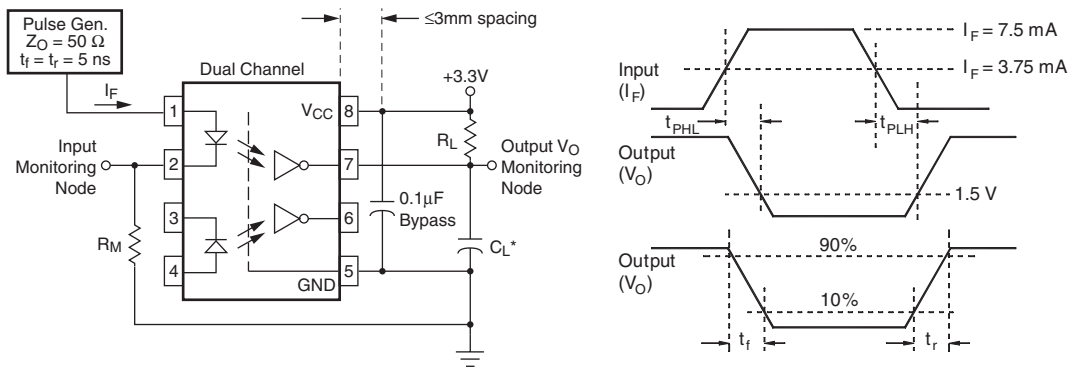
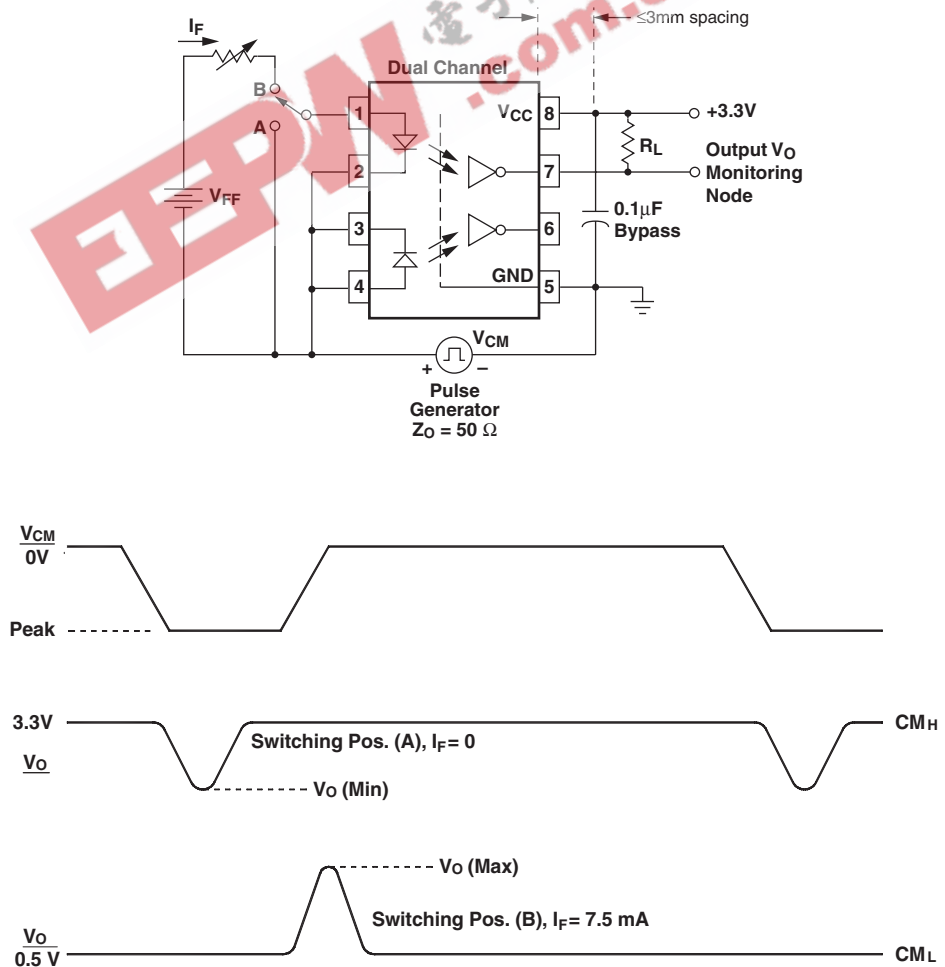
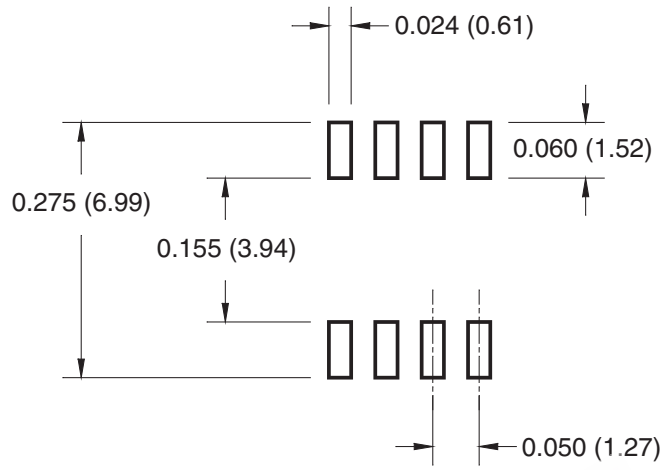


Fig. 11 Test Circuit and Waveforms for Common Mode Transient Immunity



Footprint

8-Pin Small Outline

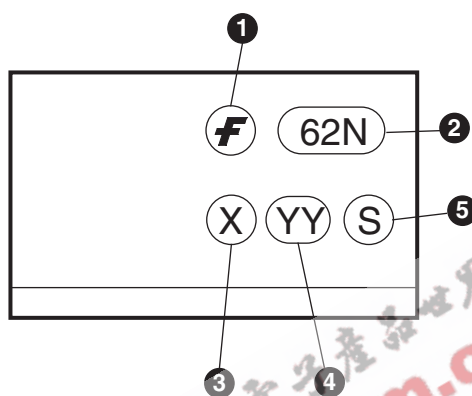


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Ordering Information

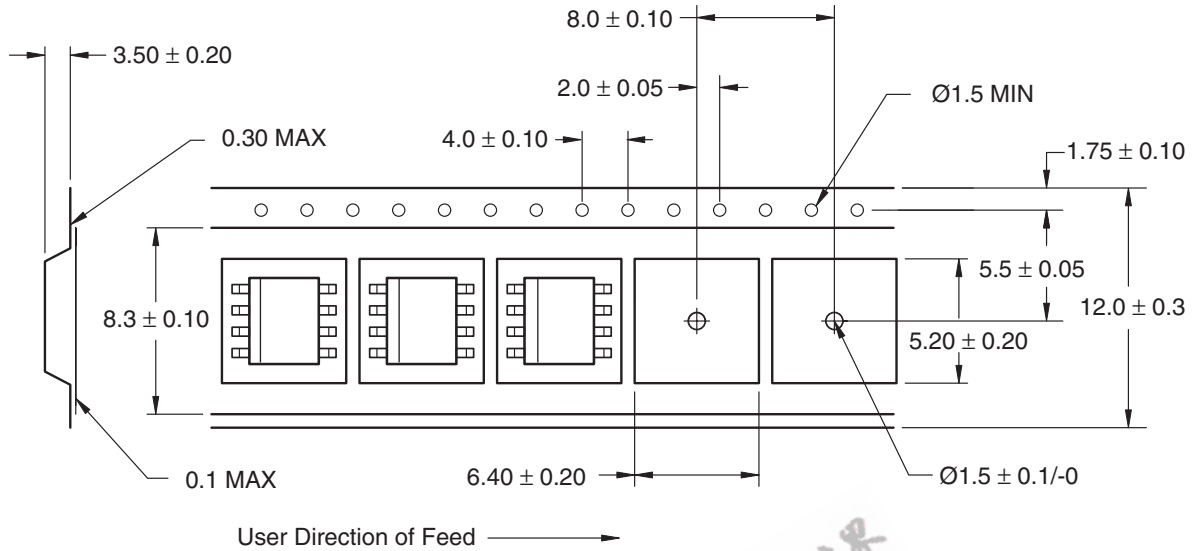
Option	Order Entry Identifier	Description
No Suffix	HCPL062N	Shipped in tubes (50 units per tube)
R1	HCPL062NR1	Tape and Reel (500 units per reel)
R2	HCPL062NR2	Tape and Reel (2500 units per reel)

Marking Information

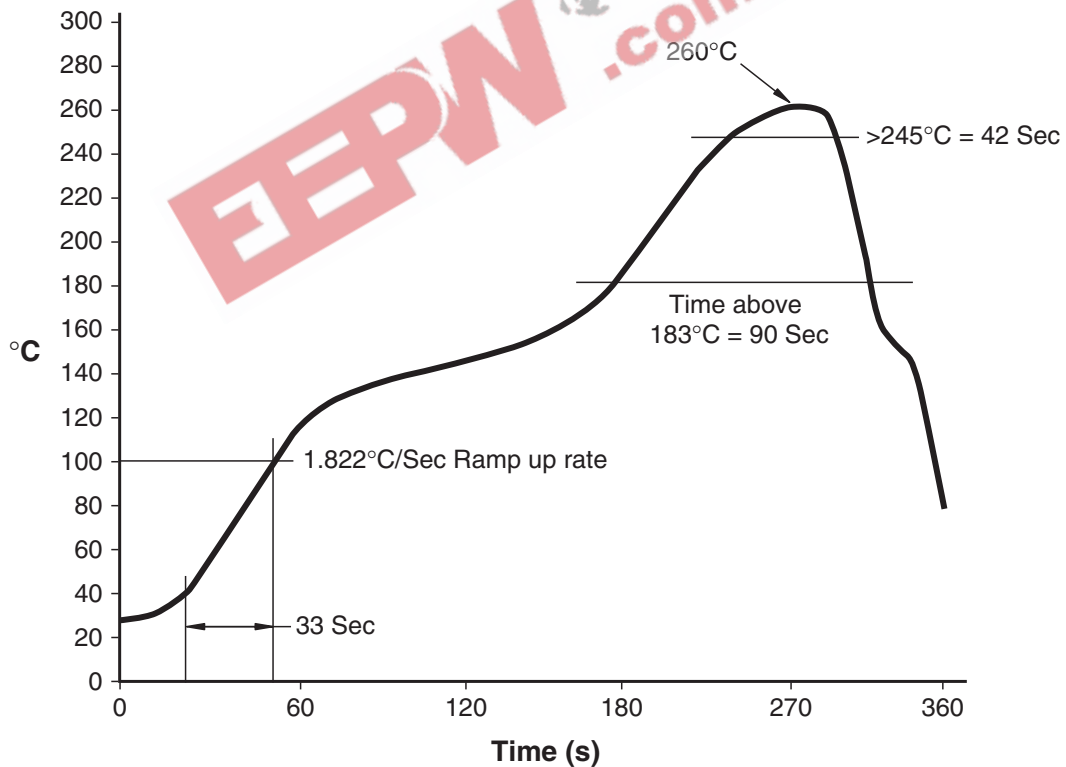


Definitions	
1	Fairchild logo
2	Device number
3	One digit year code, e.g., '3'
4	Two digit work week ranging from '01' to '53'
5	Assembly package code

Carrier Tape Specification



Reflow Profile





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