

DATA SHEET

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FBL2041

FBL2041I

3.3V BTL 7-bit Futurebus+ transceiver
(standard A-port)

Product specification
Supersedes data of 1998 May 11
IC23 Data Handbook

1999 Apr 27

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

FBL2041 FBL2041I

FEATURES

- 7-bit BTL transceiver
- Separate I/O on TTL A-port
- Inverting
- Three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω.
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack
- 5V compatible I/O on A-port
- Industrial temperature range available as FBL2041I

DESCRIPTION

The FBL2041/FBL2041I is a 7-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FBL2041 is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The FBL2041/FBL2041I is pin and function compatible with FB2041 but operates at a 3.3V supply voltage, greatly reducing power consumption.

The B-port interfaces to "Backplane Transceiver Logic" (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1Vp-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

There are three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement. The TTL/BTL output drivers for bit 0 are enabled with $OEA1/\overline{OEB1}$, output drivers for bits 1–2–3 are enabled with $OEA2/\overline{OEB2}$ and output drivers for bits 4–5–6 are enabled with $OEA3/\overline{OEB3}$.

The A-port operates at TTL levels with separate I/O. The 3-state A-port drivers are enabled when OEA_n goes High after an extra 6ns delay which is built in to provide a break-before-make function. When OEA_n goes Low, A-port drivers become High impedance without any extra delay. During power on/off cycles, the A-port drivers are held in a High impedance state when V_{CC} is below 1.3V.

The B-port has an output enable, OEB_0 , which affects all seven drivers. When OEB_0 is High and \overline{OEB}_n is Low the output driver will be enabled. When OEB_0 is Low or if \overline{OEB}_n is High, the B-port drivers will be inactive and at the level of the backplane signal.

To support live insertion, OEB_0 is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 3.3V level while V_{CC} is Low. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated in the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble-shoot.

JTAG boundary scan functionality is provided as an option with signals TMS, TCK, TDI and TDO. When this option is not present, TMS and TCK are no-connects (no bond wires) and TDI and TDO are shorted together internally.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay AIn to \overline{B}_n	4.2 3.5	ns
t_{PLH} t_{PHL}	Propagation delay \overline{B}_n to AOn	4.8 4.9	ns
C_{OB}	Output capacitance (\overline{B}_0 - \overline{B}_6 only)	6	pF
I_{OL}	Output current (\overline{B}_0 - \overline{B}_6 only)	100	mA
I_{CC}	Supply Current	Standby	5.2
		AIn to \overline{B}_n (outputs Low or High)	3.2
		\overline{B}_n to AOn (outputs Low)	13.5
		\overline{B}_n to AOn (outputs High)	10.7

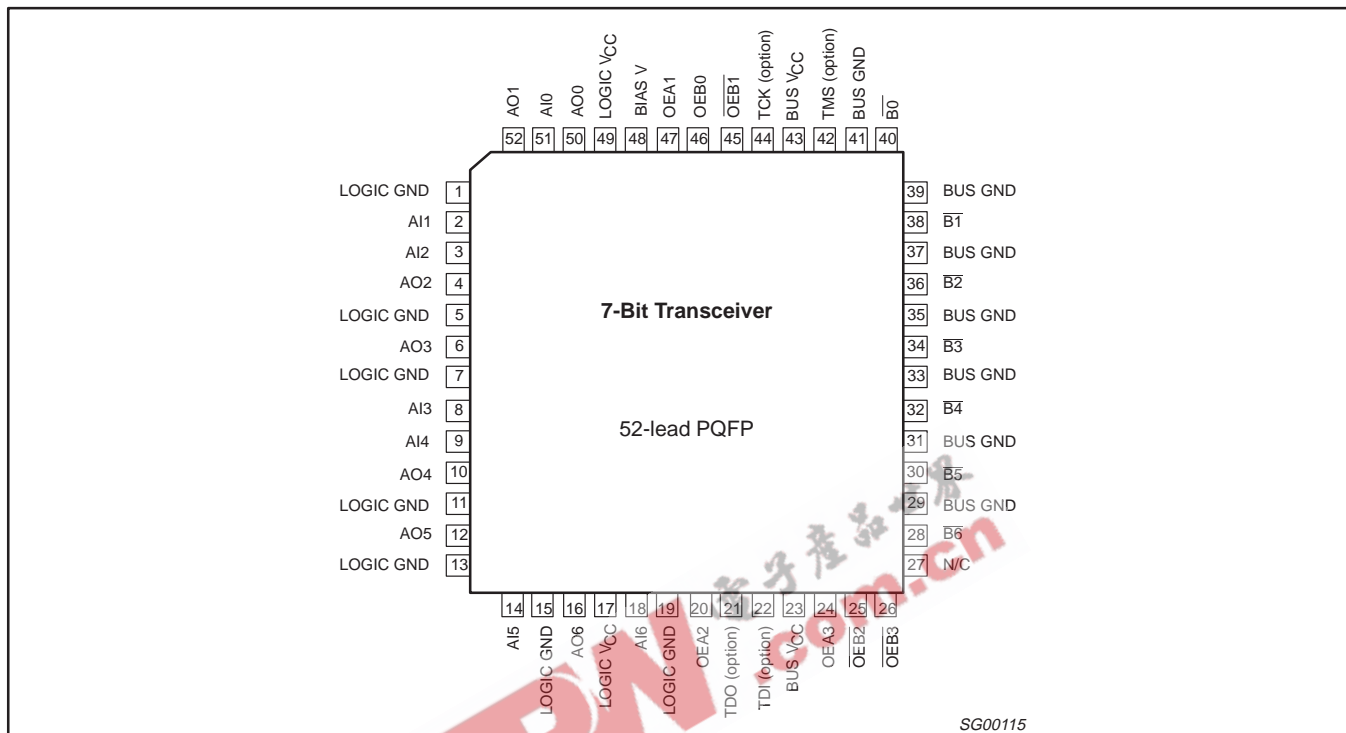
ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE $V_{CC} = 3.3V \pm 10\%$; $T_{amb} = 0$ to $+70^\circ C$	INDUSTRIAL RANGE $V_{CC} = 3.3V \pm 10\%$; $T_{amb} = -40$ to $+85^\circ C$	DWG No.
52-pin Plastic Quad Flatpack	FBL2041 BB	FBL2041I BB	SOT379-1

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

FBL2041
FBL2041I

PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
A10 – A16	51, 2, 3, 8, 9, 14, 18	Input	Data inputs (TTL)
AO0 – AO6	50, 52, 4, 6, 10, 12, 16	Output	3-State outputs (TTL)
$\bar{B}0$ – $\bar{B}6$	40, 38, 36, 34, 32, 30, 28	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the Bn outputs when High
$\bar{OEB}1$	45	Input	Enables the B0 output when Low
$\bar{OEB}2$	25	Input	Enables the B1 – B3 outputs when Low
$\bar{OEB}3$	26	Input	Enables the B4 – B6 outputs when Low
OEA1	47	Input	Enables the A0 outputs when High
OEA2	20	Input	Enables the A1 – A3 outputs when High
OEA3	24	Input	Enables the A4 – A6 outputs when High
BUS GND	41, 39, 37, 35, 33, 31, 29	GND	Bus ground (0V)
LOGIC GND	1, 5, 7, 11, 13, 15, 19	GND	Logic ground (0V)
BUS V _{CC}	23, 43	Power	Positive supply voltage
LOGIC V _{CC}	17, 49	Power	Positive supply voltage BAND GAP
BIAS V	48	Power	Positive supply voltage
TMS	42	Input	Test Mode Select (no-connect)
TCK	44	Input	Test Clock (no-connect)
TDI	22	Input	Test Data In (shorted to TDO)
TDO	21	Output	Test Data Out (TDI)
N/C	27	—	Not connected

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

FBL2041
FBL2041I

FUNCTION TABLE

MODE	INPUTS									OUTPUTS	
	AIn	Bn*	OEB0	OEB1	OEB2	OEB3	OEA1	OEA2	OEA3	AOn	Bn*
AIn to Bn	L	—	H	L	L	L	L	L	L	Z	H**
	H	—	H	L	L	L	L	L	L	Z	L
	L	—	H	L	L	L	H	H	H	L	H**
	H	—	H	L	L	L	H	H	H	H	L
AIO to B0	L	—	H	L	X	X	L	L	L	Z	H**
	H	—	H	L	X	X	L	L	L	Z	L
	L	—	H	L	X	X	H	H	H	L	H**
	H	—	H	L	X	X	H	H	H	H	L
AI1 – AI3 to B1 – B3	L	—	H	X	L	X	L	L	L	Z	H**
	H	—	H	X	L	X	L	L	L	Z	L
	L	—	H	X	L	X	H	H	H	L	H**
	H	—	H	X	L	X	H	H	H	H	L
AI4 – AI6 to B4 – B6	L	—	H	X	X	L	L	L	L	Z	H**
	H	—	H	X	X	L	L	L	L	Z	L
	L	—	H	X	X	L	H	H	H	L	H**
	H	—	H	X	X	L	H	H	H	H	L
Disable Bn outputs	X	X	L	X	X	X	X	X	X	X	H**
	X	X	X	H	H	H	X	X	X	X	H**
Disable B0 outputs	X	X	H	H	X	X	X	X	X	X	H**
Disable B1 – B3 outputs	X	X	H	X	H	X	X	X	X	X	H**
Disable B4 – B6 outputs	X	X	H	X	X	H	X	X	X	X	H**
Bn to AOn	X	L	L	X	X	X	H	H	H	H	Input
	X	H	L	X	X	X	H	H	H	L	Input
	X	L	X	H	H	H	H	H	H	H	Input
	X	H	X	H	H	H	H	H	H	L	Input
B0 to AO0	X	L	L	X	X	X	H	X	X	H	Input
	X	H	L	X	X	X	H	X	X	L	Input
	X	L	X	H	H	H	H	X	X	H	Input
	X	H	X	H	H	H	H	X	X	L	Input
B1 – B3 to AO1 – AO3	X	L	L	X	X	X	X	H	X	H	Input
	X	H	L	X	X	X	X	H	X	L	Input
	X	L	X	H	H	H	X	H	X	H	Input
	X	H	X	H	H	H	X	H	X	L	Input
B4 – B6 to AO4 – AO6	X	L	L	X	X	X	X	X	H	H	Input
	X	H	L	X	X	X	X	X	H	L	Input
	X	L	X	H	H	H	X	X	H	H	Input
	X	H	X	H	H	H	X	X	H	L	Input
Disable AOn outputs	X	X	X	X	X	X	L	L	L	Z	X
Disable AO0 outputs	X	X	X	X	X	X	L	X	X	Z	X
Disable AO1 – AO3 outputs	X	X	X	X	X	X	X	L	X	Z	X
Disable AO4 – AO6 outputs	X	X	X	X	X	X	X	X	L	Z	X

NOTES:

H = High voltage level

L = Low voltage level

X = Don't care

Z = High-impedance (OFF) state

— = Input not externally driven

H** = Goes to level of pull-up voltage

B* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

FBL2041
FBL2041I**ABSOLUTE MAXIMUM RATINGS**

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +4.6	V
V_{IN}	Input voltage	A10 – A16, OE $\overline{B}0$, OE $\overline{B}n$, OEAn	-0.5 to +7.0	V
		$\overline{B}0$ – $\overline{B}6$	-0.5 to +3.5	
I_{IN}	Input current	$V_{IN} < 0$	-50	
V_{OUT}	Voltage applied to output in High output state		-0.5 to +7.0	V
I_{OUT}	Current applied to output in Low output state/High output state	A00 – A06	64, -64	mA
		$\overline{B}0$ – $\overline{B}6$	200	
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	COMMERCIAL LIMITS $V_{CC} = 3.3V \pm 10\%$; $T_{amb} = 0$ to $+70^\circ C$			INDUSTRIAL LIMITS $V_{CC} = 3.3V \pm 10\%$; $T_{amb} = -40$ to $+85^\circ C$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	3.0	3.3	3.6	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	Except $\overline{B}0$ – $\overline{B}6$	2.0		2.0			V
		$\overline{B}0$ – $\overline{B}6$	1.62	1.55	1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B}0$ – $\overline{B}6$		0.8			0.8	V
		$\overline{B}0$ – $\overline{B}6$		1.47			1.47	
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current	A00 – A06		-32			-32	mA
I_{OL}	Low-level output current	A00 – A06		+32			+32	mA
		$\overline{B}0$ – $\overline{B}6$		100			100	
C_{OB}	Output capacitance on B port		6	7		6	7	pF
T_{amb}	Operating free-air temperature range	0		+70	-40		+85	°C

LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
V_{BIASV}	Bias pin voltage	Voltage difference between the Bias voltage and V_{CC} after the PCB is plugged in.		0.5	V
I_{BIASV}	Bias pin (I_{BIASV}) input DC current	$V_{CC} = 0$ V, Bias $V = 3.6$ V		1.2	mA
		$V_{CC} = 3.3$ V, Bias $V = 3.6$ V		10	μ A
\overline{V}_{Bn}	Bus voltage during prebias	$\overline{B}0$ – $\overline{B}8 = 0$ V, Bias $V = 3.3$ V		2.1	V
I_{LM}	Fall current during prebias	$\overline{B}0$ – $\overline{B}8 = 2$ V, Bias $V = 1.3$ to 2.5 V		1	μ A
I_{HM}	Rise current during prebias	$\overline{B}0$ – $\overline{B}8 = 1$ V, Bias $V = 3$ to 3.6 V		-1	μ A
\overline{I}_{BnPEAK}	Peak bus current during insertion	$V_{CC} = 0$ to 3.3 V, $\overline{B}0$ – $\overline{B}8 = 0$ to 2.0 V, Bias $V = 2.7$ to 3.6 V, OE $\overline{B}0 = 0.8$ V, $t_r = 2$ ns		10	mA
I_{OLOFF}	Power up current	$V_{CC} = 0$ to 3.3 V, OE $\overline{B}0 = 0.8$ V		100	μ A
		$V_{CC} = 0$ to 1.2 V, OE $\overline{B}0 = 0$ to 5 V		100	
t_{GR}	Input glitch rejection	$V_{CC} = 3.3$ V		1.35	ns

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

FBL2041
FBL2041I

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			MIN	TYP ²	MAX	
I _{OH}	High level output current	$\overline{B0} - \overline{B6}$ V _{CC} = MAX, V _{IL} = MAX, V _{OH} = 1.9V			100	μA
I _{OFF}	Power-off output current	$\overline{B0} - \overline{B6}$ V _{CC} = 0V, V _{IL} = MAX, V _{OH} = 1.9V			100	μA
		$\overline{B0} - \overline{B6}$ V _{CC} = 0V, V _{IL} = MAX, V _{OH} = 1.9V @ 85°C			300	μA
V _{OH}	High-level output voltage	A00 – AO6 ³ V _{CC} = MIN to MAX; I _{OH} = -100μA	V _{CC} - 0.2			V
		A00 – AO6 ³ V _{CC} = MIN; I _{OH} = -8mA	2.4			V
		A00 – AO6 ³ V _{CC} = MIN; I _{OH} = -32mA	2.0			V
V _{OL}	Low-level output voltage	A00 – AO6 ³ V _{CC} = MIN; I _{OL} = 16mA			0.4	V
		A00 – AO6 ³ V _{CC} = MIN; I _{OL} = 32mA			0.5	V
		$\overline{B0} - \overline{B6}$ V _{CC} = MIN, I _{OL} = 4mA	0.5			V
		$\overline{B0} - \overline{B6}$ V _{CC} = MIN, I _{OL} = 100mA	0.75	1.0	1.20	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK} = -18mA		-0.85	-1.2	V
I _I	Input leakage current	Control pins V _{CC} = 3.6V; V _I = V _{CC} or GND			±1.0	μA
		Control/ AI0 – AI6 V _{CC} = 0V or 3.6V; V _I = 5.5V			10	
		AI0 – AI6 V _{CC} = 3.6V; V _I = V _{CC}			1	
		Note 4 V _{CC} = 3.6V; V _I = 0V			-5	
I _{IH}	High-level input current	$\overline{B0} - \overline{B6}$ V _{CC} = MAX, V _I = 1.9V			100	μA
		$\overline{B0} - \overline{B6}$ V _{CC} = MAX, V _I = 3.5V, note 5	100			mA
		$\overline{B0} - \overline{B6}$ V _{CC} = MAX, V _I = 3.75V @ -40°C	100			mA
I _{IL}	Low-level input current	$\overline{B0} - \overline{B6}$ V _{CC} = MAX, V _I = 0.75V			-100	μA
I _{OZH}	Off-state output current	A00 – AO6 V _{CC} = MAX, V _O = 3V			5	μA
I _{OZL}	Off-state output current	A00 – AO6 V _{CC} = MAX, V _O = 0.5V			-5	μA
I _{CC}	Supply current (total)	I _{CCZ} V _{CC} = MAX		5.2	13.5	mA
		I _{CCB} V _{CC} = MAX, outputs Low or High		3.2	9.0	
		I _{CCL} V _{CC} = MAX, outputs Low		13.5	19.5	
		I _{CCH} V _{CC} = MAX, outputs High		10.7	16.0	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
- All typical values are at V_{CC} = 3.3V, T_A = 25°C.
- Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
- Unused pins are at V_{CC} or GND.
- For B port input voltage between 3 and 5 volt; I_{IH} will be greater than 100mA but the part will continue to function normally (clamping circuit is active).

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

FBL2041
FBL2041I

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS							UNIT
			$T_{amb} = +25^{\circ}\text{C}$, $V_{CC} = 3.3\text{V}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$			FBL2041 COMMERCIAL		FBL2041I INDUSTRIAL		
			MIN	TYP	MAX	$T_{amb} = 0 \text{ to } +70^{\circ}\text{C}$, $V_{CC} = 3.3\text{V}\pm 10\%$, $C_L = 50\text{pF}$, $R_L = 500\Omega$		$T_{amb} = -40 \text{ to } +85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V}\pm 10\%$, $C_L = 50\text{pF}$, $R_L = 500\Omega$		
t_{PLH} t_{PHL}	Propagation delay, \overline{Bn} to AOn	Waveform 1, 2	3.9 4.0	4.8 4.9	5.8 6.0	3.7 3.8	6.4 6.7	2.8 2.7	6.9 7.0	ns
t_{PZH} t_{PZL}	Output enable time, OEA to AOn	Waveform 4, 5	5.3 2.4	6.6 4.4	8.0 8.0	5.0 2.1	8.6 8.5	4.5 1.1	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time, OEA to AOn	Waveform 4, 5	3.5 2.3	4.8 3.1	6.0 3.9	3.4 2.2	6.5 4.3	2.7 1.4	7.0 4.7	ns
t_{TLH} t_{THL}	Transition time, AOn Port (10% to 90% or 90% to 10%)	Test Circuit and Waveforms	0.7 0.5	1.8 1.6	3.0 2.0	0.7 0.5	3.0 2.0	0.7 0.5	3.0 2.0	ns
$t_{SK(O)}$	Output skew between receivers in same package ¹	Waveform 3		0.7	1.5		1.5		1.5	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS							UNIT
			$T_{amb} = +25^{\circ}\text{C}$, $V_{CC} = 3.3\text{V}$, $C_D = 30\text{pF}$, $R_U = 9\Omega$			$T_{amb} = 0 \text{ to } +70^{\circ}\text{C}$, $V_{CC} = 3.3\text{V}\pm 10\%$, $C_D = 30\text{pF}$, $R_U = 9\Omega$		$T_{amb} = -40 \text{ to } +85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V}\pm 10\%$, $C_D = 30\text{pF}$, $R_U = 9\Omega$		
			MIN	TYP	MAX					
t_{PLH} t_{PHL}	Propagation delay, \overline{AIn} to \overline{Bn}	Waveform 1, 2	3.3 2.7	4.2 3.5	5.2 4.5	2.9 2.5	6.0 5.0	1.8 1.7	6.7 5.6	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to \overline{Bn}	Waveform 2	4.0 3.4	4.9 4.3	5.8 5.3	3.6 3.1	6.6 6.0	2.8 2.5	7.1 6.4	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB1 to \overline{Bn}	Waveform 1	4.2 2.9	5.1 3.8	6.1 4.7	3.9 2.6	6.9 5.5	2.9 1.9	7.3 6.0	ns
t_{TLH} t_{THL}	Transition time, \overline{Bn} Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.2 0.4	2.4 0.9	3.0 1.5	1.2 0.4	3.0 1.5	1.2 0.4	3.0 1.5	ns
$t_{SK(O)}$	Output skew between drivers in same package ¹	Waveform 3			1.5		1.5		1.5	ns
SYMBOL	PARAMETER	TEST CONDITION	$R_U = 16.5\Omega$			$R_U = 16.5\Omega$		$R_U = 16.5\Omega$		UNIT
			MIN	TYP	MAX					
			t_{PLH} t_{PHL}	Propagation delay, \overline{AIn} to \overline{Bn}	Waveform 1, 2	3.3 2.7	4.2 3.6	5.1 4.5	3.0 2.5	
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to \overline{Bn}	Waveform 2	4.0 3.4	4.9 4.3	5.8 5.3	3.6 3.1	6.6 6.0	2.7 2.5	7.1 6.4	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB1 to \overline{Bn}	Waveform 1	4.2 2.9	5.1 3.8	6.1 4.7	3.9 2.6	6.8 5.5	3.0 1.9	7.3 6.0	ns
t_{TLH} t_{THL}	Transition time, \overline{Bn} Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.2 0.4	2.4 0.9	3.0 1.5	1.2 0.4	3.0 1.5	1.2 0.4	3.0 1.5	ns
$t_{SK(O)}$	Output skew between drivers in same package ¹	Waveform 3			1.5		1.5		1.5	ns

NOTES:

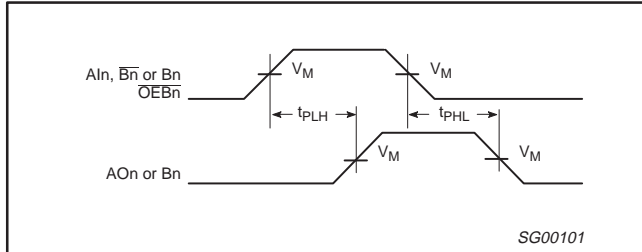
- $|t_{PN\text{actual}} - t_{PM\text{actual}}|$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC} , loading, etc.).

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

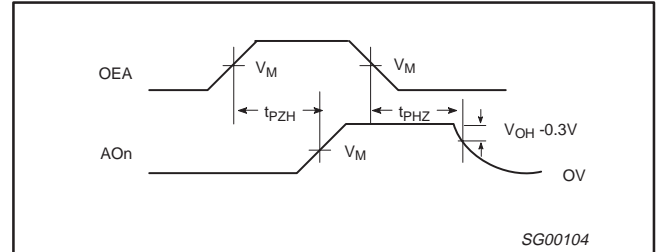
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AC WAVEFORMS

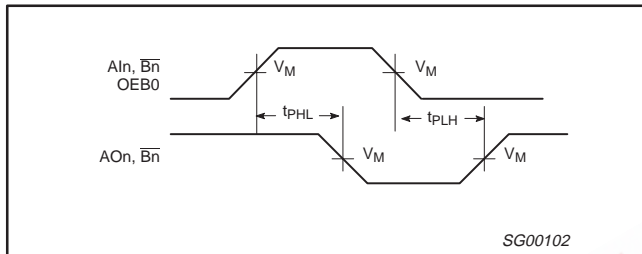
$V_M = 1.55V$ for \overline{Bn} , $V_M = 1.5V$ for all others.



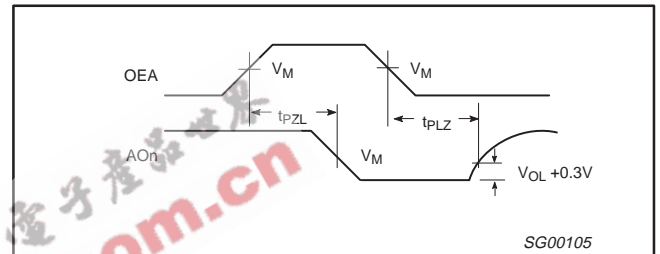
Waveform 1. Propagation Delay for Data or Output Enable to Output



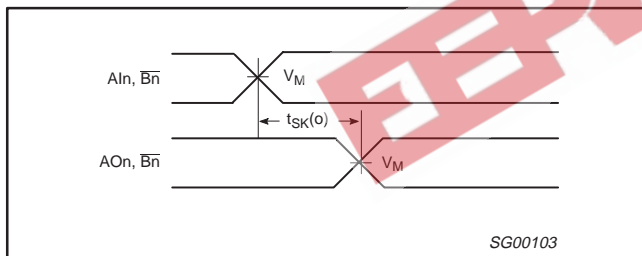
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Propagation Delay for Data or Output Enable to Output



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

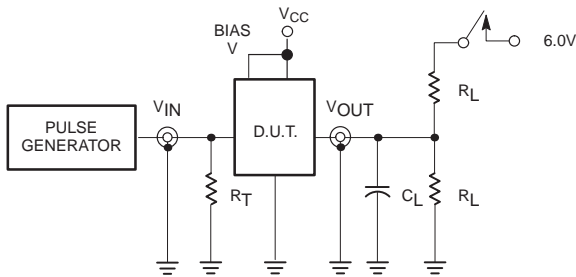


Waveform 3. Output Skews

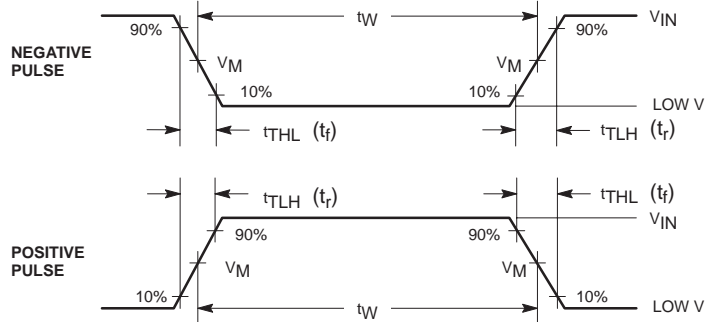
3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

FBL2041
FBL2041I

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs on A Port



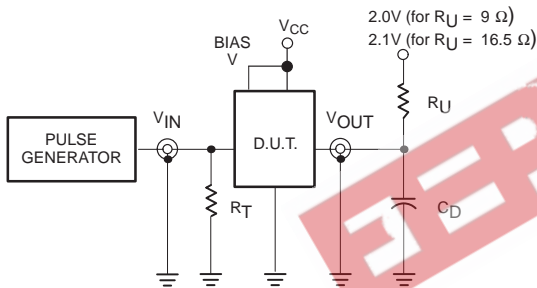
$V_M = 1.55V$ for Bn, $V_M = 1.5V$ for all others.

Input Pulse Definitions

SWITCH POSITION FOR ALL A-PORTS

TEST	SWITCH
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}, t_{PZL}	CLOSED
t_{PHZ}, t_{PZH}	GND

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_w	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.5ns	2.5ns



Test Circuit for Outputs on B Port

DEFINITIONS:

- R_L = Load Resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
- C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_U = Pull up resistor; see AC CHARACTERISTICS for value.

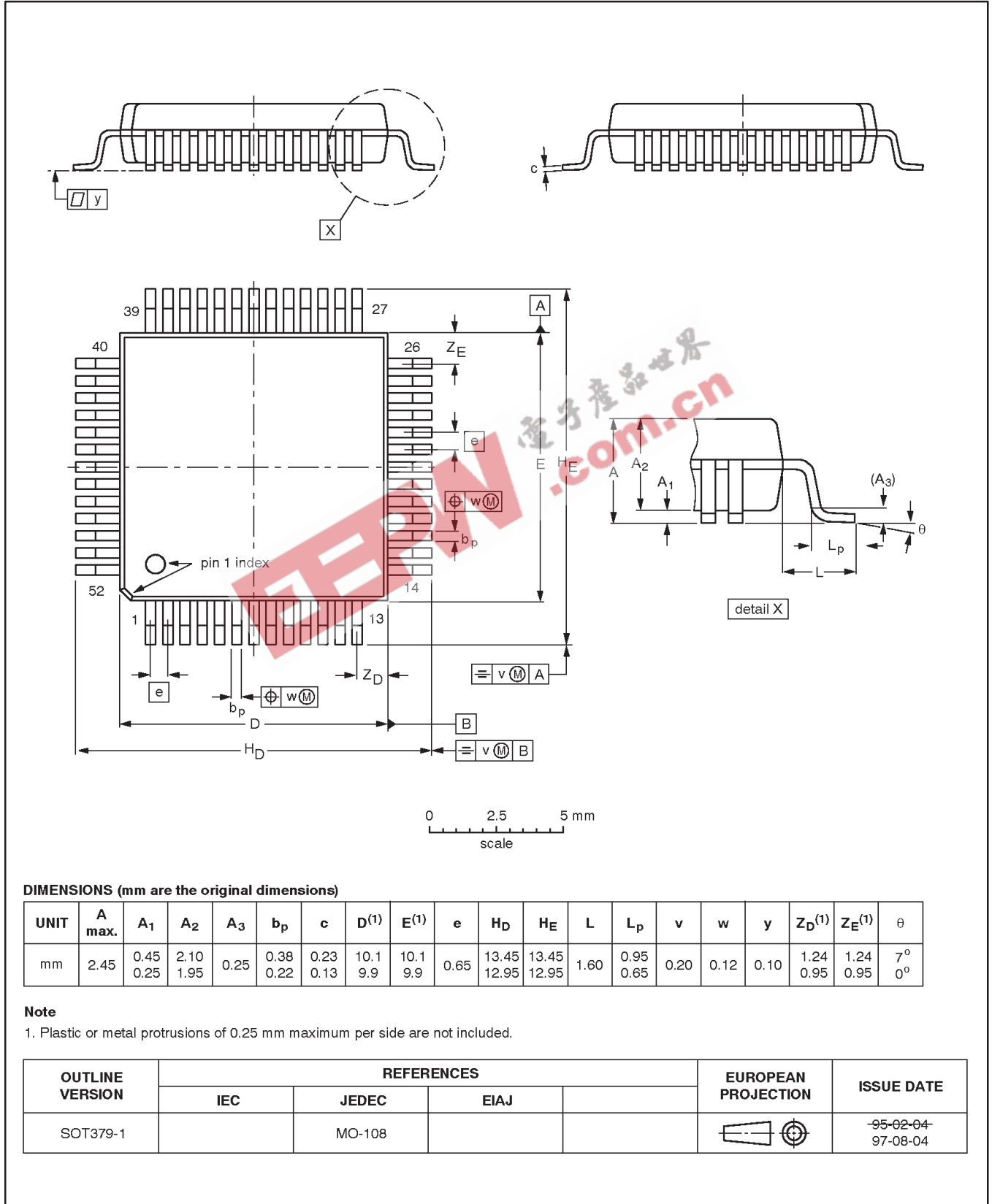
SG00090

3.3V BTL 7-bit Futurebus+ transceiver (standard A port)

FBL2041
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QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm

SOT379-1



3.3V BTL 7-bit Futurebus+ transceiver (standard A port)

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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