



**Document Title**

32K x 8 Low Power SRAM with 3.3V

**Revision History**

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0A	Initial Draft	October 5,2001	



## 32K x 8 LOW VOLTAGE STATIC RAM

### FEATURES

- Access time: 45, 70, 100 ns
- Low active power: 70 mW
- Low standby power
  - 60  $\mu$ W CMOS standby
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 3.3V power supply

### DESCRIPTION

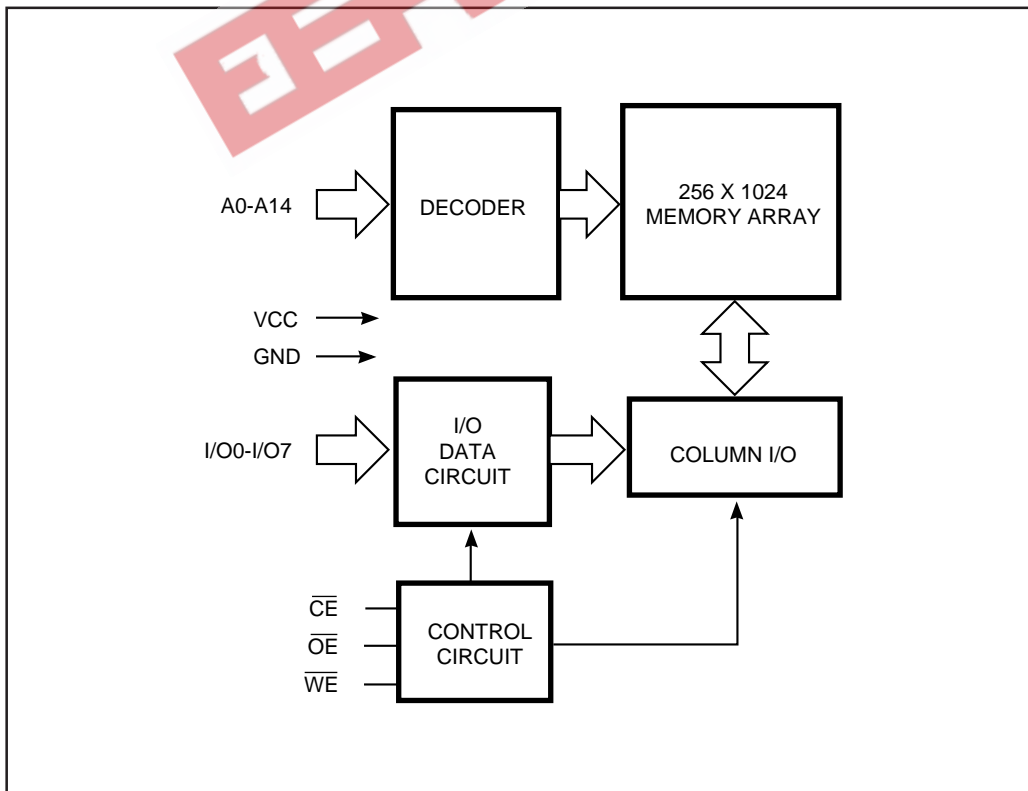
The *ICSI* IC62LV256 is a low power, 32, 768-word by 8-bit static RAM. It is fabricated using *ICSI*'s high-performance CMOS double-metal technology.

When  $\overline{CE}$  is HIGH (deselected), the device assumes a standby mode at which the power dissipation is reduced to 20  $\mu$ W (typical) with CMOS input levels.

Easy memory expansion is provided by using an active LOW Chip Enable ( $\overline{CE}$ ) input and an active LOW Output Enable ( $\overline{OE}$ ) input. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory.

The IC62LV256 is pin compatible with other 32K x 8 SRAMs in 300mil DIP and SOJ, 330mil SOP, and 8\*13.4mm TSOP-1 packages.

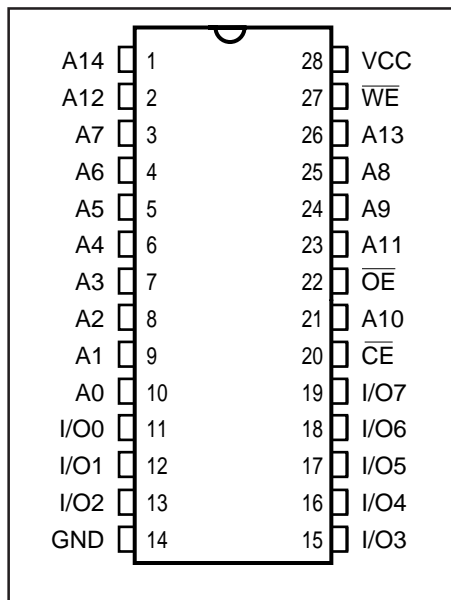
### FUNCTIONAL BLOCK DIAGRAM



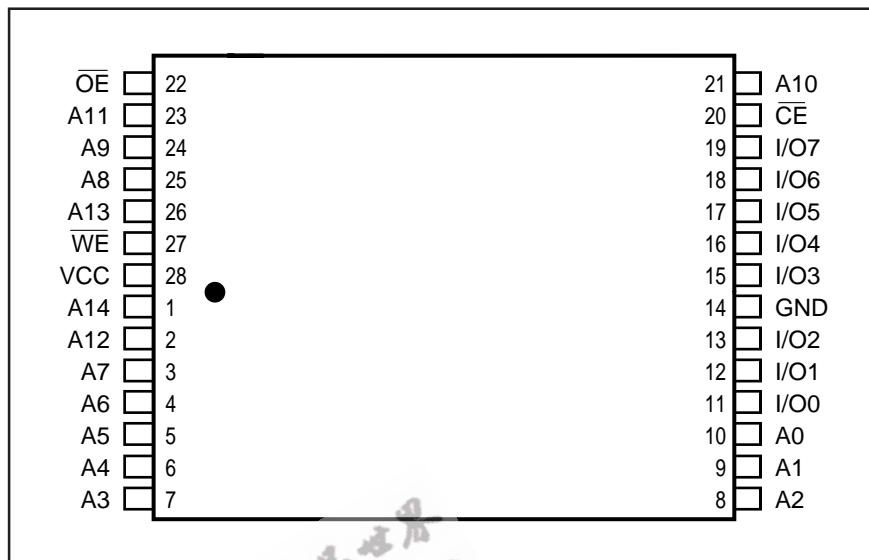
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# IC62LV256

## PIN CONFIGURATION 28-Pin DIP, SOJ and SOP



## PIN CONFIGURATION 8x13.4mm TSOP-1



## PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

## TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	High-Z	I <sub>CC1</sub> , I <sub>CC2</sub>
Read	H	L	L	D <sub>OUT</sub>	I <sub>CC1</sub> , I <sub>CC2</sub>
Write	L	L	X	D <sub>IN</sub>	I <sub>CC1</sub> , I <sub>CC2</sub>

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	W
I <sub>OUT</sub>	DC Output Current (LOW)	20	mA

### Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING RANGE**

Range	Ambient Temperature	V <sub>cc</sub>
Commercial	0°C to +70°C	3.3V ± 5%
Industrial	-40°C to +85°C	3.3V ± 5%

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.4	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.1 mA	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	Com. -2 Ind. -5	2 5	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Outputs Disabled	Com. -2 Ind. -5	2 5	μA

**Notes:**

- V<sub>IL</sub> = -3.0V for pulse width less than 10 ns.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	Test Conditions		-45 ns		-70 ns		-100 ns		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CC1</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., CE = V <sub>IL</sub> I <sub>OUT</sub> = 0 mA, f = 0	Com.	—	20	—	20	—	20	mA
			Ind.	—	30	—	30	—	30	
I <sub>CC2</sub>	V <sub>CC</sub> Dynamic Operating Supply Current	V <sub>CC</sub> = Max., CE = V <sub>IL</sub> I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	—	35	—	30	—	30	mA
			Ind.	—	45	—	40	—	40	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> CE ≥ V <sub>IH</sub> , f = 0	Com.	—	2	—	2	—	2	mA
			Ind.	—	5	—	5	—	5	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>CC</sub> = Max., CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com.	—	90	—	90	—	90	μA
			Ind.	—	200	—	200	—	200	

**Notes:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**CAPACITANCE<sup>(1,2)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5	pF

**Notes:**

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 3.3V.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

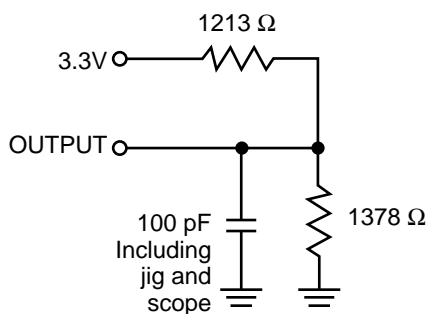
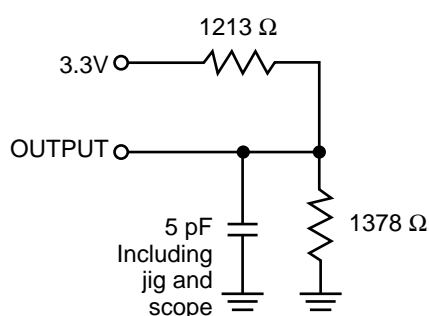
Symbol	Parameter	-45 ns		-70 ns		-100 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	45	—	70	—	100	—	ns
t <sub>AA</sub>	Address Access Time	—	45	—	70	—	100	ns
t <sub>OH</sub>	Output Hold Time	2	—	2	—	2	—	ns
t <sub>ACE</sub>	$\overline{CE}$ Access Time	—	45	—	70	—	100	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	25	—	35	—	50	ns
t <sub>LZOE<sup>(2)</sup></sub>	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	ns
t <sub>HZOE<sup>(2)</sup></sub>	$\overline{OE}$ to High-Z Output	0	20	0	25	0	25	ns
t <sub>LZCE<sup>(2)</sup></sub>	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	ns
t <sub>HZCE<sup>(2)</sup></sub>	$\overline{CE}$ to High-Z Output	0	20	0	25	0	25	ns
t <sub>PU<sup>(3)</sup></sub>	$\overline{CE}$ to Power-Up	0	—	0	—	0	—	ns
t <sub>PD<sup>(3)</sup></sub>	$\overline{CE}$ to Power-Down	—	30	—	50	—	50	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

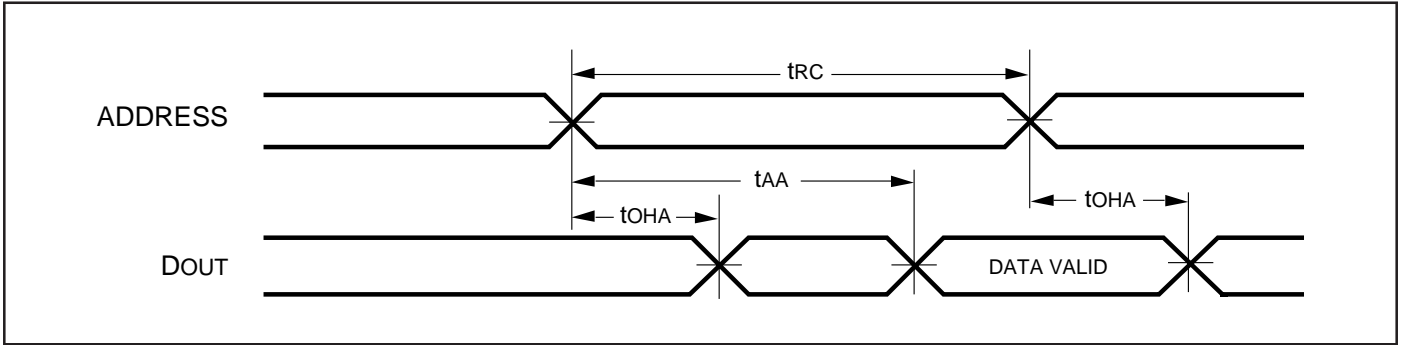
**AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1a and 1b

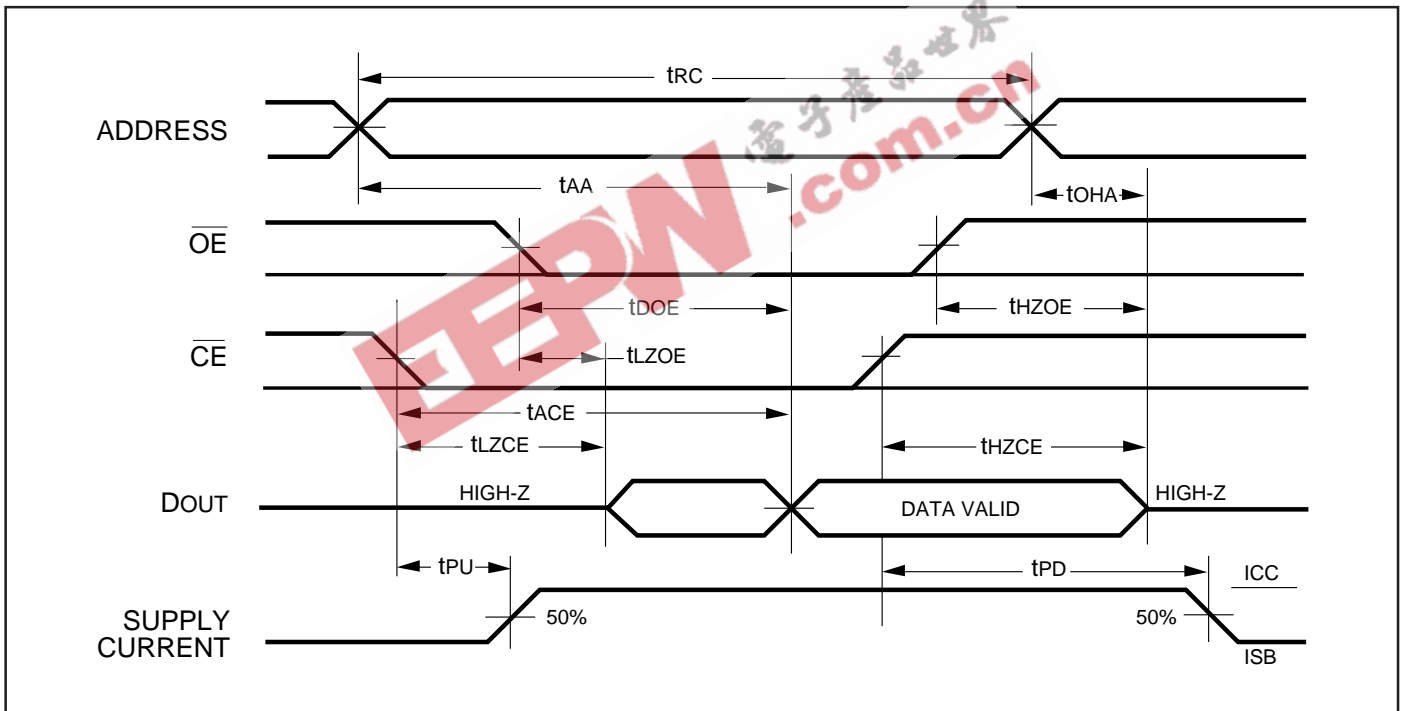
**AC TEST LOADS**

**Figure 1a.**

**Figure 1b.**

AC WAVEFORMS

READ CYCLE NO. 1<sup>(1,2)</sup>



READ CYCLE NO. 2<sup>(1,3)</sup>



Notes:

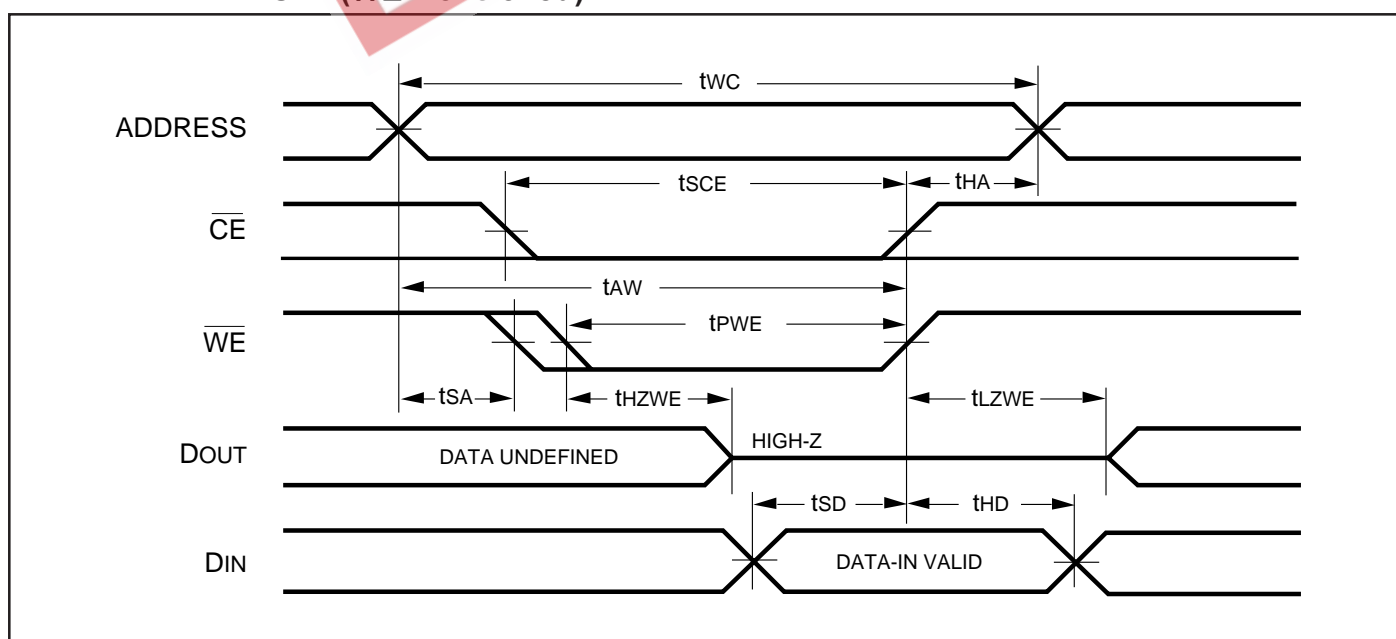
1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE}$  LOW transitions.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2,3)</sup> (Over Operating Range)**

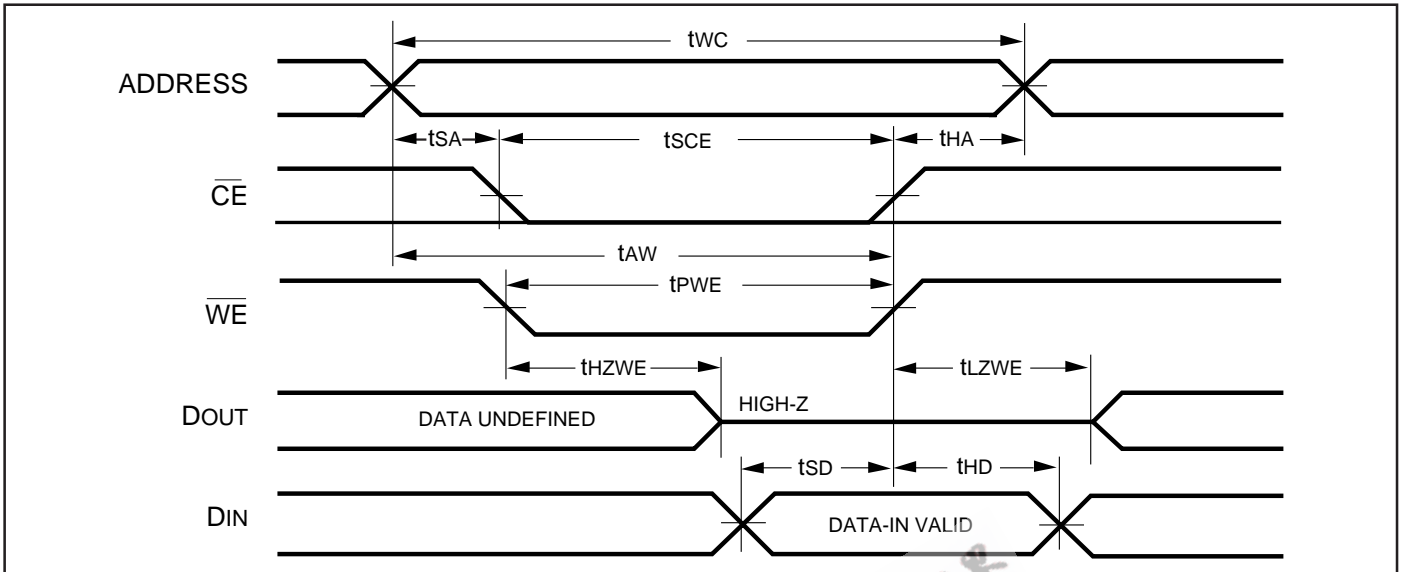
Symbol	Parameter	-45 ns		-70 ns		-100 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	45	—	70	—	100	—	ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ to Write End	35	—	60	—	80	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	25	—	60	—	80	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	0	—	ns
t <sub>PWE<sup>(4)</sup></sub>	$\overline{\text{WE}}$ Pulse Width	25	—	55	—	60	—	ns
t <sub>SD</sub>	Data Setup to Write End	20	—	30	—	35	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	0	—	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with  $\text{OE}$  HIGH.

**AC WAVEFORMS**
**WRITE CYCLE NO. 1 ( $\overline{\text{WE}}$  Controlled)<sup>(1,2)</sup>**


WRITE CYCLE NO. 2 ( $\overline{CE}$  Controlled)<sup>(1,2)</sup>



Notes:

1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} \geq V_{IH}$ .





**ORDERING INFORMATION**

**Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
45	IC62LV256-45N	300mil DIP
45	IC62LV256-45J	300mil SOJ
45	IC62LV256-45T	8*13.4mm TSOP-1
45	IC62LV256-45U	330mil SOP
70	IC62LV256-70N	300mil DIP
70	IC62LV256-70J	300mil SOJ
70	IC62LV256-70T	8*13.4mm TSOP-1
70	IC62LV256-70U	330mil SOP
100	IC62LV256-100N	300mil DIP
100	IC62LV256-100J	300mil SOJ
100	IC62LV256-100T	8*13.4mm TSOP-1
100	IC62LV256-100U	330mil SOP

**ORDERING INFORMATION**

**Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
45	IC62LV256-45JI	300mil SOJ
45	IC62LV256-45TI	8*13.4mm TSOP-1
45	IC62LV256-45UI	330mil SOP
70	IC62LV256-70JI	300mil SOJ
70	IC62LV256-70TI	8*13.4mm TSOP-1
70	IC62LV256-70UI	330mil SOP
100	IC62LV256-100JI	300mil SOJ
100	IC62LV256-100TI	8*13.4mm TSOP-1
100	IC62LV256-100UI	330mil SOP



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