MC74LCX125

Low-Voltage CMOS Quad Buffer

With 5 V−Tolerant Inputs and Outputs (3−State, Non−Inverting)

The MC74LCX125 is a high performance, non−inverting quad buffer operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX125 inputs to be safely driven from 5.0 V devices. The MC74LCX125 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Current drive capability is 24 mA at the outputs. The Output Enable ($\overline{OE}$n) inputs, when HIGH, disable the outputs by placing them in a HIGH Z condition.

Features

- Designed for 2.3 to 3.6 V V_{CC} Operation
- 5.0 V Tolerant − Interface Capability With 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0 V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in all Three Logic States (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V
  Machine Model >200 V
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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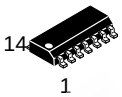
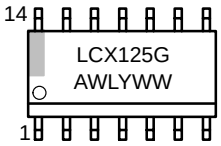
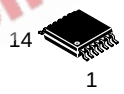
http://onsemi.com

MARKING DIAGRAMS

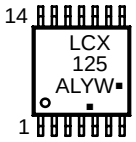


SOIC−14
D SUFFIX
CASE 751A





TSSOP−14
DT SUFFIX
CASE 948G



A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G	= Pb−Free Package
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

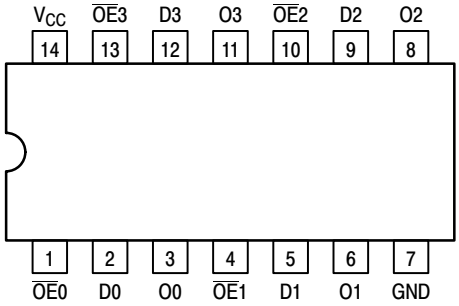


Figure 1. Pinout: 14−Lead (Top View)

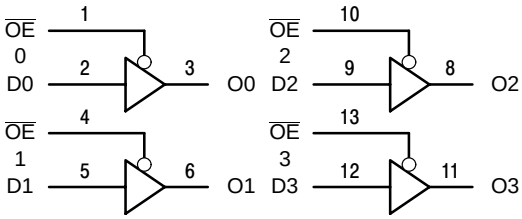


Figure 2. Logic Diagram

PIN NAMES

Pins	Function
$\overline{OE}$n	Output Enable Inputs
Dn	Data Inputs
On	3−State Outputs

TRUTH TABLE

INPUTS		OUTPUTS
$\overline{OE}$n	Dn	On
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance State
X = High or Low Voltage Level and Transitions Are Acceptable; for I_{CC} reasons, DO NOT FLOAT Inputs

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	Output in 3−State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$	Output in HIGH or LOW State. (Note 1)	V
I_{IK}	DC Input Diode Current	−50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	−50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	−65 to +150		°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	2.5, 3.3 2.5, 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State) (3−State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current	V_{CC} = 3.0 V − 3.6 V V_{CC} = 2.7 V − 3.0 V V_{CC} = 2.3 V − 2.7 V			− 24 − 12 − 8	mA
I_{OL}	LOW Level Output Current	V_{CC} = 3.0 V − 3.6 V V_{CC} = 2.7 V − 3.0 V V_{CC} = 2.3 V − 2.7 V			+ 24 + 12 + 8	mA
T_A	Operating Free−Air Temperature		−40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = −40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V_{CC} ≤ 2.7 V	1.7		V
		2.7 V ≤ V_{CC} ≤ 3.6 V	2.0		
V_{IL}	LOW Level Input Voltage (Note 2)	2.3 V ≤ V_{CC} ≤ 2.7 V		0.7	V
		2.7 V ≤ V_{CC} ≤ 3.6 V		0.8	
V_{OH}	HIGH Level Output Voltage	2.3 V ≤ V_{CC} ≤ 3.6 V; I_{OL} = 100 μA	V_{CC} − 0.2		V
		V_{CC} = 2.3 V; I_{OH} = −8 mA	1.8		
		V_{CC} = 2.7 V; I_{OH} = −12 mA	2.2		
		V_{CC} = 3.0 V; I_{OH} = −18 mA	2.4		
		V_{CC} = 3.0 V; I_{OH} = −24 mA	2.2		
V_{OL}	LOW Level Output Voltage	2.3 V ≤ V_{CC} ≤ 3.6 V; I_{OL} = 100 μA		0.2	V
		V_{CC} = 2.3 V; I_{OL}= 8 mA		0.6	
		V_{CC} = 2.7 V; I_{OL}= 12 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 16 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 24 mA		0.55	
I_I	Input Leakage Current	2.3 V ≤ V_{CC} ≤ 3.6 V; 0 V ≤ V_I ≤ 5.5 V		±5	μA
I_{CC}	Quiescent Supply Current	2.3 ≤ V_{CC} ≤ 3.6 V; V_I = GND or V_{CC}		10	μA
		2.3 ≤ V_{CC} ≤ 3.6 V; 3.6 ≤ V_I or V_O ≤ 5.5 V		±10	
ΔI_{CC}	Increase in I_{CC} per Input	2.3 ≤ V_{CC} ≤ 3.6 V; V_{IH} = V_{CC} − 0.6 V		500	μA

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS $t_R = t_F = 2.5$ ns; $R_L = 500\ \Omega$

Symbol	Parameter	Waveform	Limits						Unit
			$T_A = -40°C$ to $+85°C$						
			$V_{CC} = 3.3\ V \pm 0.3\ V$		$V_{CC} = 2.7\ V$		$V_{CC} = 2.5\ V \pm 0.2\ V$		
			$C_L = 50$ pF		$C_L = 50$ pF		$C_L = 30$ pF		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Time Input to Output	1	1.5 1.5	6.0 6.0	1.5 1.5	6.5 6.5	1.5 1.5	7.2 7.2	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	1.5 1.5	9.1 9.1	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	1.5 1.5	7.2 7.2	ns
t_{OSHL} t_{OSLH}	Output−to−Output Skew (Note 3)			1.0 1.0					ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 4)	$V_{CC} = 3.3$ V, $C_L = 50$ pF, $V_{IH} = 3.3$ V, $V_{IL} = 0$ V $V_{CC} = 2.5$ V, $C_L = 30$ pF, $V_{IH} = 2.5$ V, $V_{IL} = 0$ V		0.8 0.6		V V
V_{OLV}	Dynamic LOW Valley Voltage (Note 4)	$V_{CC} = 3.3$ V, $C_L = 50$ pF, $V_{IH} = 3.3$ V, $V_{IL} = 0$ V $V_{CC} = 2.5$ V, $C_L = 30$ pF, $V_{IH} = 2.5$ V, $V_{IL} = 0$ V		−0.8 −0.6		V V

4. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.

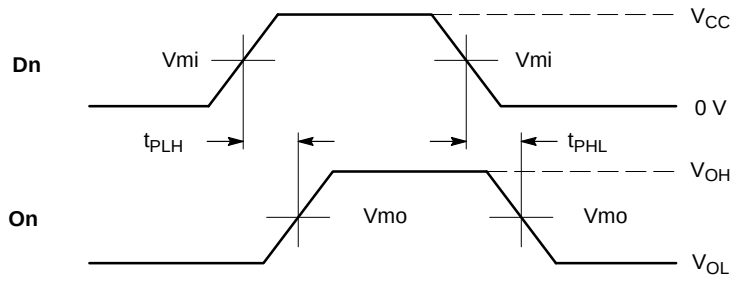
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 3.3$ V, $V_I = 0$ V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3$ V, $V_I = 0$ V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10 MHz, $V_{CC} = 3.3$ V, $V_I = 0$ V or V_{CC}	25	pF

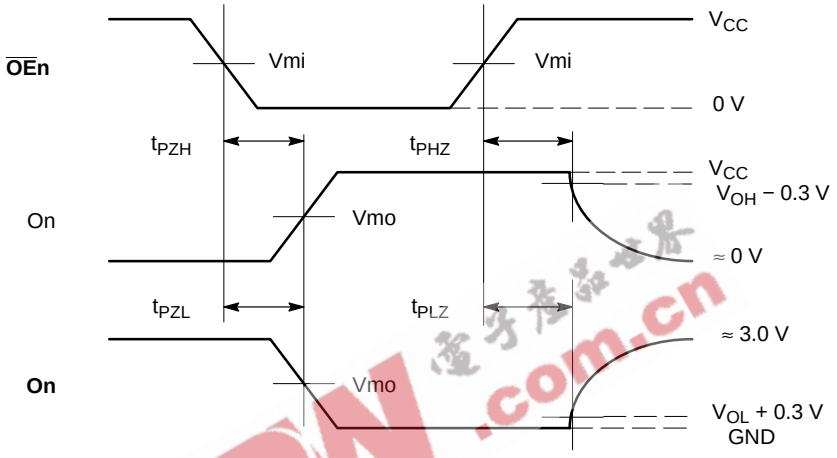
ORDERING INFORMATION

Device	Package	Shipping†
MC74LCX125D	SOIC−14	55 Units / Rail
MC74LCX125DG	SOIC−14 (Pb−Free)	55 Units / Rail
MC74LCX125DR2	SOIC−14	2500 Tape & Reel
MC74LCX125DR2G	SOIC−14 (Pb−Free)	2500 Tape & Reel
MC74LCX125DT	TSSOP−14*	96 Units / Rail
MC74LCX125DTG	TSSOP−14*	96 Units / Rail
MC74LCX125DTR2	TSSOP−14*	2500 Tape & Reel
MC74LCX125DTR2G	TSSOP−14*	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.



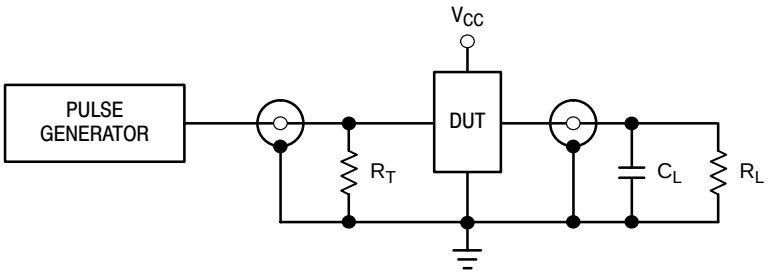
WAVEFORM 1 − PROPAGATION DELAYS
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 2 − OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

	V_{CC}		
Symbol	3.3 V ± 0.3 V	2.7 V	2.5 V ± 0.2 V
Vmi	1.5 V	1.5 V	$V_{CC}/2$
Vmo	1.5 V	1.5 V	$V_{CC}/2$

Figure 3. AC Waveforms

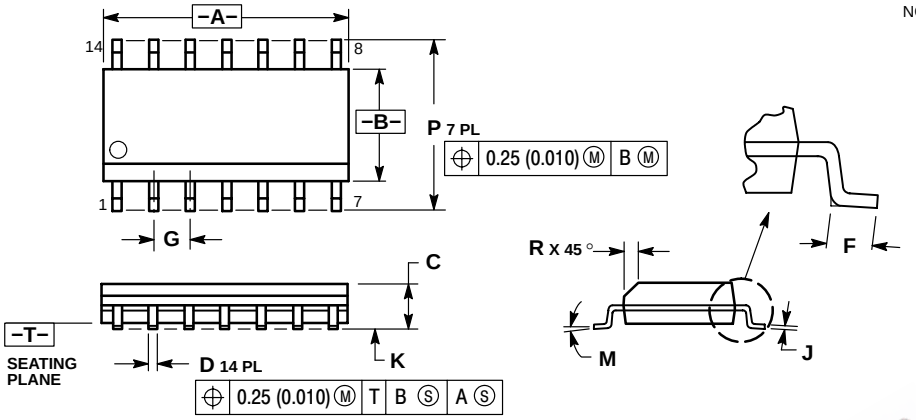


C_L = 50 pF at V_{CC} = 3.3 ±0.3 V or equivalent (includes jig and probe capacitance)
C_L = 30 pF at V_{CC} = 2.5 ±0.2 V or equivalent (includes jig and probe capacitance)
R_L = R_1 = 500 Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 4. Test Circuit

PACKAGE DIMENSIONS

SOIC−14
D SUFFIX
CASE 751A−03
ISSUE G

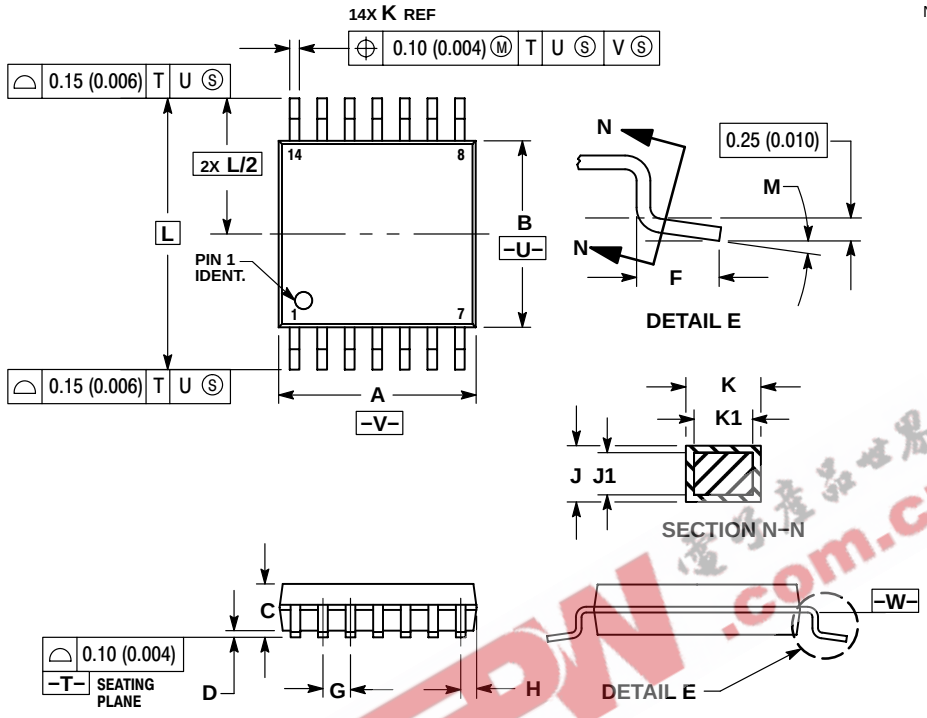


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

TSSOP−14
DT SUFFIX
CASE 948G−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

MC74LCX125

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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