Octal 3-State Noninverting Transparent Latch with LSTTL Compatible Inputs

High-Performance Silicon-Gate CMOS

The MC74HCT573A is identical in pinout to the LS573. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold times becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT573A is identical in function to the HCT373A but has the Data Inputs on the opposite side of the package from the outputs to facilitate PC board layout.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 10 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates
 - Improved Propagation Delays
 - 50% Lower Quiescent Power
- These devices are available in Pb-free package(s). Specifications herein
 apply to both standard and Pb-free devices. Please see our website at
 www.onsemi.com for specific Pb-free orderable part numbers, or
 contact your local ON Semiconductor sales office or representative.



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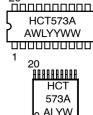
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MARKING DIAGRAMS









HHHHHHHHH



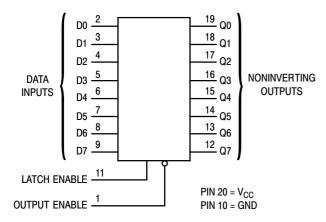
TSSOP-20 DT SUFFIX CASE 948E



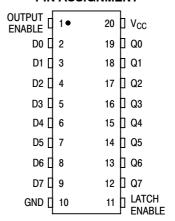
ORDERING INFORMATION

Device	Package	Shipping
MC74HCT573AN	PDIP-20	1440 / Box
MC74HCT573ADW	SOIC-WIDE	38 / Rail
MC74HCT573ADWR2	SOIC-WIDE	1000 / Reel
MC74HCT573ADT	TSSOP-20	75 / Rail
MC74HCT573ADTR2	TSSOP-20	2500 / Reel

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

	Inputs				
Output Enable	Latch Enable	D	Q		
L	Н	Н	Н		
L	Н	L	L		
L	L	Х	No Change		
Н	Х	Х	Z		

	Enable	Enable	D	(Q			
	L	Н	Н	I	Η			
	L	Н	L		L			- 1
	L	L	Χ	No C	hange			3,35,7
	Н	Х	Х		Z			张 30
	X = Don'	t Care						2 多多···································
	Z = High	Impedano	е					
								~0"
	Desi	gn Criteri	а		Valu	e	Units	.0
Intern	al Gate Co	ount*			58.5		ea	
Intern	al Gate Pr	opagation	Delay		1.5		ns	
Intern	al Gate Po	ower Dissi	pation		5.0		μW	
	d Power P	roduct		MAND	0.007	'5	рЈ	

^{*}Equivalent to a two-input NAND gate.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±[2 0	mA
l _{out}	DC Output Current, per Pin	±[2 5	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±[5 0	mA
P _D	Power Dissipation in Still Air Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, TSSOP or SOIC Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

SOIC Package: -7 mW/°C from 65° to 125° C

TSSOP Package: -6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	٧
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Gu			
Symbol	Paramet <mark>e</mark> r	Test Conditions	V _{CC}	– 55 to 25°C	≤ 85 °C	≤ 125°C	Unit
V _{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} - 0.1 V $ I_{out} \le 20 \mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $ I_{out} \le 20 \mu A$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \ \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 6.0 \text{ mA}$	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \ \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 6.0 \text{ mA}$	4.5	0.26	0.33	0.4	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5	±[0.1	±∏1.0	±]1.0	μΑ
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	5.5	±[0.5	±[5.0	±[10	μΑ
I _{CC}	Maximum Quiescent Supply Current (per Package)	$\begin{aligned} V_{in} &= V_{CC} \text{ or GND} \\ I_{out} &\leq 0 \ \mu A \end{aligned}$	5.5	4.0	40	160	μΑ
Δl _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4 V, Any One Input V _{in} = V _{CC} or GND, Other Inputs		≥ - 55°C	25°C to	125°C	
	Curron	I _{out} = 0 μA	5.5	2.9	2	.4	mA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

^{*}Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

[†]Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V \pm 10%, C_L = 50 pF, Input t_{r} = t_{f} = 6.0 ns)

		Guaranteed Limit		mit	
Symbol	Parameter	– 55 to 25° C	≤ 85 °C	≤ 125°C	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input D to Output Q (Figures 1 and 5)	30	38	45	ns
t _{PLH}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	30	38	45	ns
T _{PLZ,} T _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	28	35	42	ns
t _{TZL,}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	28	35	42	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, any Output (Figures 1 and 5)	12	15	18	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

		72: 3P	Турі	cal @ 25°C, V _{CC} = 5.0 V	
C _{PD}	Power Dissipation Capacitance (Per Enabled Output)*	2 3 72	5	48	pF

^{*}Used to determine the no–load dynamic power consumption: $P_D = C_{PD} \, V_{CC}^2 f + I_{CC} \, V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS ($V_{CC} = 5.0 \text{ V} \pm \boxed{10\%}$, $C_L = 50 \text{ pF}$, Input $t_r = t_f = 6.0 \text{ ns}$)

			Gi		Guaranteed Limit				
			– 55 to	25°C	≤ 8	5°C	≤ 12	25°C	
Symbol	Parameter	Fig.	Min	Max	Min	Max	Min	Max	Unit
t _{su}	Minimum Setup Time, Input D to Latch Enable	4	10		13		15		ns
t _h	Minimum Hold Time, Latch Enable to Input D	4	5.0		5.0		5.0		ns
t _w	Minimum Pulse Width, Latch Enable	2	15		19		22		ns
t _r , t _f	Maximum Input Rise and Fall Times	1		500		500		500	ns

SWITCHING WAVEFORMS

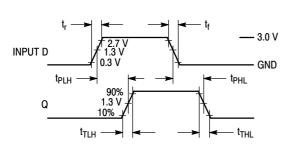


Figure 1.

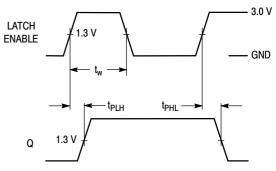


Figure 2.

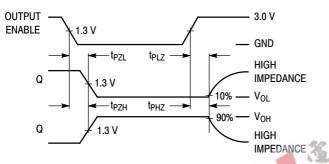


Figure 3.

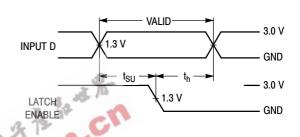
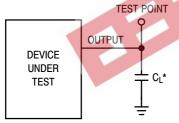


Figure 4.



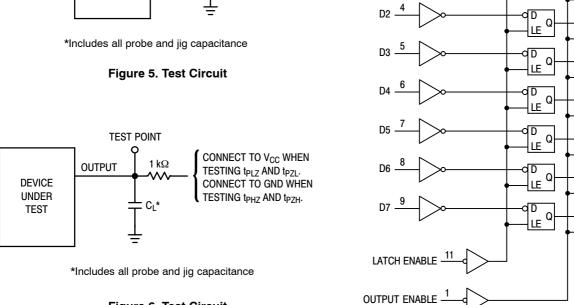


Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM

19 Q0

<u>17</u> Q2

16 Q3

15 Q4

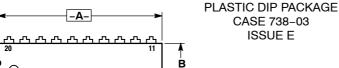
14 Q5

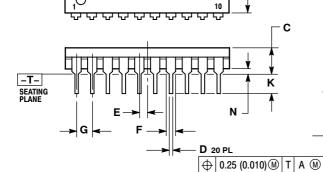
13 Q6

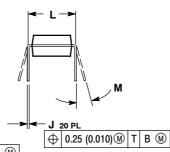
12 Q7

PACKAGE DIMENSIONS

PDIP-20 **N SUFFIX**





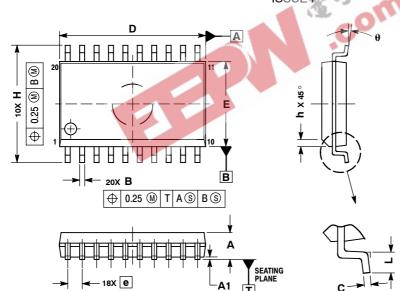


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	1.010	1.070	25.66	27.17	
В	0.240	0.260	6.10	6.60	
С	0.150	0.180	3.81	4.57	
D	0.015	0.022	0.39	0.55	
Е	0.050	BSC	1.27 BSC		
F	0.050	0.070	1.27	1.77	
G	0.100	BSC	2.54	BSC	
J	0.008	0.015	0.21	0.38	
K	0.110	0.140	2.80	3.55	
L	0.300 BSC		7.62	BSC	
M	0°	15°	0°	15°	
N	0.020	0.040	0.51	1.01	

SO-20 **DW SUFFIX**

CASE 751D-05 ISSUE F



NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS. 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- PER ASME 114-50M, 1994.

 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.

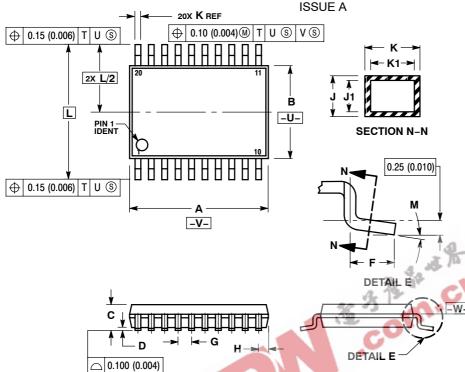
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
- DIMENSION B DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE PROTRUSION SHALL
 BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT
 MAXIMUM MATERIAL CONDITION.

	MILLIMETERS				
DIM	MIN	MAX			
Α	2.35	2.65			
A1	0.10	0.25			
В	0.35	0.49			
С	0.23	0.32			
D	12.65	12.95			
Е	7.40	7.60			
е	1.27	BSC			
Н	10.05	10.55			
h	0.25	0.75			
٦	0.50	0.90			
	• 0	- 0			

PACKAGE DIMENSIONS







NOTES:

- 1. DIMEINO. 2 Y14.5M, 1982. DIMENSIONING AND TOLERANCING PER ANSI
- 114-3/M, 1962.

 CONTROLLING DIMENSION: MILLIMETER.

 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED
- FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION ALLOWABLE DAMBAR PROTRUSION ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION. MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.

 7. DIMENSION A AND B ARE TO BE
 DETERMINED AT DATUM PLANE -W-

	MILLIN	MILLIMETERS		HES	
DIM	MIN	MAX	MIN	MAX	
Α	6.40	6.60	0.252	0.260	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.27	0.37	0.011	0.015	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L		BSC	0.252		
M	0°	8°	0°	8°	

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