DATA SHEET

74F2240
Octal inverter buffer with 30Ω equivalent output termination (3-State)

74F2241
Octal buffer with 30Ω equivalent output termination (3-State)

Product specification

1990 Dec 13

IC15 Data Handbook

Philips
Semiconductors

PHILIPS

Octal buffers 74F2240, 74F2241

FEATURES

- Octal bus interface
- 30Ω output termination ideal for driving DRAM
- 15mA source current

DESCRIPTION

The 74F2240 and 74F2241 are octal buffers that are ideal for driving dynamic DRAM with impedance matching. The outputs are all capable of sinking 5mA and sourcing up to 15mA. The device features two output enables, each controlling four of the 3-state outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F2240	4.3ns	37mA
74F2241	4.5ns	30mA

ORDERING INFORMATION

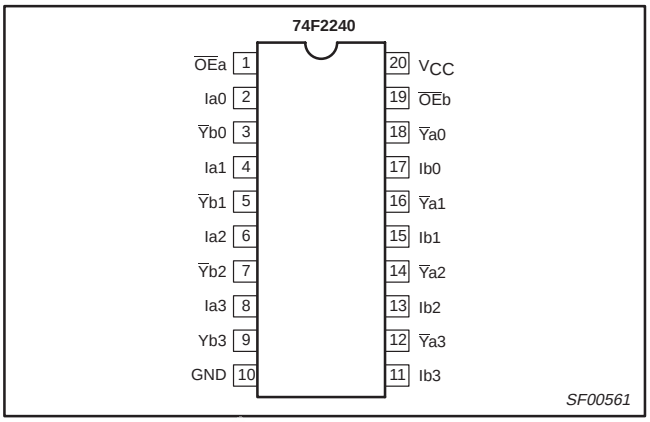
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20-pin plastic DIP	N74F2240N, N74F2241N	SOT146-1
20-pin plastic SOL	N74F2240D, N74F2241D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

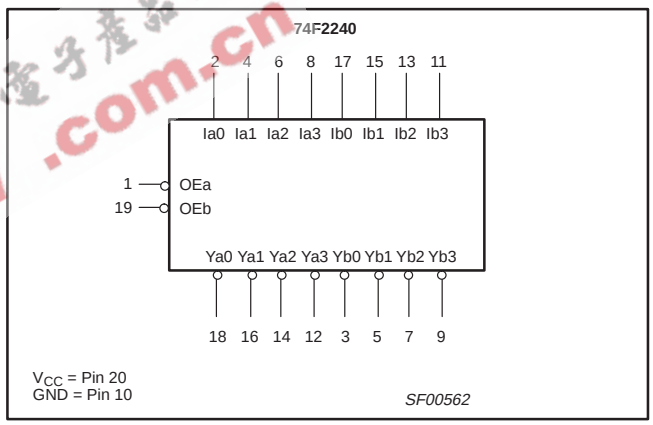
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/0.33	20µA/0.2mA
$\overline{OE}$a, $\overline{OE}$b	Output enable inputs (active Low)	1.0/0.33	20µA/0.2mA
OEb	Output enable input (74F2241)	1.0/0.33	20µA/0.2mA
Yan, Ybn	Data outputs (74F2241)	750/8.33	15mA/5mA
$\overline{Y}$an, $\overline{Y}$bn	Data outputs (74F2240)	750/8.33	15mA/5mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

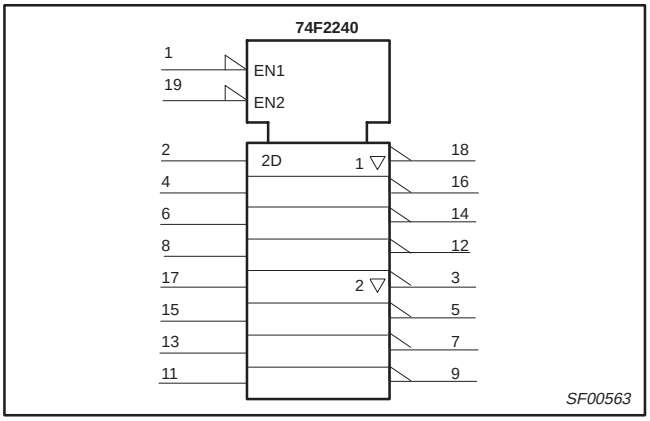
PIN CONFIGURATION



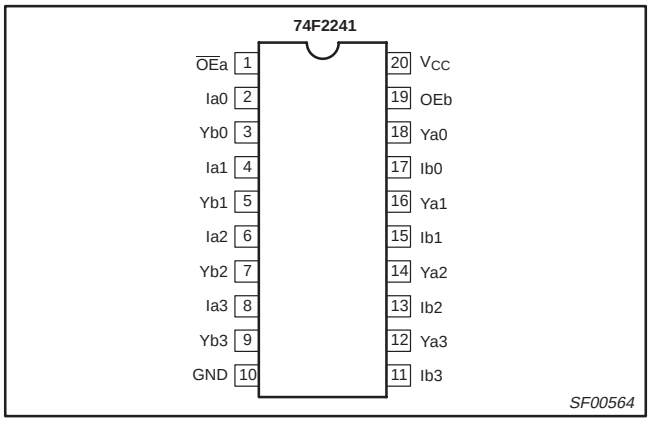
LOGIC SYMBOL



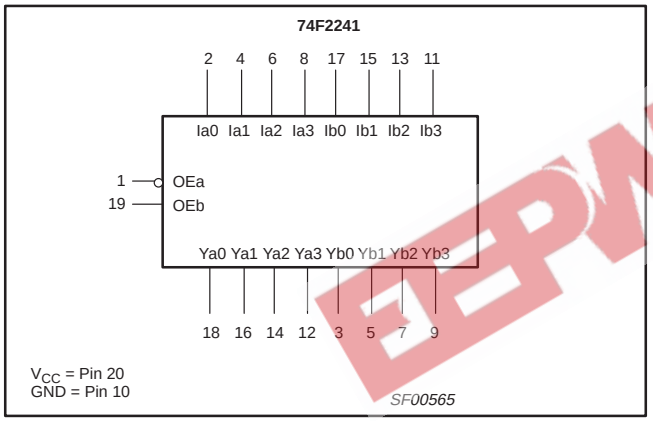
IEC/IEEE SYMBOL



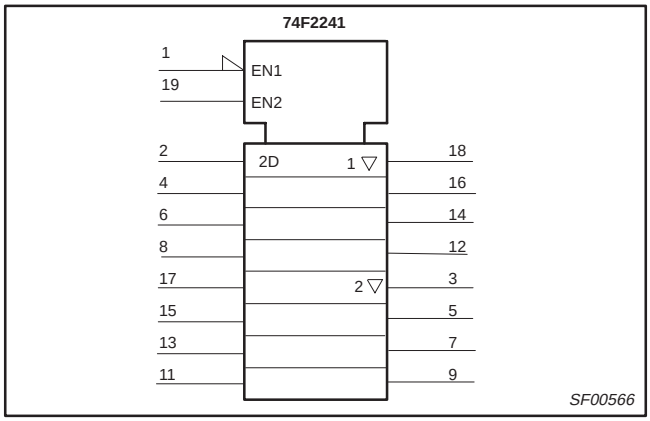
PIN CONFIGURATION



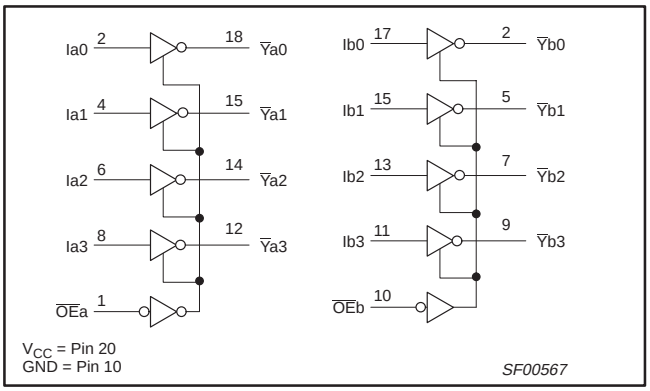
LOGIC SYMBOL



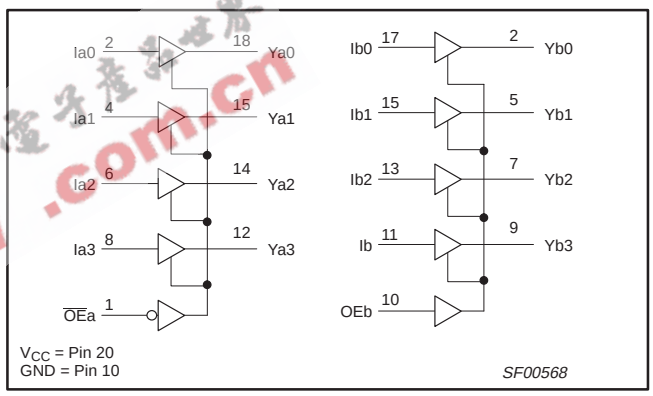
IEC/IEEE SYMBOL



LOGIC DIAGRAM FOR 74F2240



LOGIC DIAGRAM FOR 74F2241



FUNCTION TABLE FOR 74F2240

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	$\overline{Y}a$	$\overline{Y}b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

Notes to function table for 74F2240

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

FUNCTION TABLE FOR 74F2241

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	OEb	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

Notes to function table for 74F2241

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	10	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–15	mA
I_{OL}	Low–level output current			5	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH} = –15mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL} = MAX	±10%V_{CC}			0.50	V
				±5%V_{CC}		0.42	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	V_{CC} = MAX, V_I = 0.5V					–0.2	mA
I_{OZH}	Off–state output current, high–level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off–state output current, low–level voltage applied	V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short–circuit output current[3]	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	74F2240	I_{CCH}	V_{CC} = MAX		25	35	mA
			I_{CCL}			53	75	mA
			I_{CCZ}			35	45	mA
		74F2241	I_{CCH}	V_{CC} = MAX		19	30	mA
			I_{CCL}			45	65	mA
			I_{CCZ}			27	40	mA

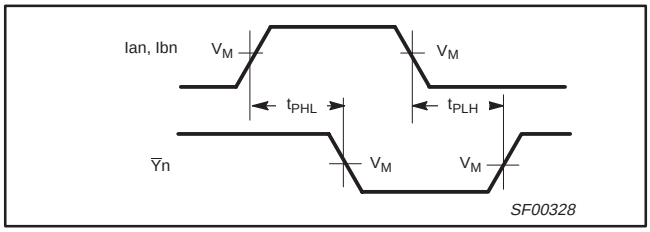
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

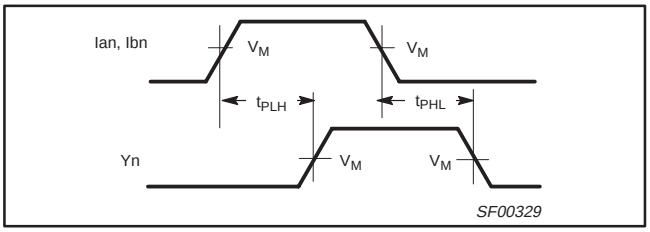
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to $\overline{Y}$n	74F2240	Waveform 1	3.0 2.0	5.0 3.5	7.0 5.5	2.5 2.0	8.0 6.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	3.0 3.5	4.5 5.0	7.0 8.0	2.5 3.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 1.0	3.5 2.5	6.5 5.5	1.5 1.0	7.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	74F2241	Waveform 2	3.0 2.5	4.5 4.5	7.0 6.5	2.5 2.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	3.0 3.5	5.0 5.5	7.0 7.5	2.0 3.0	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 1.5	4.0 3.5	6.0 6.0	1.5 1.0	7.0 6.5	ns

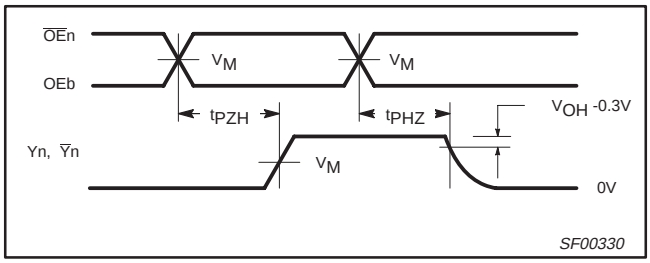
AC WAVEFORMS



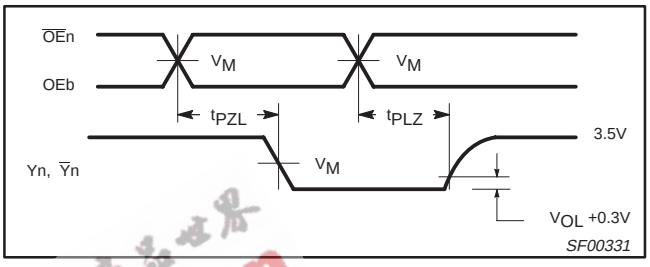
Waveform 1. Propagation delay for inverting outputs



Waveform 2. Propagation delay for non–inverting outputs



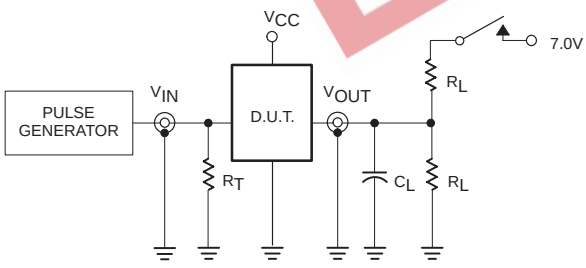
Waveform 3. 3-state output enable time to high level and output disable time from high level



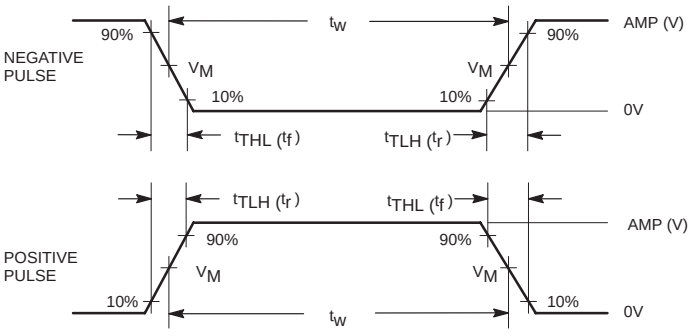
Waveform 4. 3-state output enable time to low level and output disable time from low level

NOTES:
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

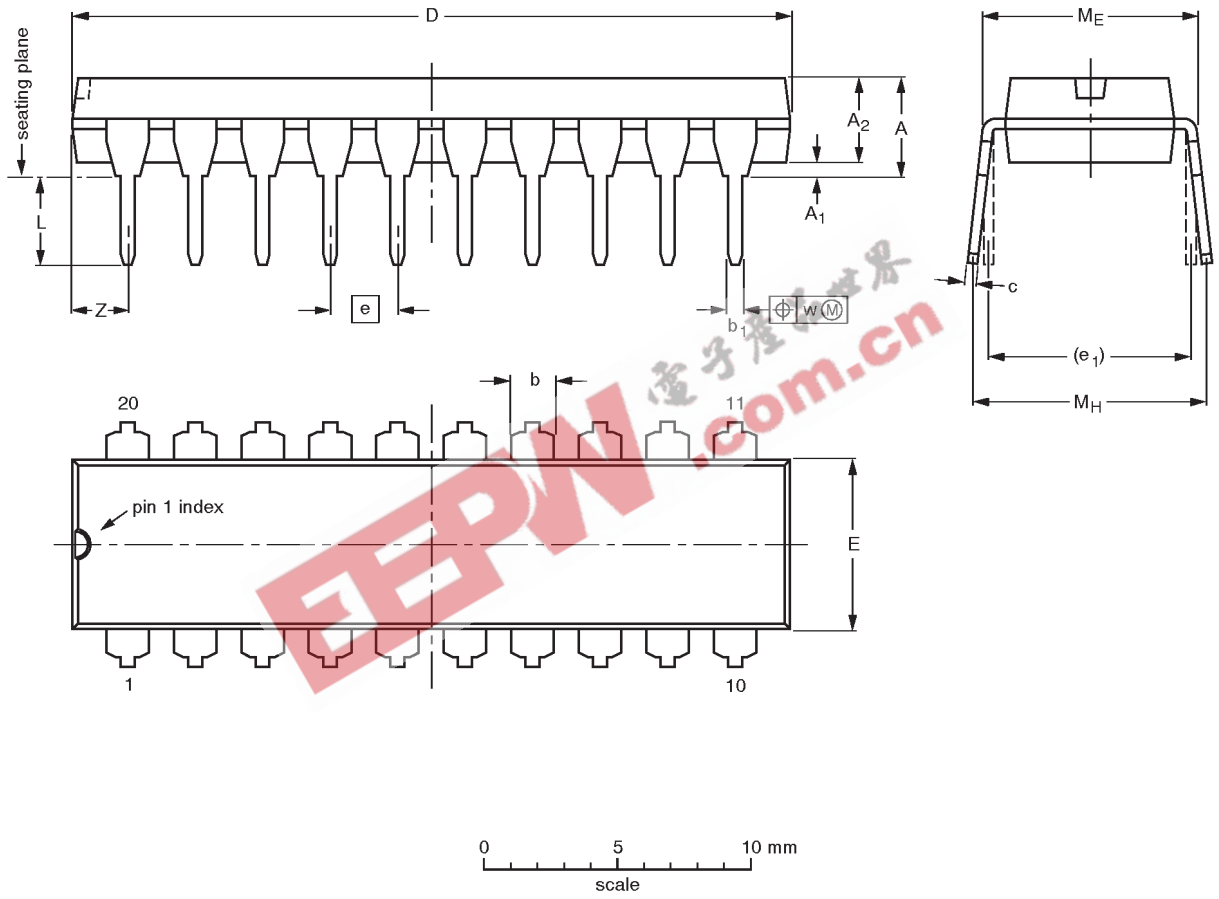
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

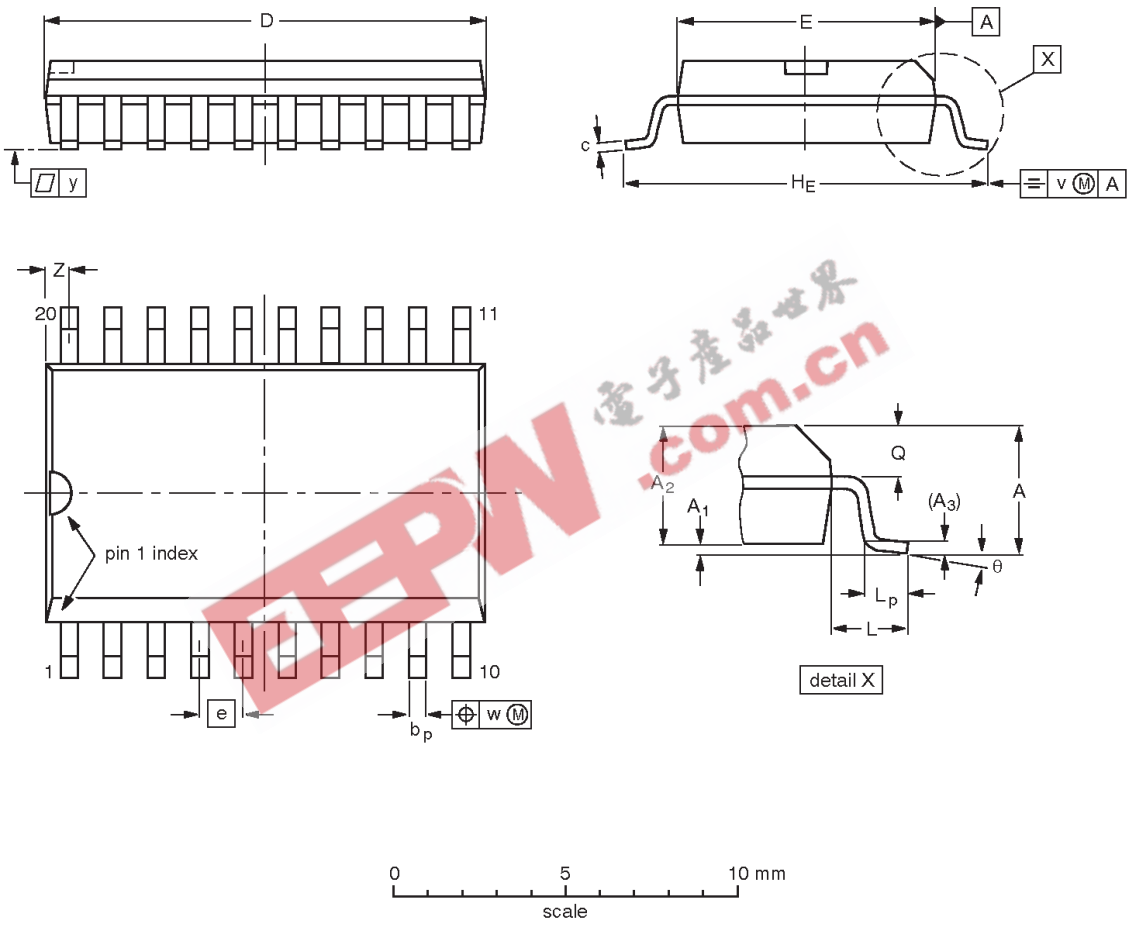
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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