

Octal 3-State Noninverting Transparent Latch

High-Performance Silicon-Gate CMOS

The MC54/74HC573A is identical in pinout to the LS573. The devices are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

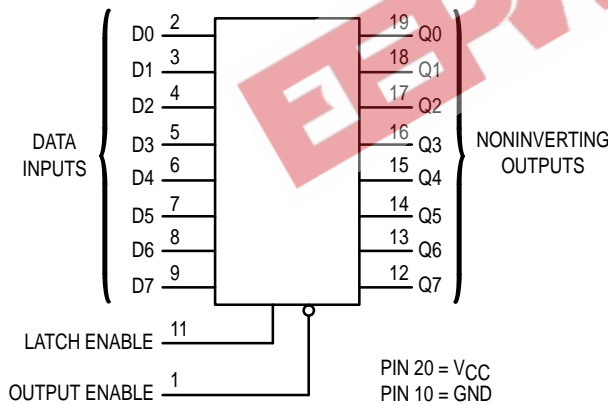
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The HC573A is identical in function to the HCT373A but has the data inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HC573A is the noninverting version of the HC563A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 218 FETs or 54.5 Equivalent Gates

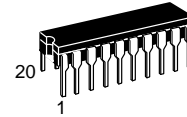
LOGIC DIAGRAM



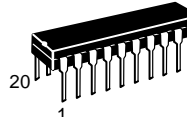
Design Criteria	Value	Units
Internal Gate Count*	54.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μ W
Speed Power Product	0.0075	pJ

* Equivalent to a two-input NAND gate.

MC54/74HC573A



J SUFFIX
CERAMIC PACKAGE
CASE 732-03



N SUFFIX
PLASTIC PACKAGE
CASE 738-03



DW SUFFIX
SOIC PACKAGE
CASE 751D-04



DT SUFFIX
TSSOP PACKAGE
CASE 948E-02

ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXADW	SOIC
MC74HCXXXADT	TSSOP

PIN ASSIGNMENT

OUTPUT ENABLE	1	20	VCC
D0	2	19	Q0
D1	3	18	Q1
D2	4	17	Q2
D3	5	16	Q3
D4	6	15	Q4
D5	7	14	Q5
D6	8	13	Q6
D7	9	12	Q7
GND	10	11	LATCH ENABLE

FUNCTION TABLE

Inputs		Output	
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care

Z = High Impedance



MC54/74HC573A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, TSSOP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
Ceramic DIP: - 10 mW/°C from 100° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	3.0	2.48	2.34	2.2	
			4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V _{OL}	Maximum Low-Level Output Voltage	V _{out} = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	3.0	0.26	0.33	0.4	
			4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	– 0.5	– 5.0	– 10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0	150	190	225	ns
		3.0	100	140	180	
		4.5	30	38	45	
		6.0	26	33	38	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0	160	200	240	ns
		3.0	105	145	190	
		4.5	32	40	48	
		6.0	27	34	41	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		3.0	100	125	150	
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		3.0	100	125	150	
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	60	75	90	ns
		3.0	27	32	36	
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance		10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)		15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Enabled Output)*	Typical @ 25°C, V _{CC} = 5.0 V		pF
		23		

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

MC54/74HC573A

TIMING REQUIREMENTS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6.0 \text{ ns}$)

Symbol	Parameter	Fig.	VCC Volts	Guaranteed Limit						Unit
				- 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Input D to Latch Enable	4	2.0	50		65		75		ns
			3.0	40		50		60		
			4.5	10		13		15		
			6.0	9.0		11		13		
t_h	Minimum Hold Time, Latch Enable to Input D	4	2.0	5.0		5.0		5.0		ns
			3.0	5.0		5.0		5.0		
			4.5	5.0		5.0		5.0		
			6.0	5.0		5.0		5.0		
t_w	Minimum Pulse Width, Latch Enable	2	2.0	75		95		110		ns
			3.0	60		80		90		
			4.5	15		19		22		
			6.0	13		16		19		
t_r, t_f	Maximum Input Rise and Fall Times	1	2.0		1000		1000		1000	ns
			3.0		800		800		800	
			4.5		500		500		500	
			6.0		400		400		400	



SWITCHING WAVEFORMS

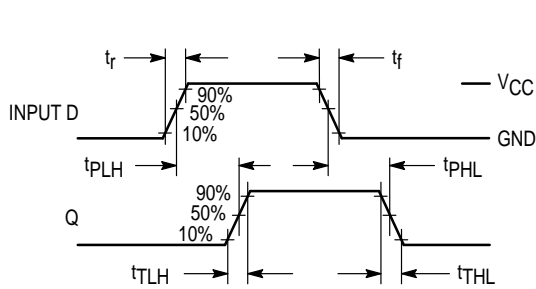


Figure 1.

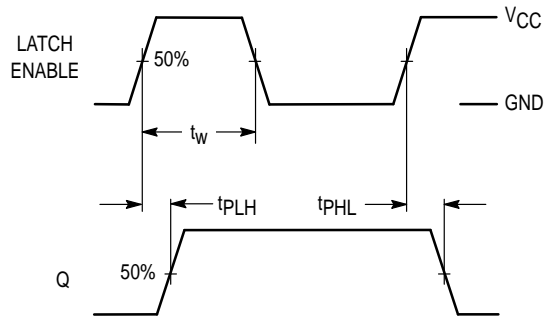


Figure 2.

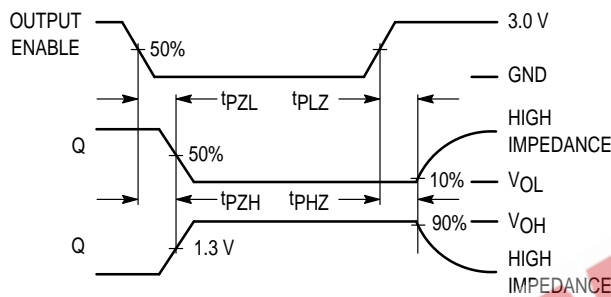


Figure 3.

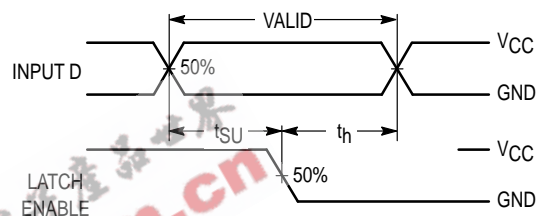
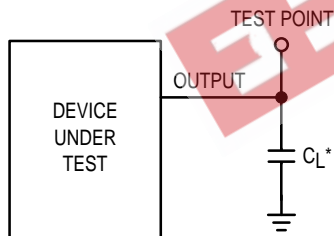
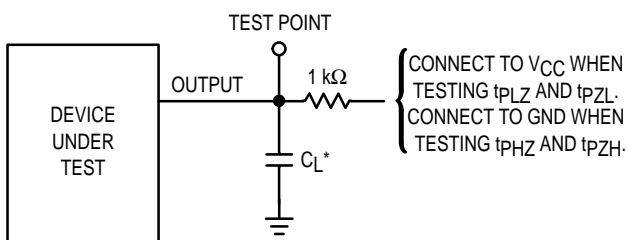


Figure 4.



* Includes all probe and jig capacitance

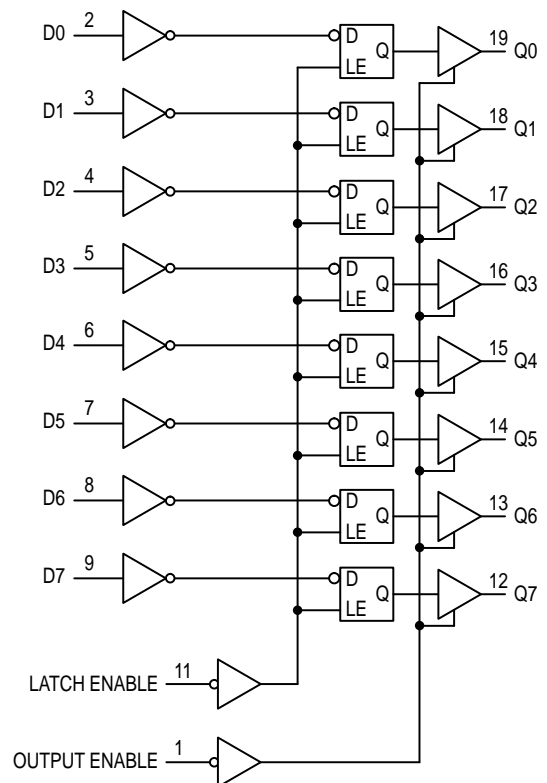
Figure 5. Test Circuit



* Includes all probe and jig capacitance

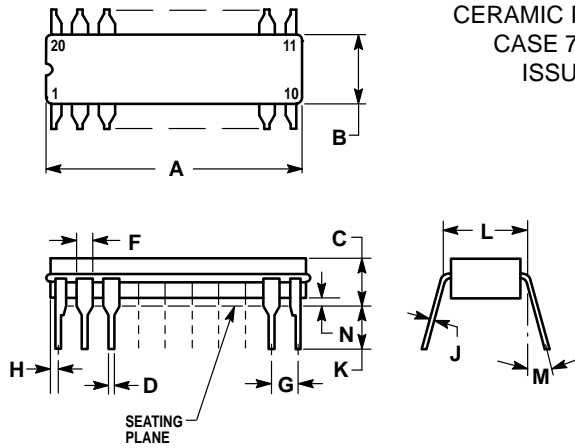
Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



OUTLINE DIMENSIONS

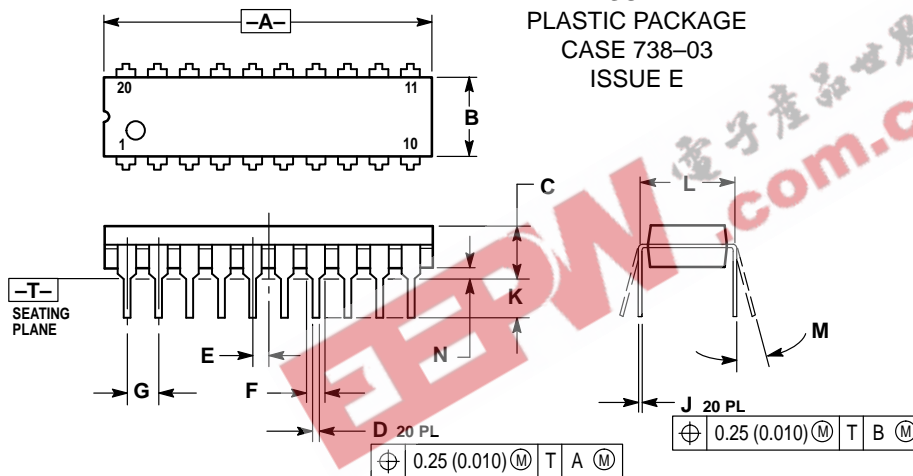
J SUFFIX
CERAMIC PACKAGE
CASE 732-03
ISSUE E



- NOTES:
- LEADS WITHIN 0.25 (0.010) DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
 - DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - DIMENSIONS A AND B INCLUDE MENISCUS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

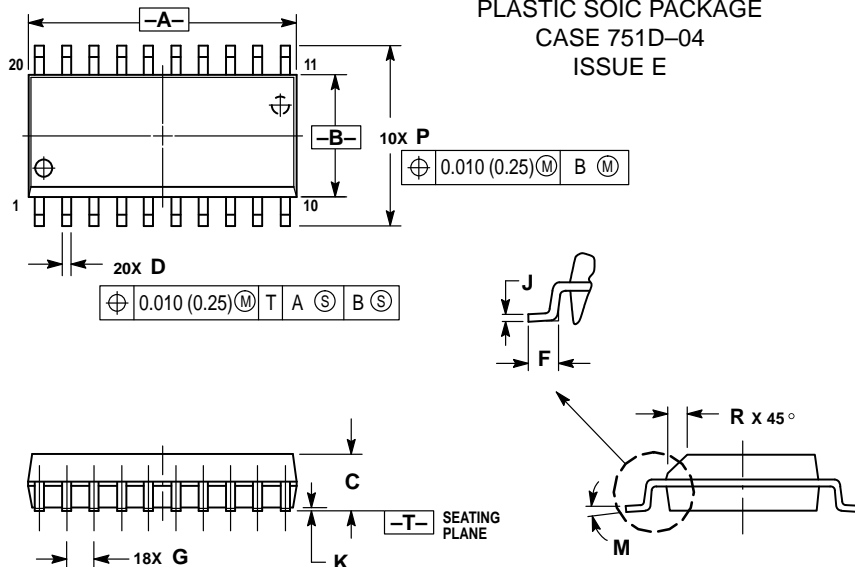
N SUFFIX
PLASTIC PACKAGE
CASE 738-03
ISSUE E



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.
 - DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 - DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-04
ISSUE E

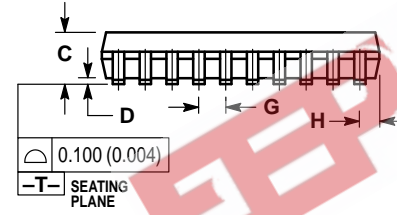
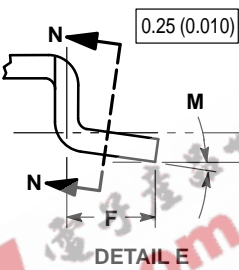
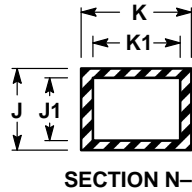
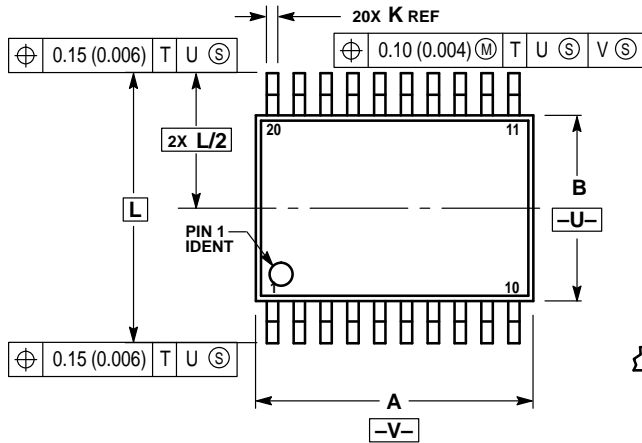


- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: MILLIMETER.
 - DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 - MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
 - DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E-02
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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