Register stack – 16×4 RAM 3-State output register 74F410

FEATURES

- Edge triggered output register
- ypical access time of 19.5ns
- Optimize for register stack operation
- 3–state outputs
- 18–pin package

DESCRIPTION

The 74F410 is a register oriented high speed 64–bit read/write memory organized as 16–words by 4–bits. An edge–triggered 4–bit output register allows new input data to be written while previous data is held. 3–state outputs are provided for maximum versatility.

The 74F410 is fully compatible with all TTL families.

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F410	19.5ns	45mA

FUNCTIONAL DESCRIPTION

Write operation – When the three control inputs, write enable ($\overline{WE}$), chip select ($\overline{CS}$), and clock (CP), are low the information on the data inputs (D0–D3) is written into the memory location selected by the address inputs (A0–A3). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are low, the contents of the selected memory location follow these changes provided setup and hold time criteria are met.

Read operation – When $\overline{CS}$ is low, $\overline{WE}$ is high, and CP goes from low–to–high, the contents of the memory location selected by the address inputs (A0–A3) are edge–triggered into the output register.
When $\overline{WE}$ is low, $\overline{CS}$ is low, CP goes from low–to–high, the data at the data inputs is edge–triggered into the output register. The $\overline{OE}$ input controls the output buffers. When $\overline{OE}$ is high the four outputs (Q0–Q3) are in a high impedance or off state; when $\overline{OE}$ is low, the outputs are determined by the state of the output register.

ORDERING INFORMATION

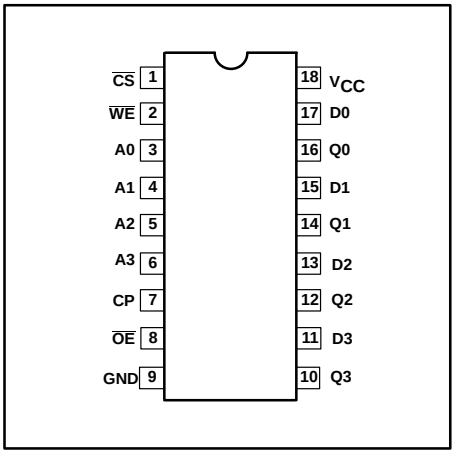
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
18–pin plastic DIP (300mil)	N74F410N

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

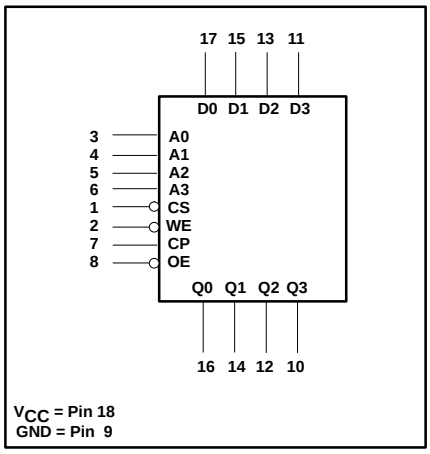
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20µA/0.6mA
A0 – A3	Address inputs	1.0/1.0	20µA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/2.0	20µA/1.2mA
$\overline{CS}$	Chip select input (active low)	1.0/2.0	20µA/1.2mA
$\overline{OE}$	Output enable input (active low)	1.0/1.0	20µA/0.6mA
$\overline{WE}$	Write enable input (active low)	1.0/1.0	20µA/0.6mA
Q0 – Q3	Data outputs	150/40	3mA/24mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

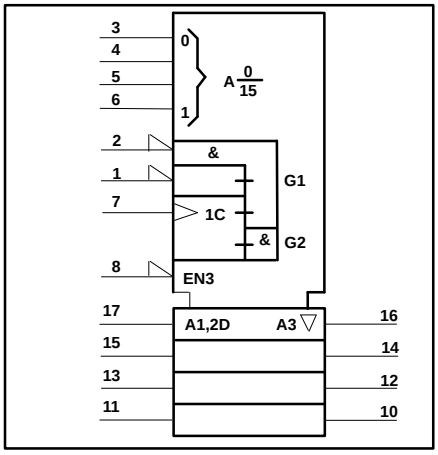
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



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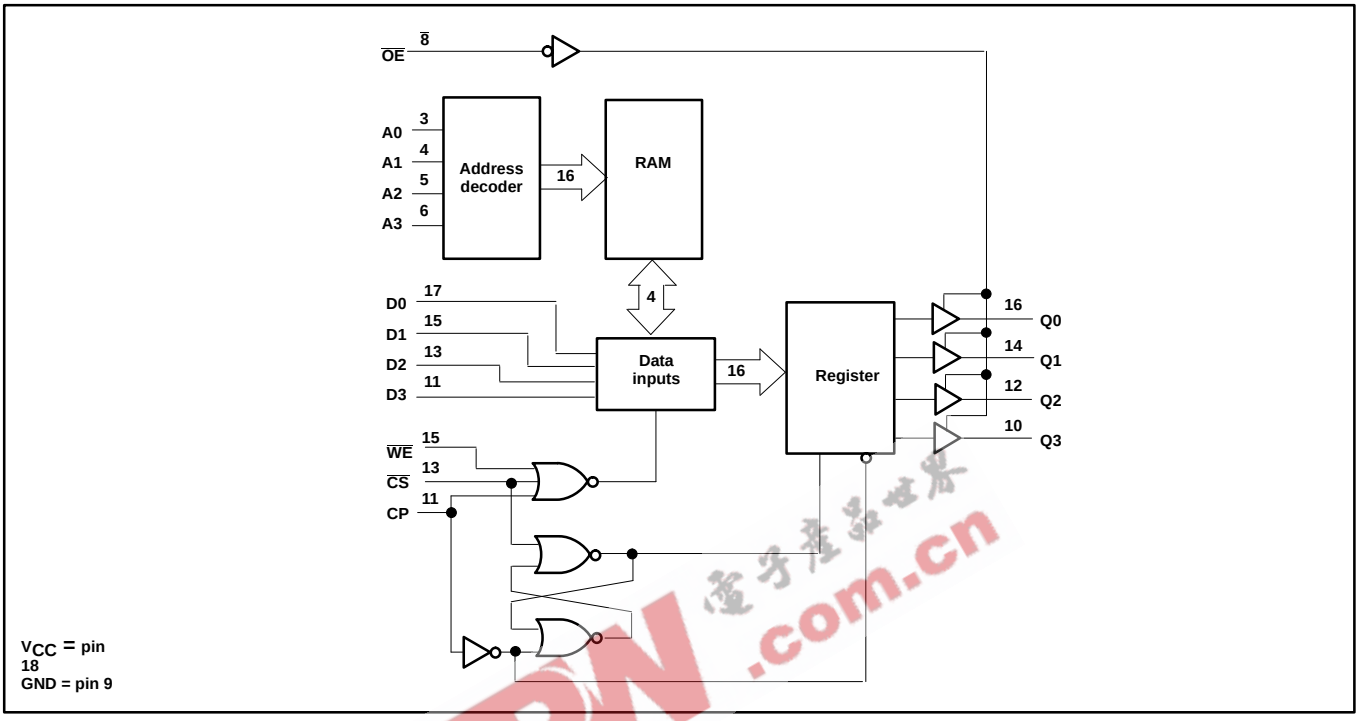
LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	48	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–3	mA
I_{OL}	Low–level output current			24	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current	others	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		CP, $\overline{CS}$					-1.2	mA
I_{OZH}	Offset–output current, high–level voltage applied		V_{CC} = MAX, V_I = 2.7V				50	µA
I_{OZL}	Offset–output current, low–level voltage applied		V_{CC} = MAX, V_I = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			45	70	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation dealy CP to Qn	Waveform 1	4.0 4.5	6.5 6.5	8.5 9.0	3.5 4.0	9.5 10.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to Qn	Waveform 3, 4	3.0 4.5	4.5 6.0	7.5 9.0	2.5 3.5	8.5 9.5	ns
t_{PHZ} t_{PHL}	Output disable time $\overline{OE}$ to Qn	Waveform 3, 4	2.0 2.0	3.5 3.5	6.0 6.5	1.5 2.0	6.5 7.0	ns

AC SETUP REQUIREMENTS FOR READ MODE

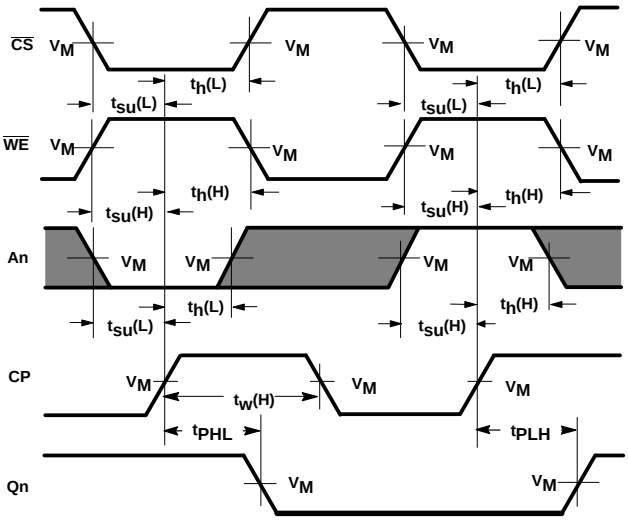
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{su}(L)$	Setup time, low, $\overline{CS}$ to CP[1]	Waveform 1	4.0			4.5		ns
$t_h(L)$	Hold time, low, $\overline{CS}$ to CP[1]	Waveform 1	3.5			4.5		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An to CP[1]	Waveform 1	13.0 13.0			15.0 15.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An to CP[1]	Waveform 1	0 0			0 0		ns
$t_{su}(H)$	Setup time, high, $\overline{WE}$ to CP[1]	Waveform 1	13.0			15.0		ns
$t_h(H)$	Hold time, high, $\overline{WE}$ to CP[1]	Waveform 1	0			0		ns
$t_w(L)$	CP pulse width, low	Waveform 1	5.0			6.0		ns

NOTE:
1. Low–to–high clock transition.

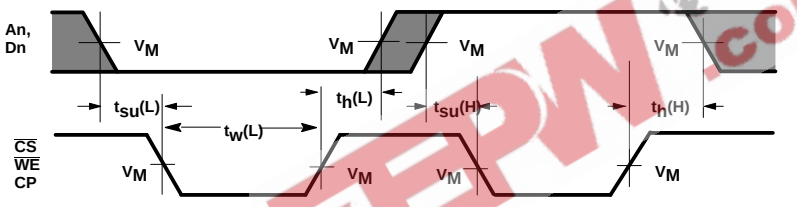
AC SETUP REQUIREMENTS FOR WRITE MODE

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	0 0			0 0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	0 0			0 0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Dn to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	6.0 6.0			8.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low Dn to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	0 0			0 0		ns
$t_w(L)$	$\overline{WE}$ pulse width, low	Waveform 2	7.0			8.0		ns
$t_w(L)$	$\overline{CS}$ pulse width, low	Waveform 2	6.0			7.0		ns
$t_w(L)$	CP pulse width, low	Waveform 2	7.0			8.0		ns

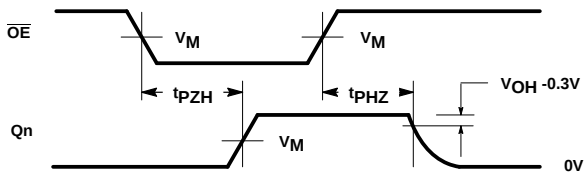
AC WAVEFORMS



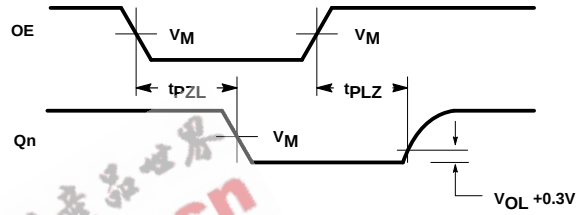
Waveform 1. Read cycle timing



Waveform 2. Write cycle timing



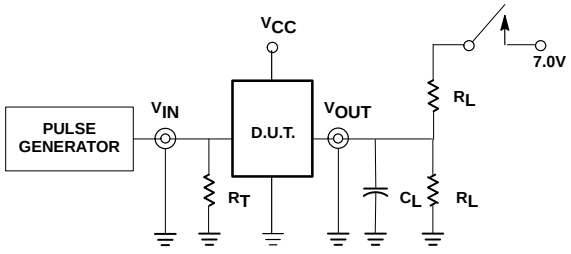
Waveform 3. 3-State output enable time to high level and output disable time from high level



Waveform 4. 3-State output enable time to low level and output disable time from low level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM

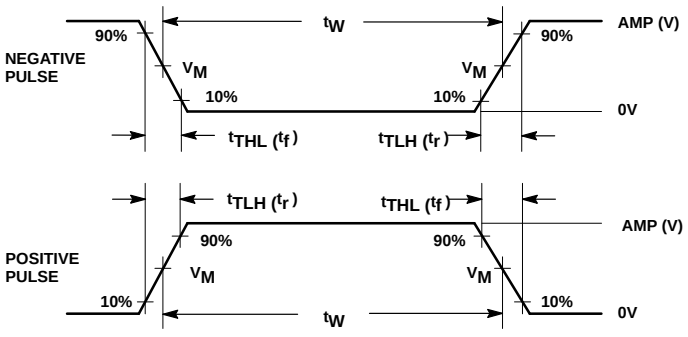


Test circuit for 3–state outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns