M2001 Series

5x7 mm, 3.3 Volt, CMOS/LVPECL/LVDS, Clock Oscillator

- Low cost oscillator series with jitter performance optimized specifically for Fibre Channel applications. CMOS, LVPECL, and LVDS versions available.
- Ideal for Fibre Channel, Storage Area Networks (SAN), and HDD Control

Ordering Information

M2001 — 1 — 5 — T — L — N — 00.0000 MHz

Product Series

Temperature Range
- **1:** 0°C to +70°C
- **2:** -40°C to +85°C
- **6:** -20°C to +70°C
- **7:** -0°C to +85°C
- **8:** 0°C to +50°C

Stability
- **3:** ±100 ppm
- **4:** ±50 ppm
- **6:** ±25 ppm
- **5:** ±35 ppm

Output Type
- **F:** Fixed
- **T:** Tristate

Symmetry/Output Logic Type
- **C:** 45/55% CMOS
- **L:** 45/55% LVDS
- **P:** 45/55% PECL

Package/Lead Configurations
- **N:** Leadless Ceramic

Frequency (customer specified)

Electrical Specifications

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	53.125		125	MHz	CMOS
		53.125		156.25	MHz	PECL/LVDS
Operating Temperature	TA	(See Ordering Information)				
Storage Temperature	Ts	-55		+125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				See Note 1
Aging						
1st Year			±2		ppm	
Thereafter (per year)			±1		ppm	
Input Voltage	Vcc/Vdd	3.135	3.3	3.465	V	
Input Current	Vdd/Idd			60	mA	CMOS/LVDS
				100	mA	PECL
Output Type						CMOS/PECL/LVDS
Load		15 pF				CMOS (See Note 2)
		50 Ohms to Vcc -2 VDC				PECL (See Note 3)
		100 Ohm differential load				LVDS (See Note 4)
Symmetry (Duty Cycle)		45	50	55	%	50% Vdd (CMOS)
(Per Symmetry Code)		45	50	55	%	Vcc -1.3 VDC (PECL)
		45	50	55	%	1.25 VDC (LVDS)
Output Skew				200	ps	PECL
Differential Voltage	Vo	250	340	450	mV	LVDS
Logic "1" Level	Voh	90% Vdd			V	CMOS
		Vcc -1.02			V	PECL
		1.375			V	LVDS
Logic "0" Level	Vol			10% Vdd	V	CMOS
				Vcc -1.63	V	PECL
				1.125	V	LVDS
Output Current		-4		+4	mA	CMOS
Rise/Fall Time	Tr/Tf			3	ns	CMOS @ 20/80%
			0.35	0.55	ns	LVPECL @ 20/80%
			.50	1.0	ns	LVDS @ 20/80%
Tristate Function		80% Vdd min or floating: output active 20% Vdd max: output disables to high-Z				
Start up Time			5		ms	
Peak to Peak Jitter (+/-)	Tj					@ BER 1E-12 (See Note 5)
			10	15	ps	CMOS
			15	20	ps	PECL/LVDS

1. Inclusive of initial tolerance, deviation over temperature, shock, vibration, voltage, and aging.
2. See load circuit diagram #2.
3. See load circuit diagram #5.
4. See load circuit diagram #9.
5. See jitter test circuit in Figure 1.

Revision: 4-26-06

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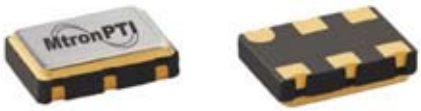
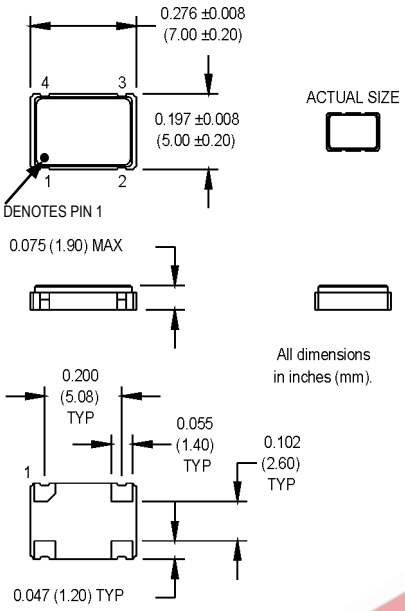
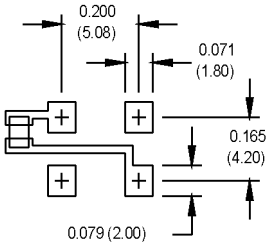


CMOS Output



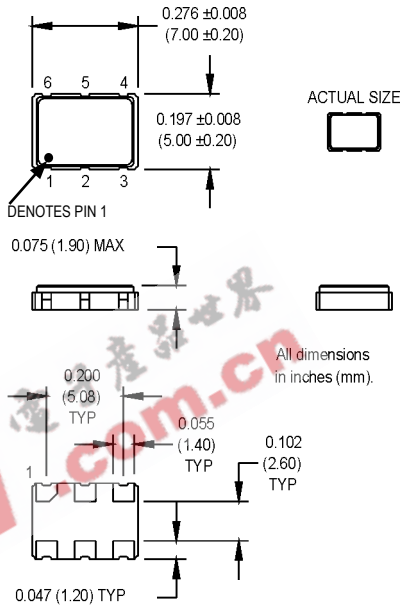
SUGGESTED SOLDER PAD LAYOUT



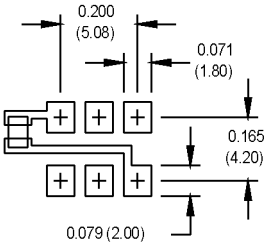
Pin Connections

PIN	FUNCTION
1	Tristate/NC
2	Ground
3	Output
4	+Vdd

LVPCEL/LVDS Output



SUGGESTED SOLDER PAD LAYOUT



Pin Connections

PIN	FUNCTION
1	Tristate
2	N/C
3	Ground
4	Output1/ Q
5	Output2/ $\overline{Q}$
6	+Vdd

Figure 1