

Hex Non-Inverting 3-State Buffer

The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

- 3-State Outputs
- TTL Compatible — Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|------------------------------------|---|--------------------------------|------|
| V _{DD} | DC Supply Voltage | - 0.5 to + 18.0 | V |
| V _{in} , V _{out} | Input or Output Voltage (DC or Transient) | - 0.5 to V _{DD} + 0.5 | V |
| I _{in} | Input Current (DC or Transient), per Pin | ± 10 | mA |
| I _{out} | Output Current (DC or Transient), per Pin | ± 25 | mA |
| P _D | Power Dissipation, per Package† | 500 | mW |
| T _{stg} | Storage Temperature | - 65 to + 150 | °C |
| T _L | Lead Temperature (8-Second Soldering) | 260 | °C |

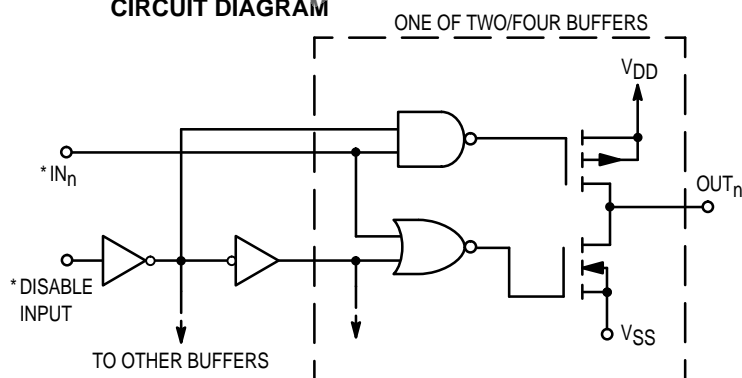
* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

CIRCUIT DIAGRAM

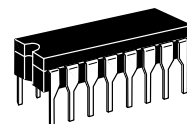


* Diode protection on all inputs (not shown)

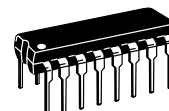
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

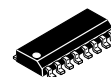
MC14503B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

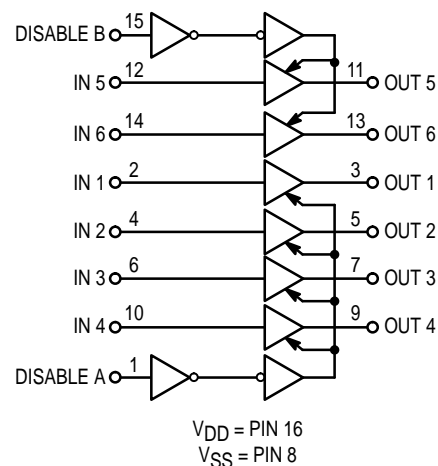
T_A = - 55° to 125°C for all packages.

TRUTH TABLE

| In _n | Appropriate Disable Input | Out _n |
|-----------------|---------------------------|------------------|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| X | 1 | High Impedance |

X = Don't Care

LOGIC DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V_{DD} Vdc | - 55°C | | 25°C | | | 125°C | | Unit | | | | |
|--|---------------------------------------|------------------|----------|--|-----------|-----------|--------------|---------------|-----------|-----------|-----------------|-----------------|-----------------|--|
| | | | Min | Max | Min | Typ # | Max | Min | Max | | | | | |
| Output Voltage $V_{in} = 0$ $V_{in} = V_{DD}$ | "0" Level V_{OL} | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc | | | | |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | | | | |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | | | | |
| | "1" Level V_{OH} | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | Vdc | | | | |
| | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | | | | | |
| | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | | | | | |
| Input Voltage ($V_O = 3.6$ or 1.4 Vdc) ($V_O = 7.2$ or 2.8 Vdc) ($V_O = 11.5$ or 3.5 Vdc) ($V_O = 1.4$ or 3.6 Vdc) ($V_O = 2.8$ or 7.2 Vdc) ($V_O = 3.5$ or 11.5 Vdc) | "0" Level V_{IL} | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | Vdc | | | | |
| | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | | | | | |
| | | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | | | | | |
| | "1" Level V_{IH} | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | Vdc | | | | |
| | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | | | | | |
| | | 15 | 11 | — | 11 | 8.25 | — | 11 | — | | | | | |
| Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc) | Source I_{OH} | 4.5 | - 4.3 | — | - 3.6 | - 5.0 | — | - 2.5 | — | mAdc | | | | |
| | | 5.0 | - 5.8 | — | - 4.8 | - 6.1 | — | - 3.0 | — | | | | | |
| | | 5.0 | - 1.2 | — | - 1.02 | - 1.4 | — | - 0.7 | — | | | | | |
| | | 10 | - 3.1 | — | - 2.6 | - 3.7 | — | - 1.8 | — | | | | | |
| | | 15 | - 8.2 | — | - 6.8 | - 14.1 | — | - 4.8 | — | | | | | |
| | | Sink I_{OL} | 4.5 | 2.2 | — | 1.8 | 2.1 | — | 1.2 | | — | mAdc | | |
| | 5.0 | | 2.6 | — | 2.1 | 2.3 | — | 1.3 | — | | | | | |
| | 10 | | 6.5 | — | 5.5 | 6.2 | — | 3.8 | — | | | | | |
| | 15 | | 19.2 | — | 16.1 | 25 | — | 11.2 | — | | | | | |
| | Input Current | | I_{in} | 15 | — | ± 0.1 | — | ± 0.00001 | ± 0.1 | — | ± 1.0 | | μAdc | |
| | Input Capacitance ($V_{in} = 0$) | | C_{in} | — | — | — | — | 5.0 | 7.5 | — | — | | pF | |
| | Quiescent Current (Per Package) | | I_Q | 5.0 | — | 1.0 | — | 0.002 | 1.0 | — | 30 | μAdc | | |
| | | | 10 | — | 2.0 | — | 0.004 | 2.0 | — | 60 | | | | |
| | | | 15 | — | 4.0 | — | 0.006 | 4.0 | — | 120 | | | | |
| Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs) (All outputs switching, 50% Duty Cycle) | | I_T | 5.0 | $I_T = (2.5 \mu\text{A/kHz}) f + I_{DD}$ | | | | | | | μAdc | | | |
| | | | 10 | $I_T = (6.0 \mu\text{A/kHz}) f + I_{DD}$ | | | | | | | | | | |
| | | | 15 | $I_T = (10 \mu\text{A/kHz}) f + I_{DD}$ | | | | | | | | | | |
| Three-State Output Leakage Current | | I_{TL} | 15 | — | ± 0.1 | — | ± 0.0001 | ± 0.1 | — | ± 3.0 | μAdc | | | |

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V_{fk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.006$.

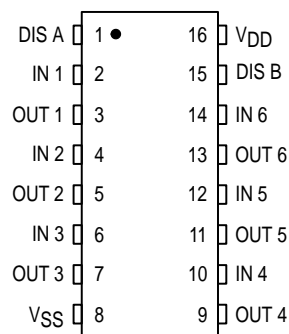
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V _{DD} V _{CC} | All Types | | Unit |
|--|-----------|------------------------------------|-----------------|-----------------|------|
| | | | Typ # | Max | |
| Output Rise Time $t_{TLH} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.3 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{TLH} = (0.2 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ | t_{TLH} | 5.0 10 15 | 45 23 18 | 90 45 35 | ns |
| Output Fall Time $t_{THL} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.3 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{THL} = (0.2 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ | t_{THL} | 5.0 10 15 | 45 23 18 | 90 45 35 | ns |
| Turn-Off Delay Time, all Outputs $t_{PLH} = (0.3 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{PLH} = (0.15 \text{ ns/pF}) C_L + 27 \text{ ns}$ $t_{PLH} = (0.1 \text{ ns/pF}) C_L + 20 \text{ ns}$ | t_{PLH} | 5.0 10 15 | 75 35 25 | 150 70 50 | ns |
| Turn-On Delay Time, all Outputs $t_{PHL} = (0.3 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{PHL} = (0.15 \text{ ns/pF}) C_L + 27 \text{ ns}$ $t_{PHL} = (0.1 \text{ ns/pF}) C_L + 20 \text{ ns}$ | t_{PHL} | 5.0 10 15 | 75 35 25 | 150 70 50 | ns |
| 3-State Propagation Delay Time Output "1" to High Impedance Output "0" to High Impedance High Impedance to "1" Level High Impedance to "0" Level | t_{PHZ} | 5.0 10 15 | 75 40 35 | 150 80 70 | ns |
| | t_{PLZ} | 5.0 10 15 | 80 40 35 | 160 80 70 | ns |
| | t_{PZH} | 5.0 10 15 | 65 25 20 | 130 50 40 | ns |
| | t_{PZL} | 5.0 10 15 | 100 35 25 | 200 70 50 | ns |

* The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

PIN ASSIGNMENT



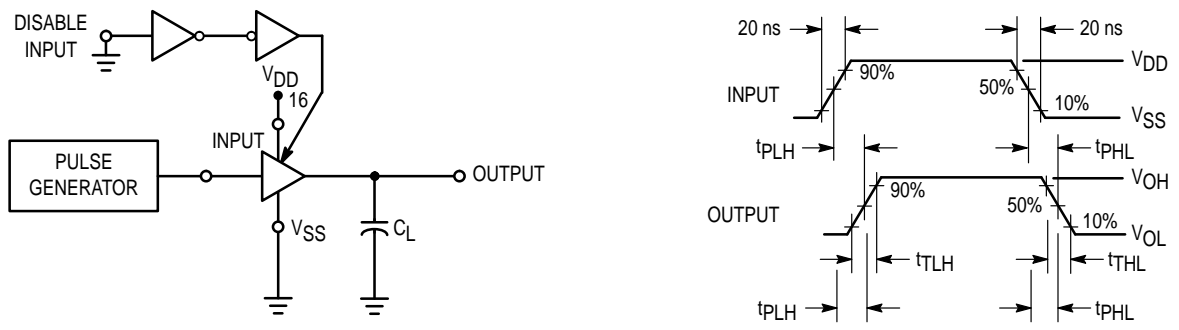


Figure 1. Switching Time Test Circuit and Waveforms (t_{TLH} , t_{THL} , t_{PHL} , and t_{PLH})

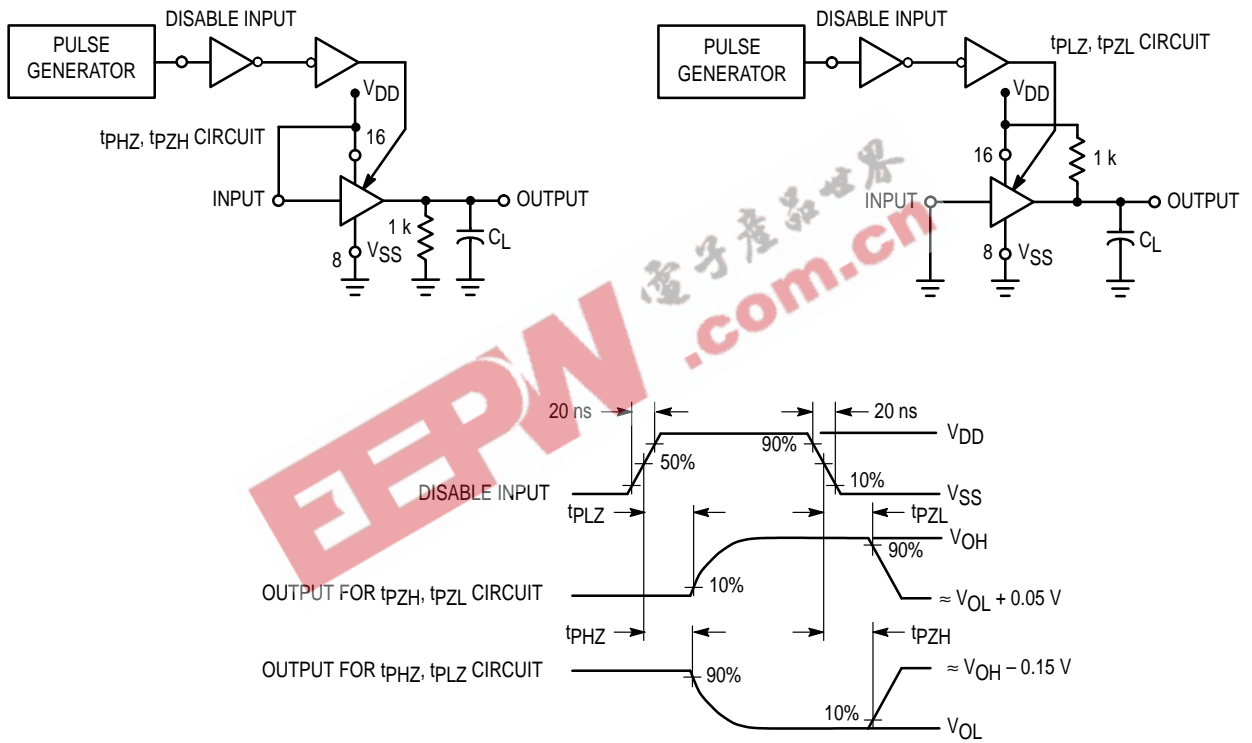
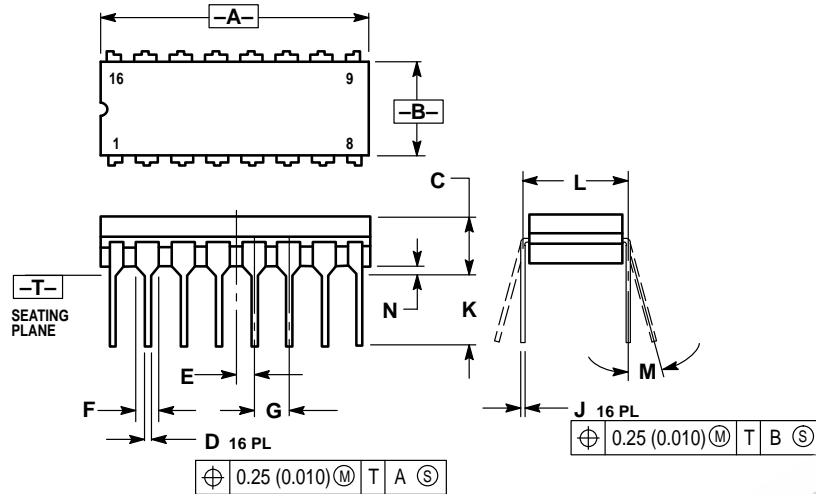


Figure 2. 3-State AC Test Circuit and Waveforms (t_{PLZ} , t_{PHZ} , t_{PZH} , t_{PZL})

OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

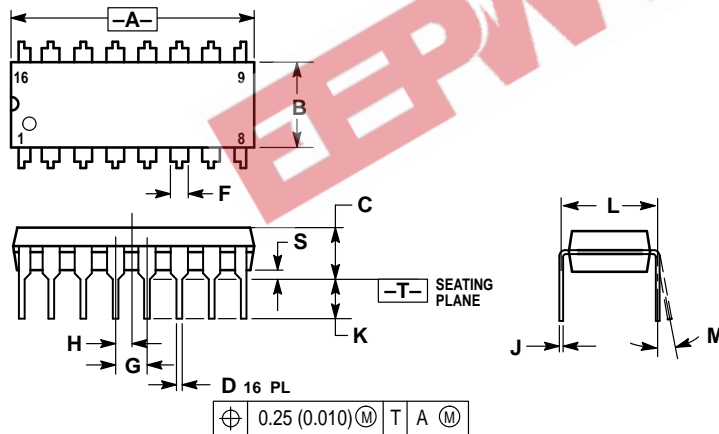


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.750 | 0.785 | 19.05 | 19.93 |
| B | 0.240 | 0.295 | 6.10 | 7.49 |
| C | — | 0.200 | — | 5.08 |
| D | 0.015 | 0.020 | 0.39 | 0.50 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.055 | 0.065 | 1.40 | 1.65 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.125 | 0.170 | 3.18 | 4.31 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



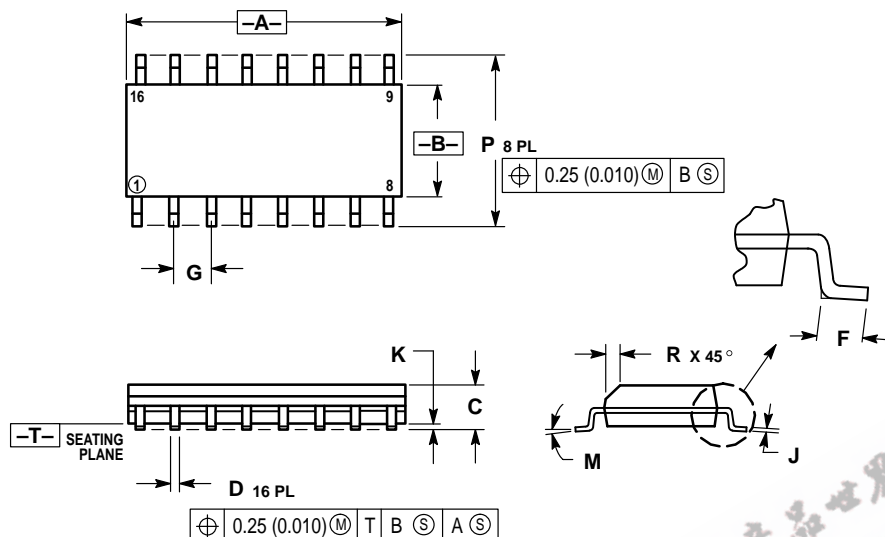
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

OUTLINE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

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MC14503B/D

