Noninverting 3-State Buffer

The MC74VHC1G126 is an advanced high speed CMOS noninverting 3-state buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power

The internal circuit is composed of three stages, including a buffered 3-state output which provides high noise immunity and stable output.

The MC74VHC1G126 input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the MC74VHC1G126 to be used to interface 5.0 V circuits to 3.0 V circuits.

Features

- High Speed: $t_{PD} = 3.5 \text{ ns}$ (Typ) at $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu A \text{ (Max)}$ at $T_A = 25 \text{°C}$

- Pin and Function Compatible with Other Standard Logic Families
 Chip Complexity: FETs = 58; Equivalent Gates = 15
 Pb-Free Packages

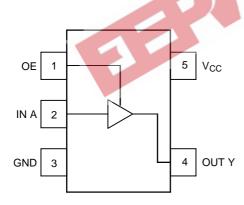


Figure 1. Pinout (Top View)



Figure 2. Logic Symbol



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MARKING DIAGRAMS



SC-88A/SOT-353/SC-70 **DF SUFFIX CASE 419A**





TSOP-5/SOT-23/SC-59 DT SUFFIX **CASE 483**



W2 = Device Code M = Date Code* = Assembly Location Α Υ = Year W = Work Week

= Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT					
1	OE				
2	IN A				
3	GND				
4	OUT Y				
5	V _{CC}				

FUNCTION TABLE

A Input	OE Input	Y Output
L	Н	L
Н	Н	Н
X	L	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol		Value	Unit	
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V
V _{IN}	DC Input Voltage		-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	V _{CC} = 0 High or Low State	-0.5 to 7.0 -0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current		-20	mA
I _{OK}	Output Diode Current	V _{OUT} < GND; V _{OUT} > V _{CC}	+20	mA
I _{OUT}	DC Output Current, per Pin		+25	mA
I _{CC}	DC Supply Current, V _{CC} and GN	D	+50	mA
P_{D}	Power dissipation in still air	SC-88A, TSOP-5	200	mW
θ_{JA}	Thermal resistance	SC-88A, TSOP-5	333	°C/W
TL	Lead temperature, 1 mm from ca	se for 10 s	260	°C
TJ	Junction temperature under bias		+150	°C
T _{stg}	Storage temperature		-65 to +150	°C
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 200 N/A	V
I _{Latchup}	Latchup Performance	Above V _{CC} and Below GND at 125°C (Note 4)	±500	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- 1. Tested to EIA/JESD22-A114-A
- 2. Tested to EIA/JESD22-A115-A
- 3. Tested to JESD22–C101–A
- 4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V _{CC}	DC Supply Voltage		2.0	5.5	V
V _{IN}	DC Input Voltage		0.0	5.5	V
V _{OUT}	DC Output Voltage		0.0	V_{CC}	V
T _A	Operating Temperature Range		- 55	+125	°C
t _r , t _f	Input Rise and Fall Time	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0	100 20	ns/V

Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

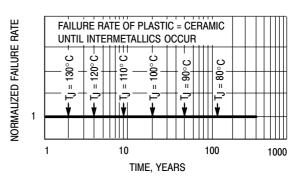


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

			v _{cc}	Т	T _A = 25°C		T _A ≤	85°C	-55 ≤ T _A	≤ 125°C	
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		٧
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	٧
V _{OH}	Minimum High–Level Output Voltage V _{IN} = V _{IH} or V _{IL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		٧
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA $I_{OH} = -8$ mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V _{OL}	Maximum Low–Level Output Voltage V _{IN} = V _{IH} or V _{IL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu\text{A}$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0 4.5		25.	0.36 0.36	8-	0.44 0.44		0.52 0.52	V
I _{OZ}	Maximum 3–State Leakage Current	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or GND}$	5.5	36	多學	±0.25	CV.	±2.5		±2.5	μΑ
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5	CIL	₀ 0	±0.1		±1.0		±1.0	μΑ
I _{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			1.0		20		40	μΑ

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_{f} = t_{f} = 3.0 ns

			1	A = 25°	C	T _A ≤	85°C	-55 ≤ T _A	≤ 125°C	
Symbol	Parameter	Test Conditions	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay,	$V_{CC} = 3.3 \pm 0.3 \text{ VC}_{L} = 15 \text{ pF}$ $C_{L} = 50 \text{ pF}$		4.5 6.4	8.0 11.5		9.5 13.0		12.0 16.0	ns
	Input A to Y (Figures 3. and 5.)	$V_{CC} = 5.0 \pm 0.5 \text{ VC}_{L} = 15 \text{ pF}$ $C_{L} = 50 \text{ pF}$		3.5 4.5	5.5 7.5		6.5 8.5		8.5 10.5	
t _{PZL} , t _{PZH}	Maximum Output Enable Time,	$\begin{array}{c} V_{CC} = 3.3 \pm 0.3 \; V C_L = 15 \; pF \\ R_L = 1000 \; \Omega \qquad C_L = 50 \; pF \end{array}$		4.5 6.4	8.0 11.5		9.5 13.0		11.5 15.0	ns
	Input OE to Y (Figures 4. and 5.)	$ \begin{array}{c} V_{CC} = 5.0 \pm 0.5 \; VC_L = 15 \; pF \\ R_L = 1000 \; \Omega \qquad C_L = 50 \; pF \end{array} $		3.5 4.5	5.1 7.1		6.0 8.0		8.5 10.5	
t _{PLZ} , t _{PHZ}	Maximum Output Disable Time,	$\begin{array}{c} V_{CC} = 3.3 \pm 0.3 \; V C_L = 15 \; pF \\ R_L = 1000 \; \Omega \qquad C_L = 50 \; pF \end{array}$		6.5 8.0	9.7 13.2		11.5 15.0		14.5 18.0	ns
	Input OE to Y (Figures 4. and 5.)	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		4.8 7.0	6.8 8.8		8.0 10.0		10.0 12.0	
C _{IN}	Maximum Input Capacitance			4.0	10		10		10	pF
C _{OUT}	Maximum 3–State Output Capacitance (Output in High Impedance State)			6.0						pF

		Typical @ 25°C, V _{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 5)	8.0	pF

^{5.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

SWITCHING WAVEFORMS

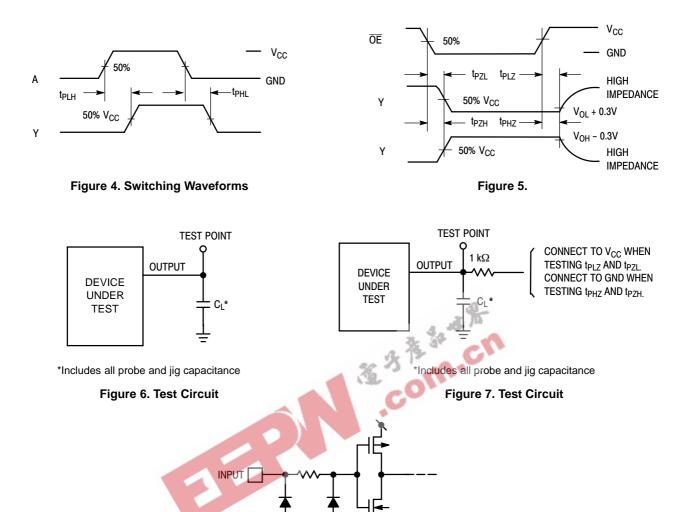


Figure 8. Input Equivalent Circuit

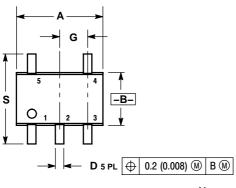
DEVICE ORDERING INFORMATION

Device Order Number	Package Type	Tape and Reel Size [†]
MC74VHC1G126DFT1	SC-88A/SOT-353/SC-70	178 mm (7") 3000 Units / Tape & Reel
M74VHC1G126DFT1G	SC-88A/SOT-353/SC-70 (Pb-Free)	178 mm (7") 3000 Units / Tape & Reel
MC74VHC1G126DFT2	SC-88A/SOT-353/SC-70	178 mm (7") 3000 Units / Tape & Reel
M74VHC1G126DFT2G	SC-88A/SOT-353/SC-70 (Pb-Free)	178 mm (7") 3000 Units / Tape & Reel
MC74VHC1G126DTT1	TSOP-5/SOT-23/SC-59	178 mm (7") 3000 Units / Tape & Reel
M74VHC1G126DTT1G	TSOP-5/SOT-23/SC-59 (Pb-Free)	178 mm (7") 3000 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

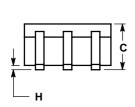
SC-88A / SOT-353 / SC70 CASE 419A-02 **ISSUE H**

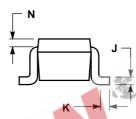




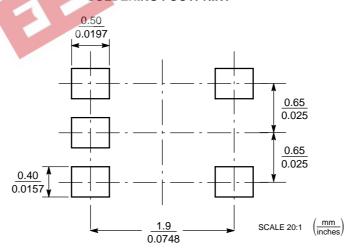
- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE RURRS. BURRS.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.071	0.087	1.80	2.20	
В	0.045	0.053	1.15	1.35	
С	0.031	0.043	0.80	1.10	
D	0.004	0.012	0.10	0.30	
G	0.026	BSC	0.65 BSC		
Н		0.004		0.10	
J	0.004	0.010	0.10	0.25	
K	0.004	0.012	0.10	0.30	
N	0.008 REF		0.20	REF	
S	0 .079	0.087	2.00	2.20	





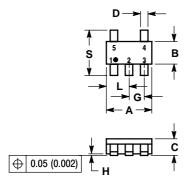
SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSOP-5 / SOT23-5 / SC59-5 DT SUFFIX CASE 483-02 ISSUE D



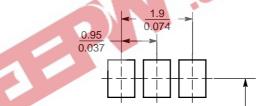


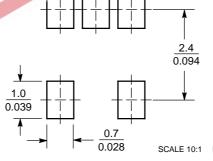
SOLDERING FOOTPRINT

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: MILLIMETER.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.1142	0.1220
В	1.30	1.70	0.0512	0.0669
С	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
Н	0.013	0.100	0.0005	0.0040
J 🦽	0.10	0.26	0.0040	0.0102
K.	0.20	0.60	0.0079	0.0236
ille :	1.25	1.55	0.0493	0.0610
M	0 °	10°	0°	10°
S	2.50	3.00	0.0985	0.1181





*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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