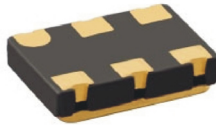


M2001 Series

5x7 mm, 3.3 Volt, CMOS/LVPECL/LVDS, Clock Oscillator



- Low cost oscillator series with jitter performance optimized specifically for Fibre Channel applications. CMOS, LVPECL, and LVDS versions available.
- Ideal for Fibre Channel, Storage Area Networks (SAN), and HDD Control

Ordering Information

Product Series	M2001	1	5	T	L	N	00.0000	MHz
Temperature Range	1: 0°C to +70°C	2: -40°C to +85°C	6: -20°C to +70°C	7: 0°C to +85°C	8: 0°C to +50°C			
Stability	3: ±100 ppm	4: ±50 ppm	6: ±25 ppm	5: ±35 ppm				
Output Type	F: Fixed	T: Tristate						
Symmetry/Output Logic Type	C: 45/55 CMOS	L: 45/55 LVDS						
Package/Lead Configurations	N: Leadless Ceramic							
Frequency (customer specified)								

M2001Sxxx - Contact factory for datasheet

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	53.125		125	MHz	CMOS
		53.125		156.25	MHz	PECL/LVDS
Operating Temperature	T _a	(See ordering information)				
Storage Temperature	T _s	-55		+125	°C	
Frequency Stability	ΔF/F	(See ordering information)				
Aging						See Note 1
1 st Year			±2		ppm	
Thereafter (per year)			±1		ppm	
Input Voltage	V _{cc} /V _{dd}	3.135	3.3	3.465	V	
Input Current	V _{dd} /I _{dd}			60	mA	CMOS/LVDS
				100	mA	PECL
Output Type						CMOS/PECL/LVDS
Load		15 pF				CMOS (See Note 2)
		50 Ohms to V _{cc} -2 VDC				PECL (See Note 3)
		100 Ohms differential load				LVDS (See Note 4)
Symmetry (Duty Cycle)		45	50	55	%	50% V _{dd} (CMOS)
		45	50	55	%	V _{cc} -1.3 VDC (PECL)
		45	50	55	%	1.25 VDC (LVDS)
Output Skew				200	ps	PECL
Differential Voltage	V _o	250	340	450	mV	LVDS
Logic "1" Level	V _{oh}	90% V _{dd}			V	CMOS
		V _{cc} -1.02			V	PECL
		1.375			V	LVDS
Logic "0" Level	V _{ol}			10% V _{dd}	V	CMOS
				V _{cc} -1.63	V	PECL
				1.125	V	LVDS
Output Current		-4		+4	mA	CMOS
Rise/Fall Time	T _r /T _f		0.35	0.55	ns	CMOS @20/80%
			.50	1.0	ns	LVPECL @ 20/80%
					ns	LVDS @ 20/80%
Tristate Function		80% V _{dd} min or floating: output active				
		20% V _{dd} max: output disables to high-Z				
Start up Time				10	ms	
Peak to Peak Jitter (+/-)	T _j		10	15	ps	@ BER 1E-12 (See Note 5)
			15	20	ps	CMOS
						PECL/LVDS
Mechanical Shock		Per MIL-STD-202, Method 213, Condition C (100 g's, 6 mS duration, ½ sinewave)				
Vibration		Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)				
Hermeticity		Per MIL-STD-202, Method 112, (1x10 ⁻⁵ atm. cc/s of Helium)				
Thermal Cycle		Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles)				
Solderability		Per EIAJ-STD-002				
Max Soldering Conditions		See solder profile, Figure 1				

1. Inclusive of initial tolerance, deviation over temperature, shock, vibration, voltage and aging.
2. See Load circuit diagram #2.
3. See Load circuit diagram #5.
4. See Load circuit diagram #9.
5. See jitter test circuit in Figure 1.

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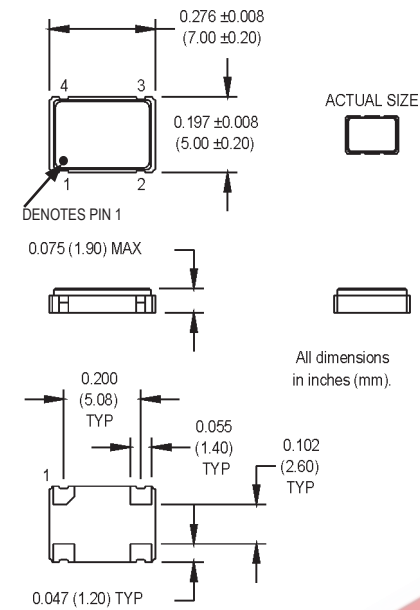
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M2001 Series

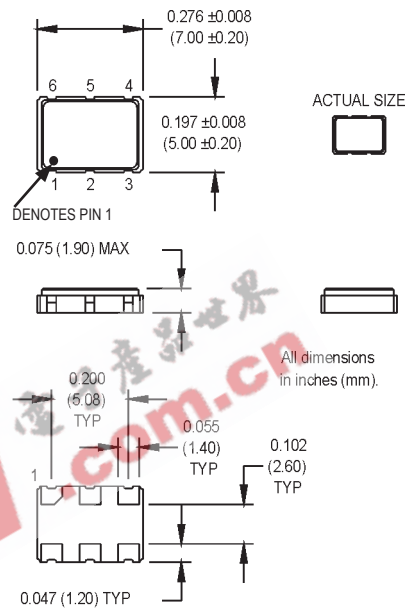
5x7 mm, 3.3 Volt, CMOS/LVPECL/LVDS, Clock Oscillator



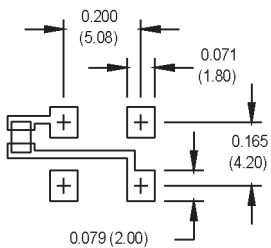
CMOS Output



LVPECL/LVDS Output



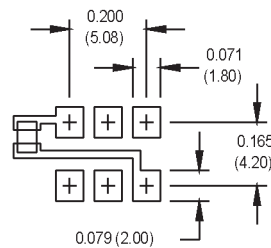
SUGGESTED SOLDER PAD LAYOUT



Pin Connections

PIN	FUNCTION
1	Tristate/NC
2	Ground
3	Output
4	+Vdd

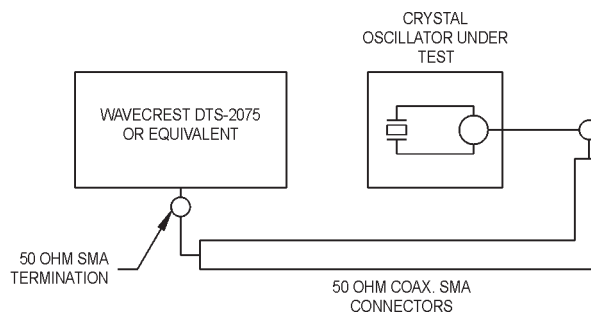
SUGGESTED SOLDER PAD LAYOUT



Pin Connections

PIN	FUNCTION
1	Tristate
2	N/C
3	Ground
4	Output1/ Q
5	Output2/ \bar{Q}
6	+Vdd

Figure 1



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MtronPTI Lead Free Solder Profile

