

Octal 3-State Inverting D Flip-Flop

High-Performance Silicon-Gate CMOS

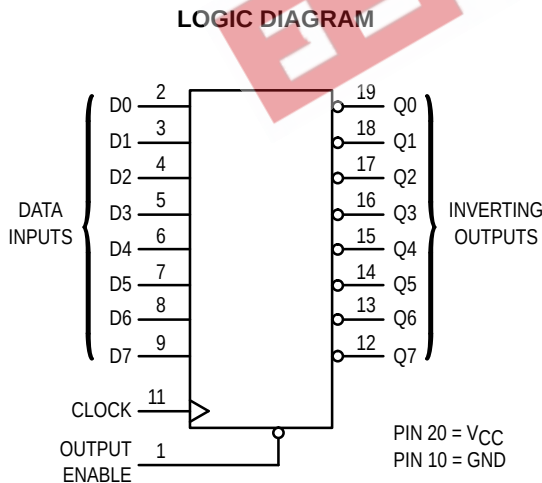
The MC74HC564 is identical in pinout to the LS564. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is identical in function to the HC534A but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

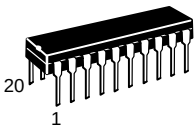
Data meeting the setup time is clocked, in inverted form, to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC564 is the inverting version of the HC574A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 282 FETs or 70.5 Equivalent Gates



MC74HC564



N SUFFIX
PLASTIC PACKAGE
CASE 738-03



DW SUFFIX
SOIC PACKAGE
CASE 751D-04

ORDERING INFORMATION

MC74HCXXXN Plastic
MC74HCXXXDW SOIC

PIN ASSIGNMENT

OUTPUT ENABLE	1	20	V _{CC}
D0	2	19	Q0
D1	3	18	Q1
D2	4	17	Q2
D3	5	16	Q3
D4	6	15	Q4
D5	7	14	Q5
D6	8	13	Q6
D7	9	12	Q7
GND	10	11	CLOCK

FUNCTION TABLE

Inputs			Output
Output Enable	Clock	D	Q
L		H	L
L		L	H
L	L, H,	X	No Change
H	X	X	Z

X = don't care
Z = high impedance



MC74HC564

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C

SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or } GND$	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		38	

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _h	Minimum Hold Time, Clock to Data (Figure 3)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

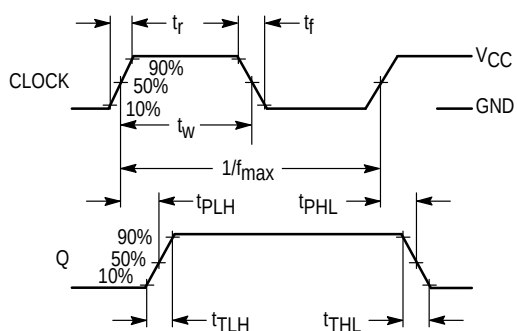


Figure 1.

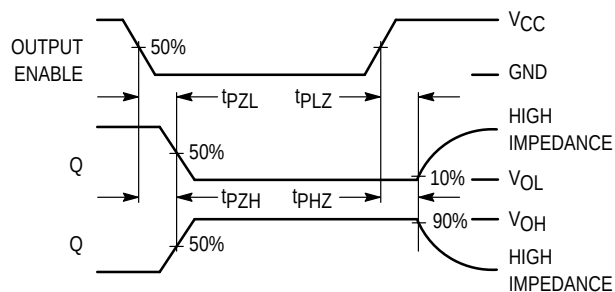


Figure 2.

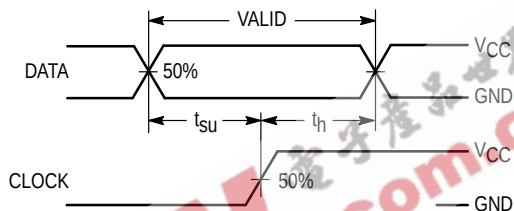
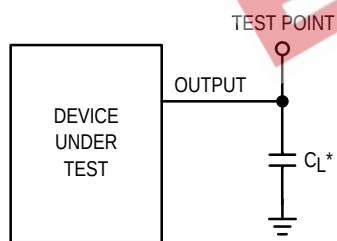


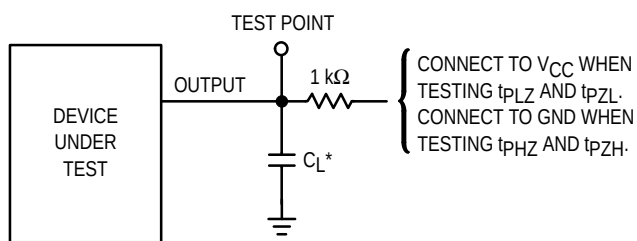
Figure 3.

TEST CIRCUITS



* Includes all probe and jig capacitance

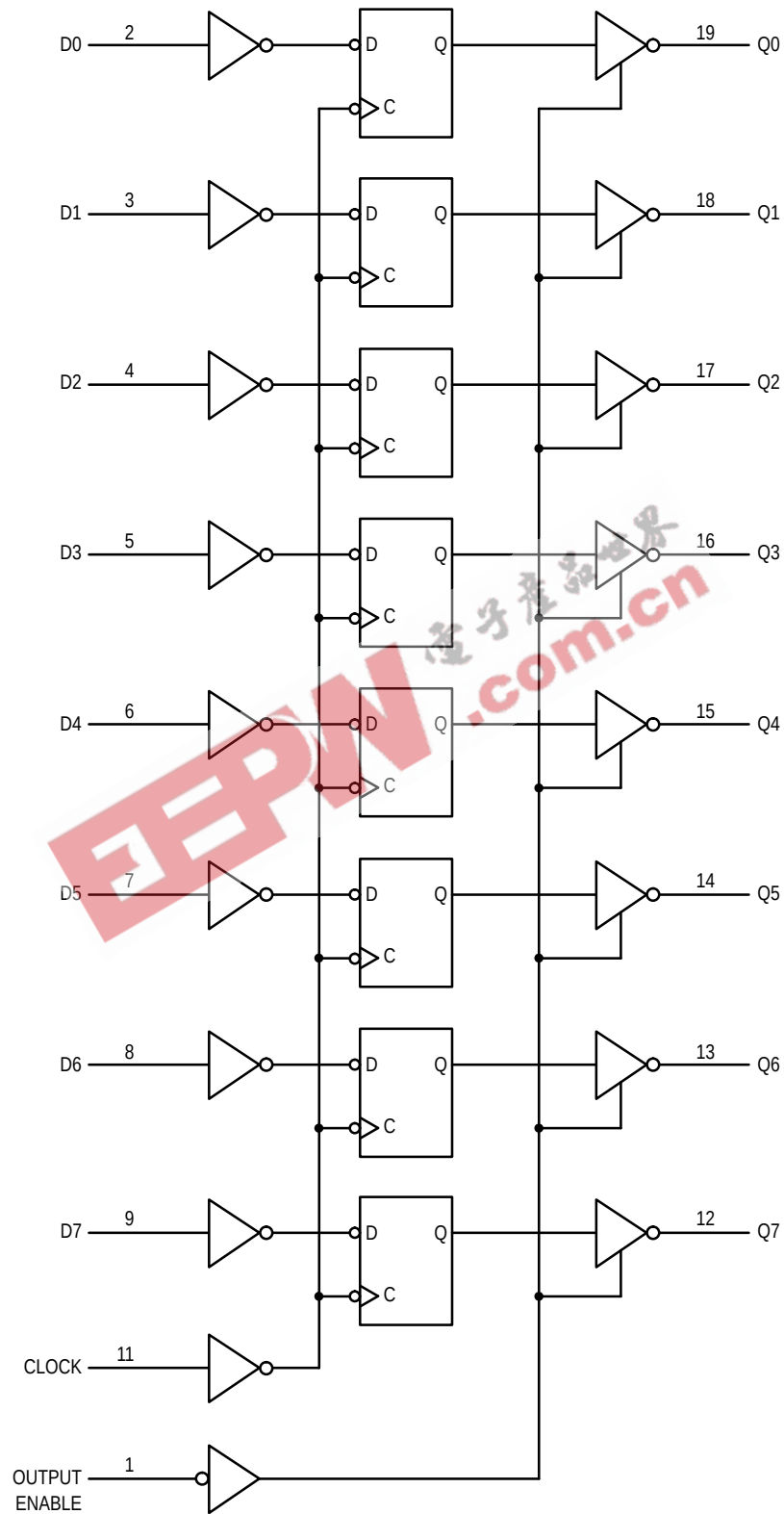
Figure 4.



* Includes all probe and jig capacitance

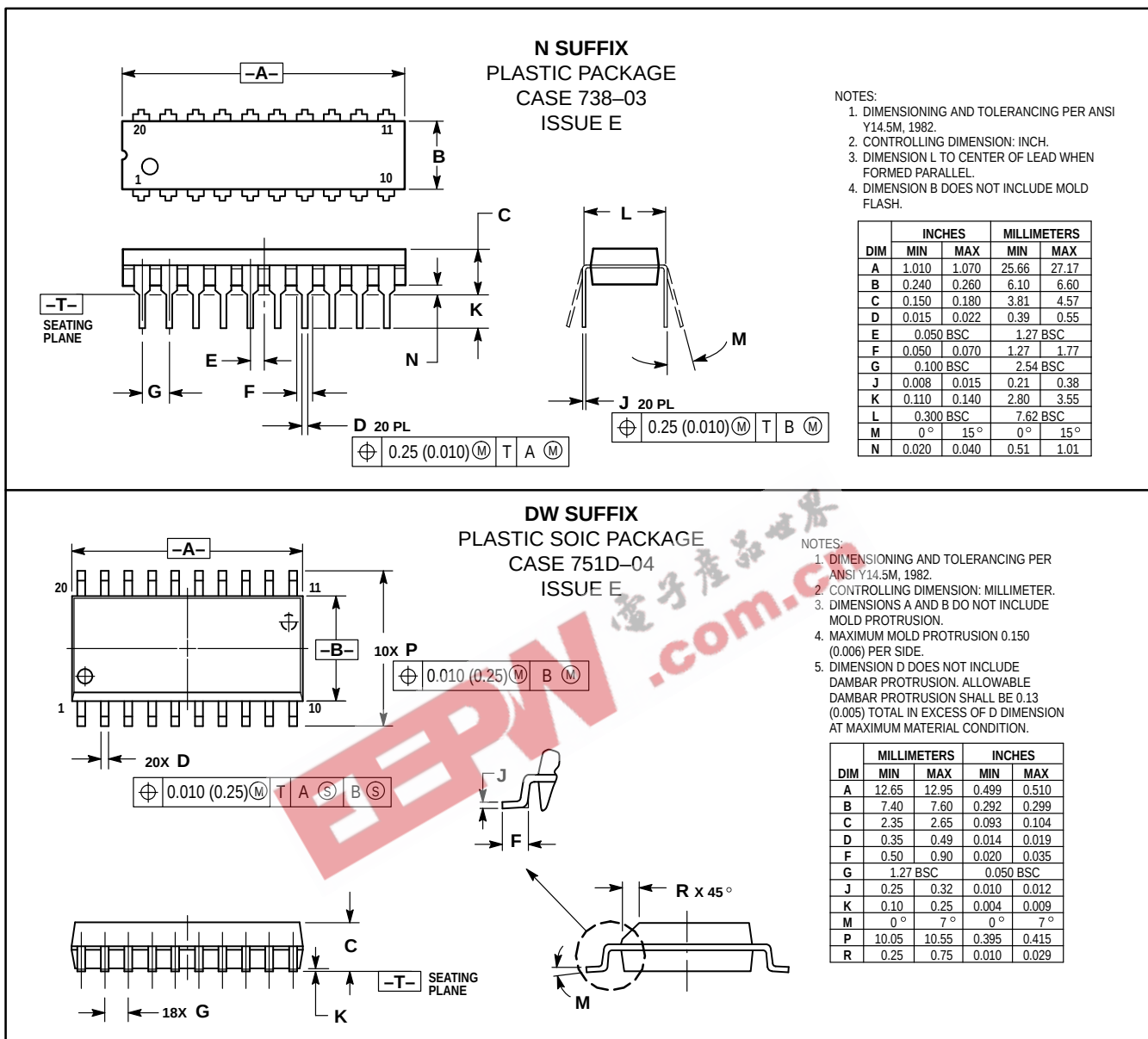
Figure 5.

EXPANDED LOGIC DIAGRAM



MC74HC564

OUTLINE DIMENSIONS



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