16 × 4 Synchronous FIFO (3-State) 74F224

FEATURES

- Independent synchronous inputs and outputs
- Organized as 16 words of 4 bits
- DC to 50MHz data rate
- 3-State outputs
- Cascadable in word–width and depth direction

DESCRIPTION

This 64-bit active element First-In-First-Out (FIFO) is a monolithic Schottky-clamped transistor-transistor logic (STLL) array organized as 16 words of 4-bits each. A memory system using the 74F224 can be easily expanded in multiples of 15m+1 words or of 4n bits, or both (where n is the number of packages in the horizontal array).

However, an external gating is required (see Figure 1). For longer words using 74F224, the IR signals of the first-rank packages and OR signals of the last-rank packages must be ANDed for proper synchronization.The 3-State outputs controlled by a single input (OE) make bus connection and multiplexing easy.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F224	50MHz	90mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
16-pin plastic Dual In-line Package	N74F224N	0406C
16-pin plastic Small Outline Large	N74F224D	0171B

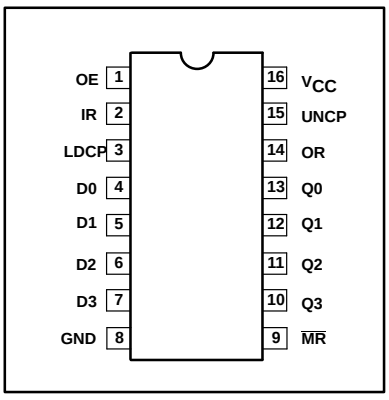
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
LDCP	Load clock input	1.0/1.0	20µA/0.6mA
D0 – D3	Data inputs	1.0/1.0	20µA/0.6mA
OE	Output enable input (active high)	1.0/1.0	20µA/0.6mA
UNCP	Unload clock input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master reset input (active low)	1.0/1.0	20µA/0.6mA
IR	Input ready output	50/33	1.0mA/20mA
Q0 – Q3	Data outputs	50/33	1.0mA/20mA
OR	Output ready output	50/33	1.0mA/20mA

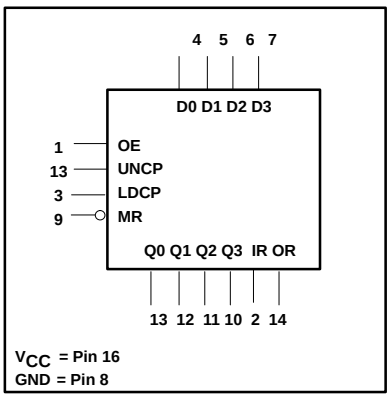
NOTE TO INPUT AND OUTPUT LOADING AND FAN OUT TABLE

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

PIN CONFIGURATION



LOGIC SYMBOL



IED/IEEE SYMBOL