

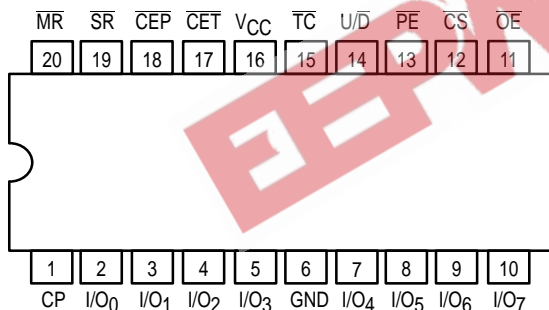


# 8-BIT BIDIRECTIONAL BINARY COUNTER (3-STATE)

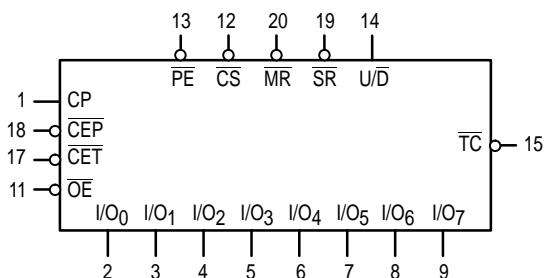
The MC74F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-state I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a  $\overline{U/D}$  input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock.  $\overline{TC}$  output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

- Multiplexed 3-State I/O Ports For Bus-oriented Applications
- Built-In Cascading Carry Capability
- Count Frequency 115 MHz Typ
- Supply Current 100 mA Typ
- Fully Synchronous Operation
- U/D Pin to Control Direction of Counting
- Separate Pins for Master Reset and Synchronous Reset
- Center Power Pins to Reduce Effects of Package Inductance
- See F269 for 24-Pin Separate I/O Port Version
- See F779 for 16-Pin Version
- ESD Protection > 4000 Volts

### PIN ASSIGNMENT



### LOGIC SYMBOL



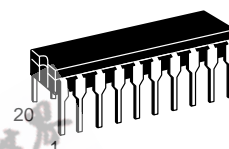
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current — High	$\overline{TC}$		-1.0	mA
		$I/O_n$		-3.0	
$I_{OL}$	Output Current — Low	$\overline{TC}$		20	mA
		$I/O_n$		24	

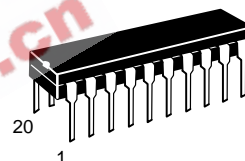
## MC74F579

### 8-BIT BIDIRECTIONAL BINARY COUNTER (3-STATE)

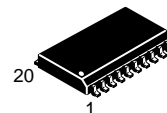
FAST™ SCHOTTKY TTL



**J SUFFIX**  
CERAMIC  
CASE 732-03



**N SUFFIX**  
PLASTIC  
CASE 738-03



**DW SUFFIX**  
SOIC  
CASE 751D-03

### ORDERING INFORMATION

MC74FXXXJ Ceramic  
MC74FXXXN Plastic  
MC74FXXXDW SOIC

# MC74F579

## FUNCTION TABLE

MR	SR	CS	PE	CEP	CET	U/D	OE	CP	Function
X	X	H	X	X	X	X	X	X	I/O <sub>0</sub> to I/O <sub>7</sub> in Hi-Z ( $\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/O <sub>0</sub> to I/O <sub>7</sub> in Hi-Z
X	X	L	H	X	X	X	L	X	Flip-Flop outputs appear on I/O lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ( $\overline{TC}$ held high)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = High voltage level  
 X = Don't care  
 (not LL) = CS and PE should never both be low voltage at the same time

L = Low voltage level  
 ↑ = Low-to-High clock transition

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	74F			Unit	Test Conditions (Note 1)	
		Min	Typ (2)	Max			
V <sub>OH</sub>	Output HIGH Voltage	TC	2.5			V	I <sub>OH</sub> = -1.0 mA V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN V <sub>CC</sub> = 4.5 V
			2.7	3.4			V <sub>CC</sub> = 4.75 V
		I/O <sub>n</sub>	2.4	3.3		V	I <sub>OH</sub> = -3.0 mA V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN V <sub>CC</sub> = 4.5 V
			2.7	3.3			V <sub>CC</sub> = 4.75 V
V <sub>OL</sub>	Output LOW Voltage	$\overline{TC}$		0.35	V	I <sub>OL</sub> = 20 mA V <sub>CC</sub> = 4.5 V V <sub>IL</sub> = MAX	
		I/O <sub>n</sub>		0.5		I <sub>OL</sub> = 24 mA V <sub>IH</sub> = MIN	
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.73	-1.2	V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA	
I <sub>IH</sub>	Input HIGH Current	I/O <sub>n</sub>		1.0	mA	V <sub>CC</sub> = 5.5 V	V <sub>IN</sub> = 5.5 V
		others		100			V <sub>IN</sub> = 7.0 V
		I/O <sub>n</sub>		70	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V	
		others		20			
I <sub>IL</sub>	Input LOW Current	Except I/O <sub>n</sub>		-0.6	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	
I <sub>OZH</sub>	OFF-State Current High-Level Voltage Applied	I/O <sub>n</sub>		70	μA	V <sub>CC</sub> = 5.5 V	V <sub>OUT</sub> = 2.7 V
I <sub>OZL</sub>	OFF-State Current Low-Level Voltage Applied			-600			V <sub>OUT</sub> = 0.5 V
I <sub>OS</sub>	Output Short Circuit Current (Note 3)		-60	-80	-150	mA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0 V
I <sub>CC</sub>	Total Supply Current (total)	I <sub>CC</sub> H		95	135	mA	V <sub>CC</sub> = MAX
		I <sub>CC</sub> L		105	145		
		I <sub>CC</sub> Z		105	150		

### NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the applicable device type.
- All typical values are at V<sub>CC</sub> = 5.0 V, T<sub>A</sub> = 25°C.
- Not more than one output should be shorted at a time. For I<sub>OS</sub> testing, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

# MC74F579

## AC ELECTRICAL CHARACTERISTICS

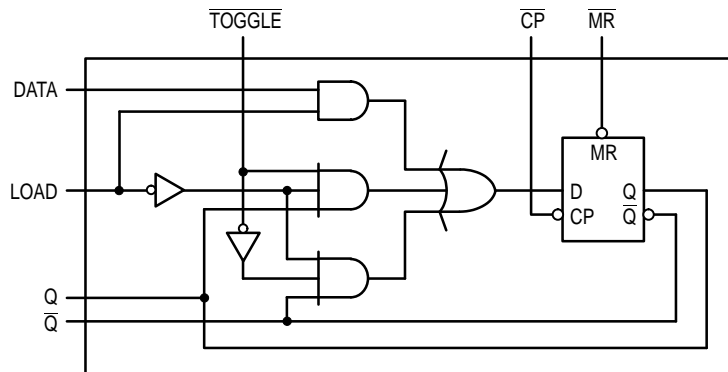
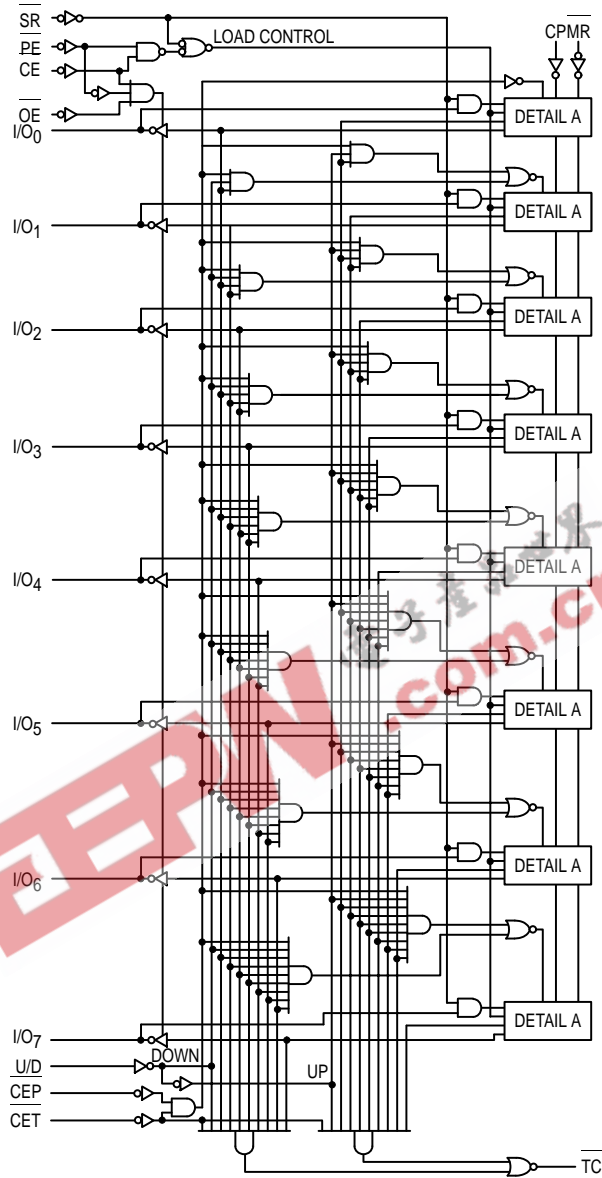
Symbol	Parameter	74F			74F		Unit
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0 V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0 V ±10% C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	100			80		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to I/O <sub>n</sub>	5.0 5.0		10.5 10.5	5.0 5.0	11.5 11.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to $\overline{TC}$	4.5 5.5		10 10	4.5 5.0	11 11	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay U/D to $\overline{TC}$	3.5 4.5		8.0 8.0	3.5 4.5	9.0 9.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.5 3.5		7.0 8.0	3.5 3.5	8.5 8.5	ns
t <sub>PHL</sub>	Propagation Delay $\overline{MR}$ to I/O <sub>n</sub>	5.0		10	5.0	11	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to HIGH or LOW Level $\overline{CS}$ , $\overline{PE}$ to I/O <sub>n</sub>	4.5 6.5		10.5 10.5	4.5 6.0	11.5 11.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time to HIGH or LOW Level $\overline{CS}$ , $\overline{PE}$ to I/O <sub>n</sub>	3.0 4.0		7.5 9.5	3.0 4.0	9.0 11	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to HIGH or LOW Level $\overline{OE}$ to I/O <sub>n</sub>	4.0 6.0		8.5 9.5	4.0 5.0	9.5 10.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time to HIGH or LOW Level $\overline{OE}$ to I/O <sub>n</sub>	1.0 2.5		6.0 7.0	1.0 2.5	6.5 8.0	ns

## AC SETUP REQUIREMENTS

Symbol	Parameter	74F			74F			Unit
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0 V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0 V ±10% C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t <sub>s(H)</sub> t <sub>s(L)</sub>	Setup Time, HIGH or LOW I/O <sub>n</sub> to CP	3.0 3.0			4.0 4.0		ns	
t <sub>h(H)</sub> t <sub>h(L)</sub>	Hold Time, HIGH or LOW I/O <sub>n</sub> to CP	1.0 1.0			1.0 1.0		ns	
t <sub>s(H)</sub> t <sub>s(L)</sub>	Setup Time, HIGH or LOW $\overline{PE}$ , $\overline{SR}$ or $\overline{CS}$ to CP	9.5 9.5			10 10		ns	
t <sub>h(H)</sub> t <sub>h(L)</sub>	Hold Time, HIGH or LOW $\overline{PE}$ , $\overline{SR}$ or $\overline{CS}$ to CP	0 0			0 0		ns	
t <sub>s(H)</sub> t <sub>s(L)</sub>	Setup Time, HIGH or LOW $\overline{CET}$ , $\overline{CEP}$ to CP	5.0 9.0			5.5 10.5		ns	
t <sub>h(H)</sub> t <sub>h(L)</sub>	Hold Time, HIGH or LOW $\overline{CET}$ , $\overline{CEP}$ to CP	0 0			0 0		ns	
t <sub>w</sub>	CP Pulse Width	4.5			6.0		ns	
t <sub>w(L)</sub>	$\overline{MR}$ Pulse Width	3.5			4.5		ns	
t <sub>rec</sub>	$\overline{MR}$ Recovery Time	4.0			4.5		ns	

# MC74F579

## LOGIC DIAGRAM



Detail A